90-180 GHz Heterostructure Monolithic Integrated Doubler*

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Abstract

This paper demonstrates the design, theory, monolithic integrated circuit (MMIC) implementation, and 180 GHz operation of a doubler based on HEMT technology. Doublers were fabricated on an InP substrate using submicron ($0.1\mu m$) InAlAs/InGaAs HEMT's. Microstrip lines were utilized for the various matching components. The doubler 90 GHz input drive was varied from approximately -10 dBm to +8 dBm as measured at the test fixture input. Conversion loss varied from approximately 6dB to 10dB and was minimum at an input drive level of approximately 0 dBm.

Introduction

Space based sensor applications where gas molecule resonances are studied at several hundred GHz require high frequency receiver functions such as frequency mixing and oscillation. Two terminal device sources such as IMPATT's and TUNNET's are reported to operate at frequencies which are normally below 200 GHz. The traditional approach for extending the frequency limits of oscillator sources above 100 GHz is frequency multiplication. This is usually performed using two-terminal multiplier diodes. The high frequency characteristics of FET's, however, suggest the possibility of three-terminal devices for such applications. In fact, the transistor approach can allow conversion gain and better efficiency than diodes which normally require relatively higher power drive levels. Also, input and output isolation is superior in FET structures. Monolithic implementations of GaAs FET doublers are also possible and have, for example, been demonstrated up to 40 GHz [1][2]. Three terminal devices such as MESFET's and

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HEMT's also offer the possibility of integrating the various receiver functions on the same chip. Amplifiers, mixers, oscillators and multiplier could consequently be realized through the use of monolithic integrated circuit technology.

HEMT's based on InAlAs/InGaAs material system have shown state-of-the-art discrete device performance with maximum oscillation frequency (f_{max}) of 450 GHz [3]. Furthermore, strained designs with excess indium in the channel show improved carrier confinement and improved characteristics [4]. Monolithic integrated circuits using this system have started emerging recently, including X-band amplifiers [5] and W-band mixers [6]. A W-band monolithic oscillator using $InAlAs/In_{0.6}Ga_{0.4}As$ HEMT's has been demonstrated by the authors and showed 81 GHz oscillation with output power of -7 dBm at the chip level [7].

This work demonstates the first experimental characteristics of a monolithic HEMT doubler from 90 GHz to 180 GHz using InAlAs/InGaAs heterostructure circuits above 100 GHz.

1. Submicron ($0.1\mu m$) Gate HEMT Fabrication

A cross-section of the $InAlAs/In_{0.65}Ga_{0.35}As$ HEMT is shown in Fig. 1. The details of the design optimization were reported by the authors in the past [4]. The layers were grown by MBE as described by Hong et. al. [8]. The active device used for the monolithic doubler is a $0.1\mu m\times 90\mu m$ mushroom-gate HEMT. A mix-and-match method is employed for this purpose whereby optical lithography is used for all levels except the submicron gates which require e-beam writing. The first level is the mesa isolation which is achieved using wet chemical etching (H_3PO_4:H_2O_2:H_2O). Next an image-reversal process (Shipley 5214-e photoresist) is used to define the ohmic patterns (2 μm source-drain spacing) and Ge/Au/Ni/Ti/Au is evaporated and lifted off using PRS100 solution. The ohmic metal is then rapid thermal annealed at $375°C$ for 7s. Good electrical characteristics and surface morphology can be obtained at the same time. This allows small acess resistance to the device and facilitates e-beam writing.

To obtain the 0.1μm gate, a bi-layer electron-beam resist technology was developed. The gates were written using the JEOL JBX 5DIIF e-beam system which is equipped with 50keV e-beam energy capability. The higher electron energy allows better beam

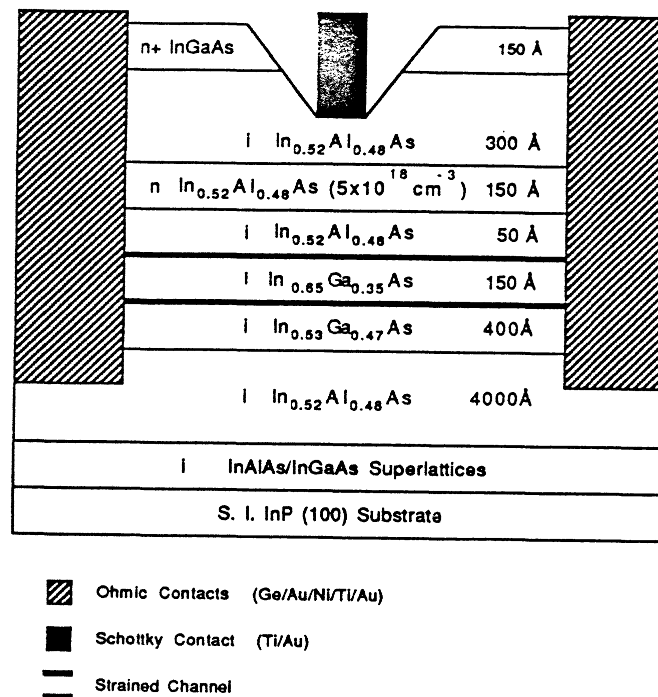

Figure 1: Device cross-section of a single-heterojunction InAlAs/$In_{0.65}Ga_{0.35}As$ HEMT

directionality which causes less back scattering in the resist during exposure and hence less broadening of the exposed area. This feature permits one to obtain a small (0.1μm) gate foot print by implementing a bi-layer resist technique rather than using a tri-layer resist technology. The advantages of the bi-layer resist technique include shorter time and fewer steps for resist preparation, excellent gate aspect ratio and higher lift-off yield for both pads and gates. 0.1μm gates are obtained with this approach in a very reproducible way and the technology lends probably itself to even shorter gate lengths.

The bi-layer resist consists of a bottom PMMA (1500Å) layer and a top P(MMA-MAA) (5500Å) layer as shown in Fig. 2. A side-lobe exposure technique is employed to obtain submicron mushroom-gate with excellent aspect ratio (4:1). This technique consists of three beam exposures. The first exposure is used to define the 0.1μm foot print. As mentioned earlier, the higher directionality of the electron-beam allows the definition of very small foot print of 0.1μm or smaller. The other two beam exposures with weaker dosage are used to obtain the top mushroom-gate profile. After exposures, the e-beam resist is developed using a MIBK:IPA solution. A SEM picture of the bi-layer resist profile is shown in Fig. 2.

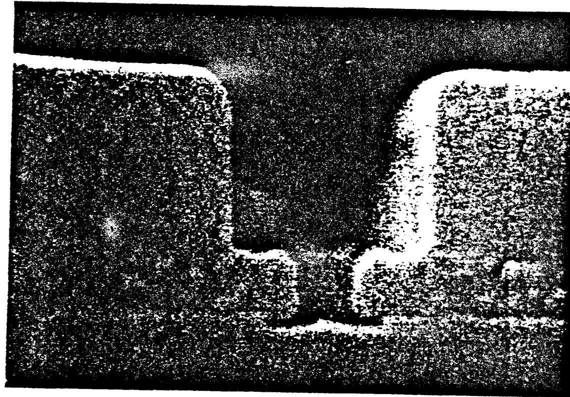

Figure 2: SEM picture of a bi-layer E-beam resist profile of the 0.1 μm mushroom gate

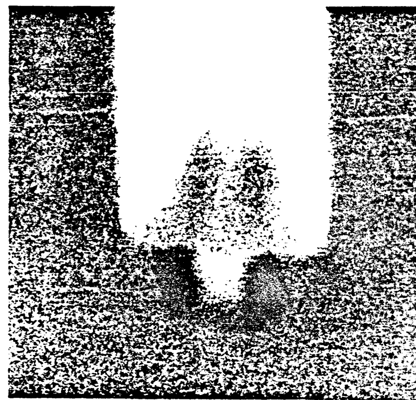

Figure 3: SEM picture of a 0.1 μm mushroom gate using bi-layer resist and side-lobe exposure technique

The next critical step after the e-beam writing is the gate recess. Before that, the wafer is descumed in an oxygen plasma to remove any resist residues in the opened areas. Next, the native oxide layer is removed using buffered HF and immediately followed by gate recess using an citric acid:H_2O_2:H_2O etchant. The gate recess is stopped when a predetermined drain-source current is reached. The wafer is then subjected to a short buffered HF etch and loaded immediately into the e-beam evaporator. Ti/Pt/Au is evporated and lifted off using acetone. After lift-off, wafers are inspected and a yield estimate is made. This is normally exceeding 90%. A complete SEM picture of a 0.1μm mushroom- gate is shown in Fig. 3.

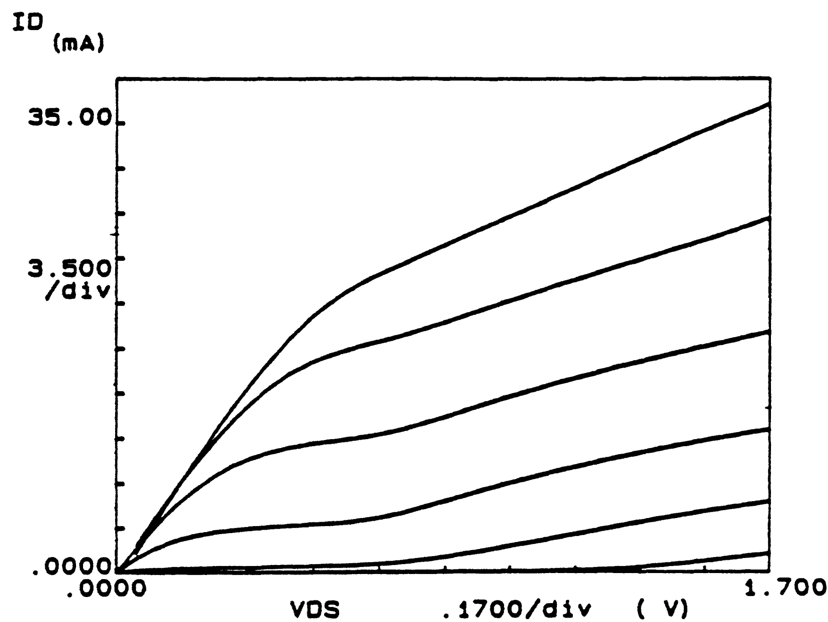

Figure 4: DC I-V characteristics of a 0.1 μm × 45 μm InAlAs/$In_{0.65}Ga_{0.35}As$ HEMT

2. DC and Microwave Characterization

Before proceeding to the next fabrication steps, the devices are tested both at DC and RF. This allows one to evaluate the suitability of the wafer for MMIC processing and monitor the degree of possible degradation when the active devices are subjected to the subsequent MMIC processing steps.

Fig. 4 shows a typical I-V characteristics of a fabricated 0.1μm×45μm HEMT's. These devices exhibit good pinch-off characteristics which is important for good doubler operation. A drain-source current as high as ~820mA/mm at V_{ds}=1.7V and V_{gs}=0.4V was obtained. Fig. 5 shows the corresponding transfer characteristics of the same device. The extrinsic g_m is ~920mS/mm with an associated I_{ds} of 550mA/mm at V_{ds}=1.5V and V_{gs}=0.18V. However, these devices also give high output conductance (G_{ds}~180mS/mm) which is typical of the single-heterojunction design using this material system [9]. As a result, th gain factor g_m/G_{ds}~5 is rather low and limits the microwave power gain performance.

The devices were also characterized using on-wafer probing from 0.5GHz to 26.5GHz. Fig. 6 shows the microwave performance of a 0.1μm×90μm HEMT. A high extrinsic f_T of 180GHz was extracted for this device following a -6dB/oct slope. The maximum power gain at 26.5GHz was ~15.5dB. The estimated f_{max} for this device is also of the same

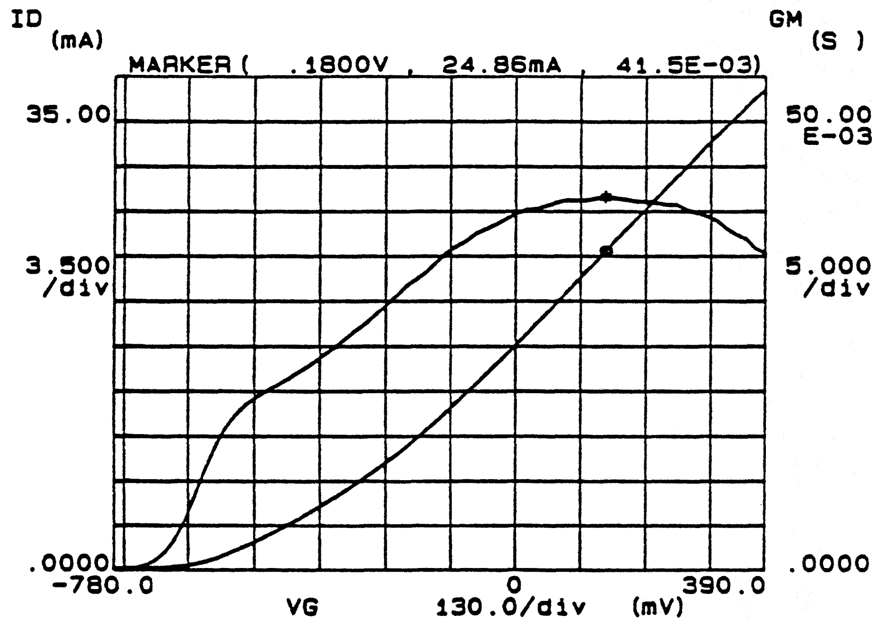

Figure 5: DC transfer characteristics (g_m-V_{gs},I_{ds}-V_{gs}) of the device corresponding to Fig. 4. Peak extrinsic g_m=920mS/mm with an associated I_{ds}=550mA/mm.

magnitude (~180GHz). Higher f_{max} values can be expected by optimizing the device structure and growth technique to suppress the high G_{ds} [9] and by improving the device technology using techniques such as double-recess gate [10].

Following the device characterization, the wafer was carried through the remaining MMIC processing steps to realize the complete doubler circuit. After the wafer has been thinned down to ~100μm and diced, the discrete HEMT's were once again being characterized. These results reflect more closely the true device performance capability since they are obtained at the end of the complete MMIC fabrication cycle. The results obtained for the doubler run reported in this paper revealed degradation in device performance. DC g_m's values on the average have dropped from 900mS/mm to 600mS/mm which corresponds to a substantial g_m decrease by 30%. Likewise, both f_T and f_{max} have decreased to ~ 130GHz. Similar degradation have also been observed in other wafers after processing steps involving heat treatment. Preliminary studies indicate that this may be related to the material and the growth conditions. A more detailed study of this phenomenal will be reported elsewhere [11].

The bias-dependent extrinsic f_T characteristics of the 0.1μm×90μm HEMT are shown in Fig. 7. The f_T's increase with V_{ds} under all gate bias conditions. The best f_T for this

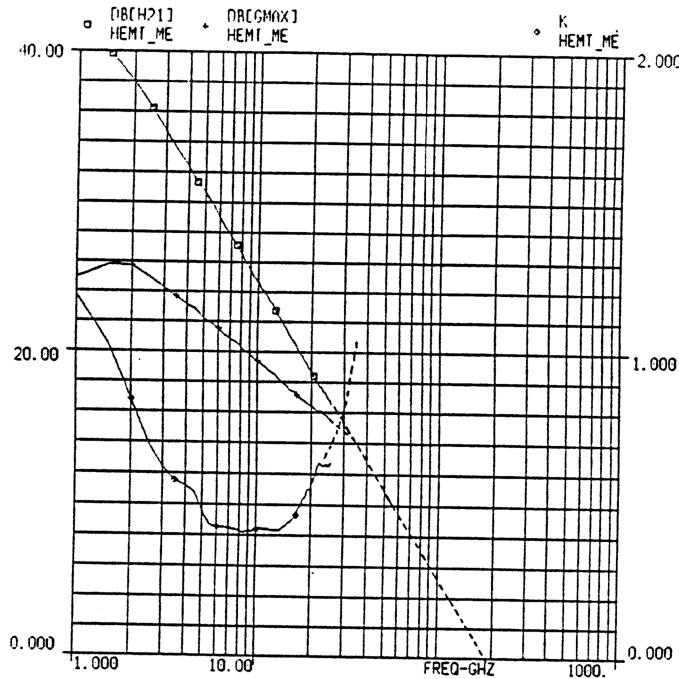

Figure 6: Microwave characteristics of a 0.1 μm × 45 μm InAlAs/$In_{0.65}Ga_{0.35}As$ HEMT right after active device fabrication. The maximum extrinsic f_T and f_{max} are approximately 180 GHz.

device is ~130GHz at V_{ds}=1.5V and V_{gs}=0V. This corresponds to a decrease of ~30% which was primarily due to the same order of magnitude degradation in the g_m of the device.

Although the device performance at the end of the MMIC processing does not demonstrate the maximum possible capability of the HEMT's, it is sufficiently good to permit the demonstration of a functional 90GHz to 180GHz doubler. This is due to the fact that the frequency of the doubler input signal is below f_T and thus the device nonlinearity can still be effective. Much better doubler performance such as lower conversion loss can be expected if the interity of the devices can be preserved throughout the processing steps.

3. Passive MMIC Component Fabrication

Following the active devices, the passive MMIC components are fabricated. These include biasing and matching capacitors, interconnect metals for microstrip stubs and bonding pads, and air-bridges.

To realize the capacitors, a sputtered lift-off technique is used which allows selective deposition of the SiO_2 without any influence on the active device characteristics. The

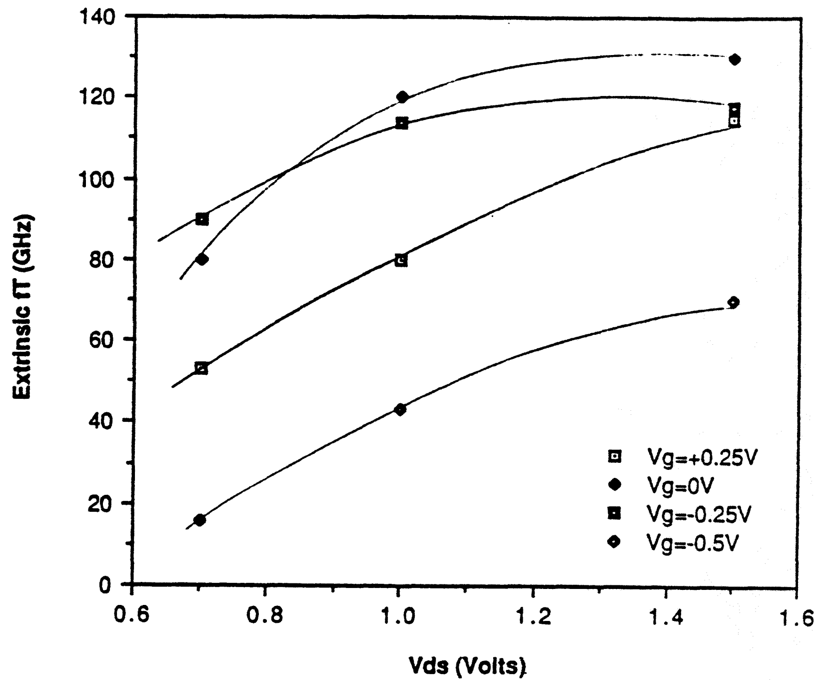

Figure 7: Bias-dependent microwave characteristics of a 0.1 μm × 90 μm HEMT after the complete MMIC fabrication cycle.

capacitor consists of the bottom plate (Ti/Au), sputtered SiO_2 as the dielectric material, and finally the top plates (Ti/Au) which also serve as the interconnect metal. All these levels are defined using optical lithography and a chlorobenzene lift-off technique.

Next, air-bridges are fabricated in a two-step process. First, the pillars of the air-bridges are defined and the entire wafer is sputtered with Ti and Au to form the pillars and also to serve as the conductive path for the subsequent electroplating. Next, the air-bridges are opened up and followed by electroplating of thick Au layer. The photoresists are then removed and the thin sputtered Ti and Au layers are etched away using buffered HF and TFA gold etchant respectivley. The integrity of the air-bridges is excellent as confimed by their stability after wafer thinning ($\sim$100μm) and dicing. The latter are the final two steps of the complete MMIC fabrication cycle used for the reported doubler. Finally, the individual chips are mounted and bonded in a specially designed text fixture for 180GHz testing.

4. 90 to 180 GHz Doubler Circuit Design

FET frequency doublers can operate in two typical bias conditions - one corresponds to a gate-source voltage (V_{gs}) near pinch-off (V_p) (class B) and the other requires an almost near V_{gs} = 0 V condition. The transconductance is used as a major source of

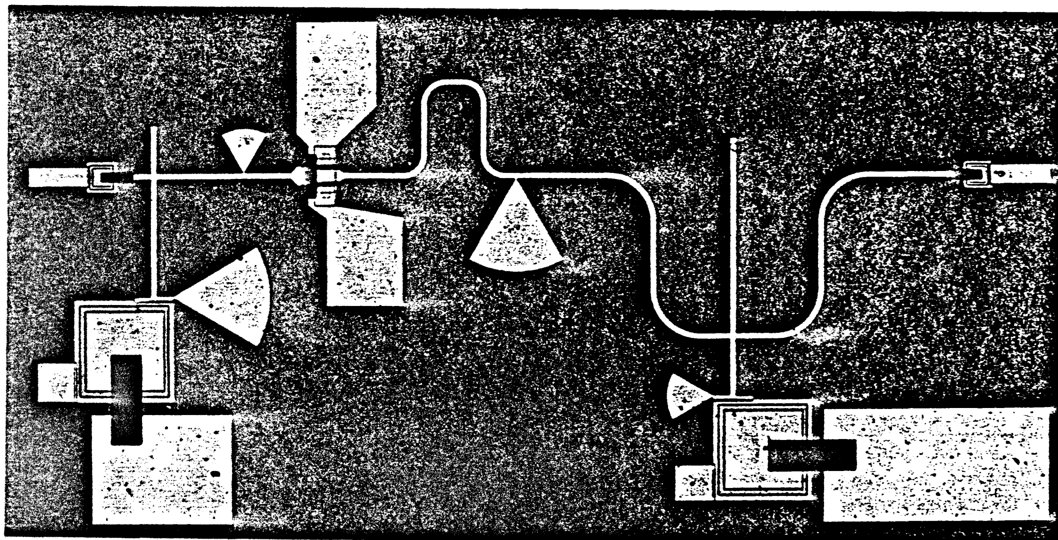

Figure 8: Photograph of a monolithic integrated doubler using InAlAs/InGaAs HEMT

nonlinearity in class B operation. For an operation with $V_{gs} = 0$, the output conductance is the predominant device nonlinearity necessary for harmonic generation. There is no major difference in conversion efficiency between these two cases for low frequency operation because both can provide efficient drain current clipping which is the main source of second-harmonic generation. However, the RF leakage current which is represented by the displacement current in the gate-source capacitance (C_{gs}) for high frequency operation prohibits the ideally expected square-wave-like waveform generation and thus degrades the efficiency significantly. Even if the device provides greater transconductance at $V_{gs} = 0$, it is advisable to use the $V_{gs} = V_p$ bias condition for high frequency multiplication to minimize the RF leakage current. This design philosophy was applied to the 90 to 180 GHz doubler reported in this paper.

A photograph of the fabricated chip is shown in Fig. 8. Right next to the HEMT one distinguishes two radial stubs used to realize bandreject filter characteristics. The left stub acts as a 180 GHz resonator prohibiting the doubled signal from leaking towards the input, while the right one functions as a 90 GHz resonator cutting off the fundamental 90 GHz from the output terminal. The radial stubs have 10 % bandwidth and a maximum rejection of more than 25 dB. These filters also serve as means to isolate the input and output ports. The bandreject filters are placed so as to provide proper reactive termination at the FET for the fundamental and doubled frequencies. Gate bias is

achieved through an overlay capacitor connected to the 90 GHz radial stub. This is quarter-wavelength transformed to yield perfect open conditions at the input line. The drain bias decoupling circuit is realized in a similar fashion. The matching networks at the input and output of the circuit are realized using narrow 90 Ω open-ended stubs and tuning capacitors.

In order to determine the large signal matching impedances and simulate the nonlinear operation of the HEMT doubler, a special nonlinear transistor modeling procedure has been developed and combined with harmonic balance analysis routine. The method allows the exact reproduction of experimental microwave data over the bias range of interest even with limited number of measurements. For the actual circuit simulation, the whole circuit was driven with a variable power source and the output power was evaluated at a 50 Ω load connected to the output port of the doubler circuit.

The conversion loss dependence on the gate bias was also studied. The time-domain characteristics of the output drain voltage after clipping resemble a truncated sinusoidal function. The DC gate bias determines the time duration over which the transistor is conductive (duty ratio). When $V_{gs} = V_p$, the duty ratio is 50 % and optimum conversion efficiency is expected theoretically. This is not, however, true in practice, due to the high frequency displacement current which leaks through C_{gs} and contributes to a parasitic signal. For this reason, the optimum gate bias condition is found to be slightly more positive than the pinch-off voltage.

The theoretical conversion loss vs. input power level obtained from the nonlinear analysis is shown in Fig. 9. For increased power levels, the conversion loss is seen to reduce and subsequently increase. The first reduction of conversion loss can be explained by a more efficient pumping with increased input power which results in a larger effective nonlinear transconductance swing. The deterioration of conversion loss with excess input power is attributed to the reduction of transconductance with increased power level in HEMT's due to parasitic "MESFET"-type operation. The theoretically estimated minimum conversion loss is of the order of 7.2 dB with 2 dBm LO power level using an InAlAs/InGaAs HEMT with f_T of 135 GHZ.

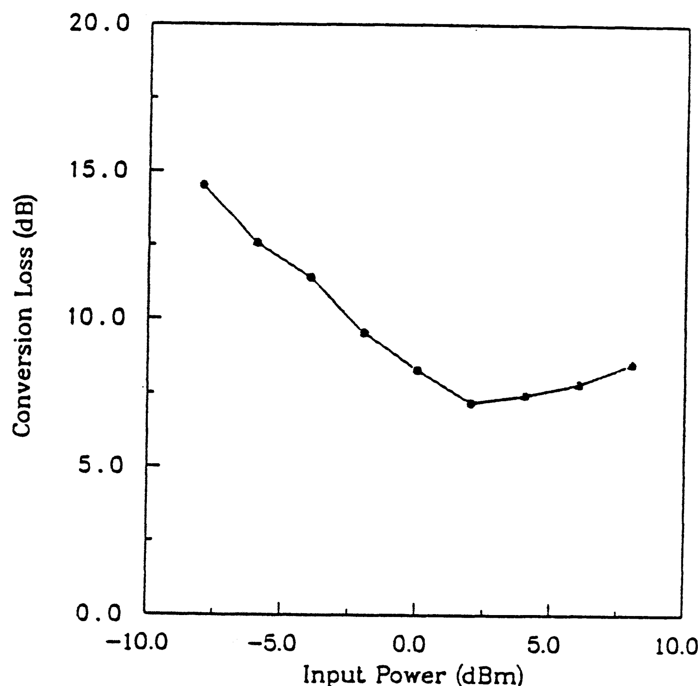

Figure 9: Theoretical conversion loss versus input power for HEMT doubler

5. High Frequency Doubler Tests and Results

Since the goal of this project is to produce working doublers, characterization is needed to verify the doubler design. Initially, the goal of characterization was to see conversion of 90 GHz to 180 GHz, i.e. a go - no go test. Thus, the test fixture design philosophy was to produce a fixture that could be designed and constructed with minimal effort, while promoting easy device mounting and reasonable testing repeatability. Doubler performance was evaluated in terms of conversion loss vs. RF drive level at 180 GHz output.

5.1 Test Fixture Design

The test fixture used to house the doubler needed to provide: a 90 GHz WR-10 waveguide input; a 180 GHz WR-3 waveguide output; two dc supply lines for drain and gate bias; and a smooth supportive surface to mount the doubler chip. The overall dimensions of the doubler test fixture were chosen to minimize waveguide lengths, yet provide adequate room for waveguide flanges, screws and other hardware (See Figure 10.). A finline to microstrip transition was selected for the WR-10 port. Theoretically, finline transitions are more lossy than probe transitions. However, finline transitions have the advantage of lower sensitivity to dimensional variations than probes [12].

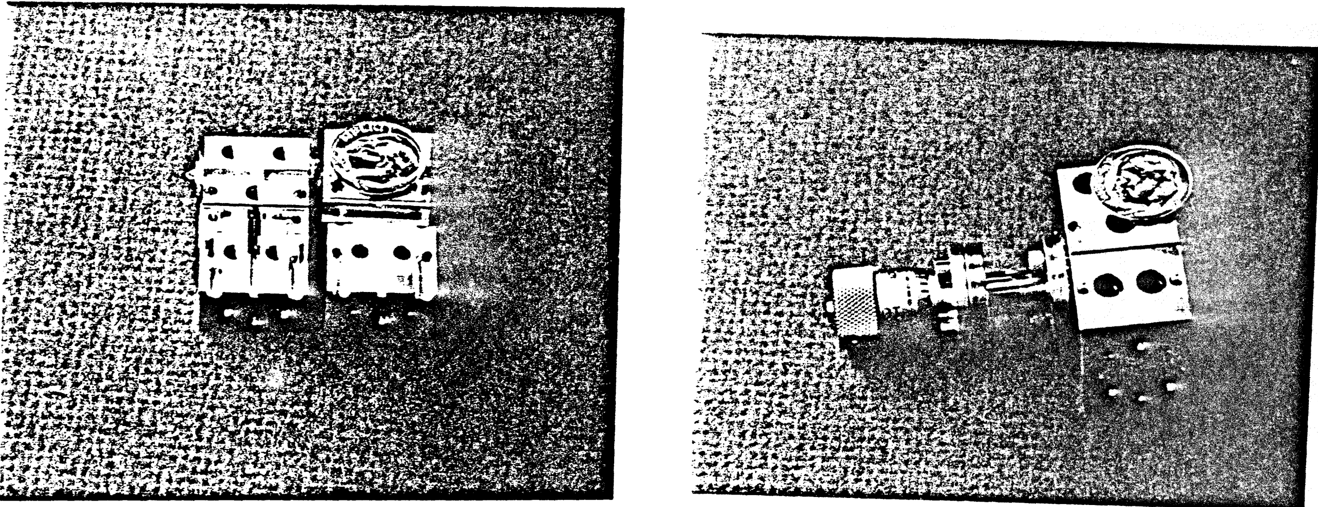

Figure 10: Photograph of the doubler test fixture

At the 180 GHz (WR-3) port, it was necessary to regress to the use of a microstrip probe transition because the minimum feasible finline transition substrate thickness of 5 mils was an appreciable fraction of the waveguide dimensions. It was expected that the addition of a WR-3 variable backshort would provide 180 GHz tuneability to offset design uncertainties in the probe. Since the microstrip probe lies in the center of the WR-3 guide, the variable backshort may be mounted on either of the two WR-3 ports. The actual WR-3 microstrip probe was realized using a microstrip realized on a 100 micron thick GaAs substrate free of backside metalization.

The 90 GHz WR-10 transition was realized using a waveguide to finline to microstrip transition (hereafter called a finline transition) on 5 mil thick fused quartz. Low dielectric constant, low losses. and a firm substrate that allows wirebonding make quartz the material of choice for this application. The transition itself is about one guide wavelength long near 94 GHz. In order to prevent evanescent waveguide modes from coupling past the transition. the quartz microstrip was made about one guide wavelength long at 94 GHz.

The finline transition is designed to present a smooth, gradual change from the waveguide TE01 mode configuration to a microstrip mode. First, the traveling waveguide E-field encounters the finline substrate. Provided that the product of the finline thickness and one minus the dielectric constant is small, the waveguide E-field sees little reflection here and proceeds to become concentrated within the substrate, between the finline edges.

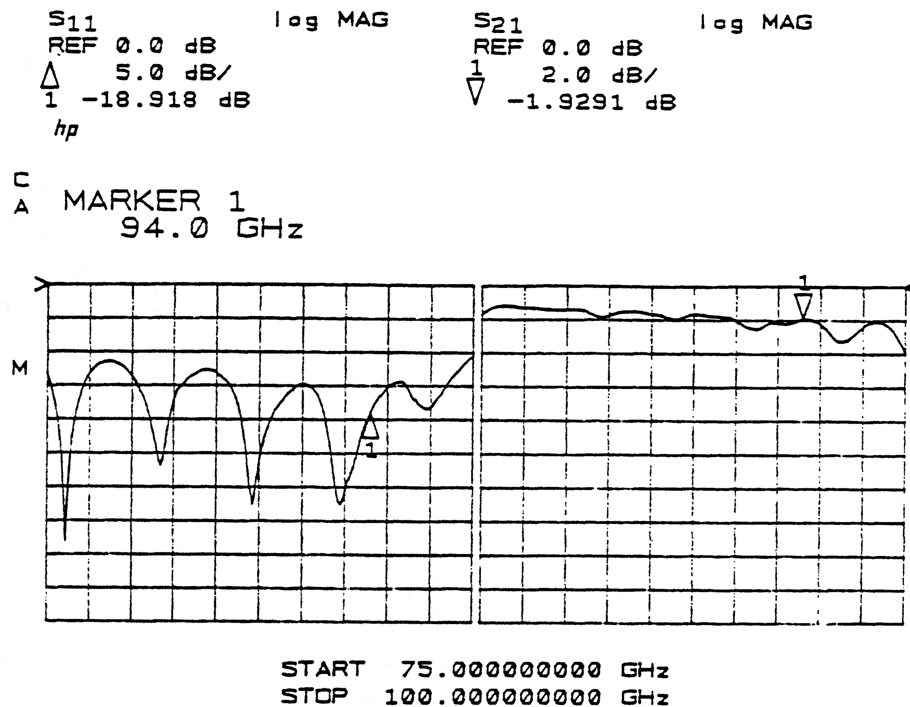

Figure 11: Double-ended finline W-band performance

From here, the antipodal finlines gradually overlap, causing the E-field to rotate towards 90 degrees as it propagates toward the microstrip. Eventually, the finline becomes a microstrip, thus carrying the E-field in a microstrip mode. In the section of the transition containing the microstrip, the backside metalization of the microstrip forms a waveguide below cutoff, thus insuring the that only the microstrip mode survives the transition.

The WR-3 microstrip probe was designed to couple to the TE01 mode of the WR-3 waveguide. In a lossless circuit, the backshort is capable of adjusting the reactance of the probe.

5.2 Test Fixture Characterization

In order to obtain reasonable measurement accuracy, it was necessary to characterize the performance of both the 90 GHz finline and 180 GHz probe transitions. Test results show that the finline - GaAs microstrip - finline has a loss of about 4.8 dB total with reflection below -30dBm at 90 GHz. This meant that the 90 GHz finline transition and bondwire in the doubler test fixture was estimated to have a 90 GHz loss of $4.8/2 = 2.4$ dB.

Next, it was necessary to characterize the doubler test fixture's 180 GHz probe transition. First, 180 GHz characteristics of the doubler test fixture's finline transition

were estimated from 180 GHz loss measurements taken on the finline - GaAs microstrip - finline configuration discussed above. This resulted in a 10 dB loss at 180 GHz. Thus, the doubler test fixture's finline loss was estimated to be 5dB at 180 GHz. To complete the characterization of the doubler test fixture's 180 GHz probe transition, a 1mm long GaAs microstrip section was installed to bridge the finline to the 180 GHz probe. Total insertion loss was about 15.5 dB at 180 GHz . Subtracting the finline loss from the measured total loss placed the doubler test fixture's 180 GHz probe transition loss at about 10.5 dB. The test results reflect the performance of test fixture of our first iteration design.

5.3 Doubler Test Procedure

Figure 12 illustrates the test setup used for the doubler characterization. One KHz square wave modulation was provided to the 90 GHz Gunn source and lock-in amplifier. The 90 GHz RF drive level was monitored using the 10 dB coupler and power meter and regulated by the continuously variable attenuator. A diode detector in conjunction with a lock in amplifier provided sensitive, detection of 180 GHz. Synchonous detection of the weak square wave output of the diode detector enables the lock-in amplifier to reduce the noise floor of these measurements. Because the diode detector exhibits broadband performance, it was necessary to eliminate the pickup of the 90 GHz fundamental. A one inch section of WR-3 waveguide provided a very effective high pass filter. To demonstrate that the detected signals were arising exclusively from the multiplying action of the doubler, the output from the 90 GHz isolator was connected through a one inch section of WR-3 waveguide to the diode detector. Under these conditions, the diode detector registered only a weak signal, about 40dB below that typical of the doubler output. Of course, with these results, one could not rule out the possibility that the doubler produced significant power at higher harmonics. However, theoretical calculations lead one to believe that the second harmonic is dominant.

5.4 90 to 180 GHz High Frequency Results

The behavior of the HEMT doubler showed some interesting features. Conversion loss was minimized at V_{ds} = 1V, I_{ds} = 5.1 mA (no input signal) and V_{gs} = -0.2 V. (The pinch-off voltage for the device tested was -0.25 V.) As expected from the simulation, the best conversion loss occurred just above pinch-off. Test results given here reflect doubler performance for the optimum bias conditions, namely those given above. Conversion loss

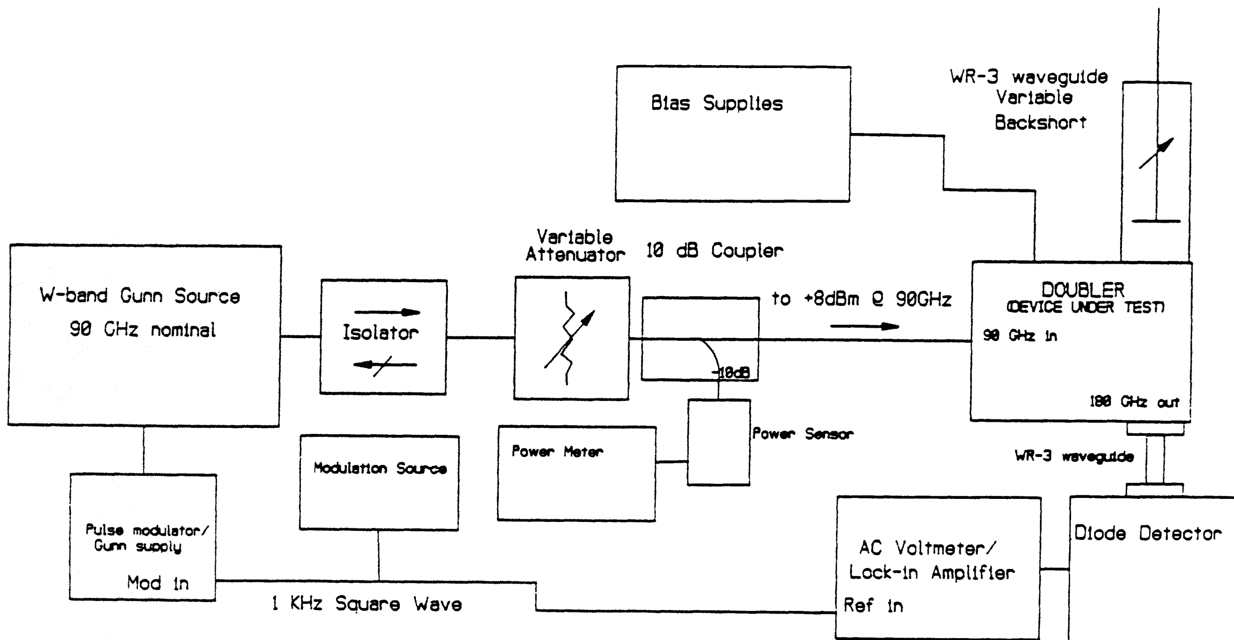

Figure 12: Doubler test setup

was found to be minimum at 0 dBm input power drive, which was close to the theoretical predictions. Over the input power range of our test (-10 dBm to 8 dBm), the conversion loss varied from 6 dB to 10 dB. This is not far off the result obtained by using hybrid diode doublers at 200 GHz. It should finally be noted that the small amount of input drive level necessary for minimum conversion loss is compatible with the limited amount of LO power available at millimeter-wave frequencies and makes the doubler compatible with other HEMT MMIC components such as, for example, oscillators [7].

Conclusion

At frequencies well above 100 GHz, and using MMIC technology, any measurable value of conversion would have been an encouraging step. The performance levels achieved (6 dB to 10 dB conversion loss for doubling from 90 to 180 GHz) was very satisfactory and even exceeded expectations. One should notice that this performance was obtained without the benefit of via hole technology. Future plans call for the implementation of via holes and further optimization of the HEMT output conductance, f_T, and f_{max} using advanced gate technologies such as offset T-gate and double recess. Eventually, these doublers will be coupled with the author's demonstrated W-Band MMIC oscillators [7] to generate milliwatt levels at 180 GHz and beyond from MMIC technology.

Acknowledgments

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