Nb BASED MIXER ELEMENTS FOR MILLIMETER AND SUBMILLIMETER WAVELENGTHS

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ABSTRACT

The superconductor-insulator-superconductor (SIS) junction is the most sensitive nonlinear element for millimeter-wave heterodyne detection. We have developed a Nb/Al–Al_2O_3/Nb junction fabrication process which is compatible with the use of planar tuning circuits integrated with the junctions. Recent results have yielded a double sideband receiver noise temperature less than 50K from 205 to 240 GHz and 44K at 230 GHz.

We are also extending our Nb/Al–Al_2O_3/Nb trilayer technology to the fabrication of sub-square-micron area junctions for submillimeter wavelengths. Two fabrication techniques are at present under investigation. The first involves a modification of our *trilevel* resist junction insulation process to augment the currently used SiO_2 masking layer with a more CF_4 etch-resistant Cr layer which should extend the capabilities of this insulation process to sub-square-micron junction areas. A trilayer insulation planarization (TIP) process, which avoids the drawbacks of machine aligned and liftoff insulation techniques, is also under investigation. TIP uses an SiO_2 deposition process to planarize, and hence insulate, a previously defined sub-square-micron junction area. Progress on the modified trilevel resist and TIP techniques will be described, and the results of recent direct detection experiments at 585 GHz and 763 GHz will be presented.

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I. Introduction

Nb/Al–Al_2O_3/Nb trilayer junctions have surpassed those made by all other SIS technologies in leakage current and uniformity. They are currently the element of choice for ultra low noise millimeter wave heterodyne detection. We are investigating both Nb and NbCN superconductors in the planar and edge junction geometries for submillimeter wavelengths. In this paper we discuss the future direction of our Nb trilayer technology.

There have generally been two approaches to SIS mixers at millimeter wavelengths: (1) the use of very small area high current density junctions to minimize $\omega R_N C$ [1,2,3,4,5] and (2) the use of integrated tuning elements to tune out the junction capacitance while keeping the benefits of a larger junction capacitance [6,7,8,9,10,11]. For millimeter wavelengths, both approaches have been rather successful. At higher frequencies the use of increasingly smaller junction areas and higher J_c values may be restricted by fabrication limitations and the properties of available superconductors. For example, with $C_s = 45fF/\mu m^2$, $I_C R_N = 1.8mV$ [12], and $R_N=100\Omega$, a choice of $\omega R_N C = 1$ at 100 GHz with the Nb/Al–Al_2O_3/Nb system requires a junction area of approximately 0.35 μm^2 and a $J_c = 5.1 \times 10^3$ A/cm^2. Even if we ignore the $J_c \propto f^2$ relationship found by Kerr and Pan for $\omega R_N C= 4$[10], at 600 GHz and 1 THz the desired junction areas and J_c values would still be 0.06 μm^2 and 3×10^4 A/cm^2, and 0.035 μm^2 and 5×10^4 A/cm^2 respectively. These numbers, particularly the J_c values, are certainly optimistic estimates. The fabrication of such planar trilayer junctions having reasonable electrical characteristics may be difficult, making the use of integrated tuning elements, which permit the use of larger junction areas and smaller J_c values, more attractive. Additionally, the expected difficulty in suppressing Josephson currents (and the resulting Josephson noise) for very small junction areas argues for the choice of junctions with the largest area. However,

resistive loss in superconductor films at frequencies approaching $2\Delta/h$ ($\simeq$ 700 GHz for Nb) will prevent the use of superconductive tuning elements above these frequencies, and normal metal tuning elements [9] or alternative mixer designs will need to be developed.

Superconductor-Insulator-Normal (SIN) junctions are also attractive at high frequencies. Although the nonlinearity of the SIN junction is weaker than that of an SIS junction, and the theoretical upper frequency limit ($2\Delta/h$) is half that of an SIS mixer[13], the SIN junction has no pair currents and is thus free of Josephson noise. This advantage could be extremely important, as Josephson noise may severely limit the high frequency performance of SIS mixers.

II. Millimeter Wavelength Device Research

A. SIS Elements with Integrated Tuning Elements

In our earlier work [9,14], we reported utilizing a trilevel resist to pattern junction areas in Nb/Al–Al_2O_3/Nb films. After reactive ion etching to define the junction area, the perimeter of the junction is revealed and a liftoff structure is defined with an oxygen plasma shrink of the exposed polyimide sidewalls. A subsequently deposited insulation layer seals the sides and the perimeter of the Nb counter electrode button (Fig. 1). The excellent liftoff profile that is obtained with this technique allows the use of thick insulation layers. An off-axis SiO insulation deposition with wafer rotation results in good step coverage and a nonabrupt surface for the subsequent Nb wiring layer (Fig. 2). We have repeatably utilized this technique to fabricate high-quality junctions of 1.5 μm diameter and current density as large as 1 x 10^4 A/cm^2.

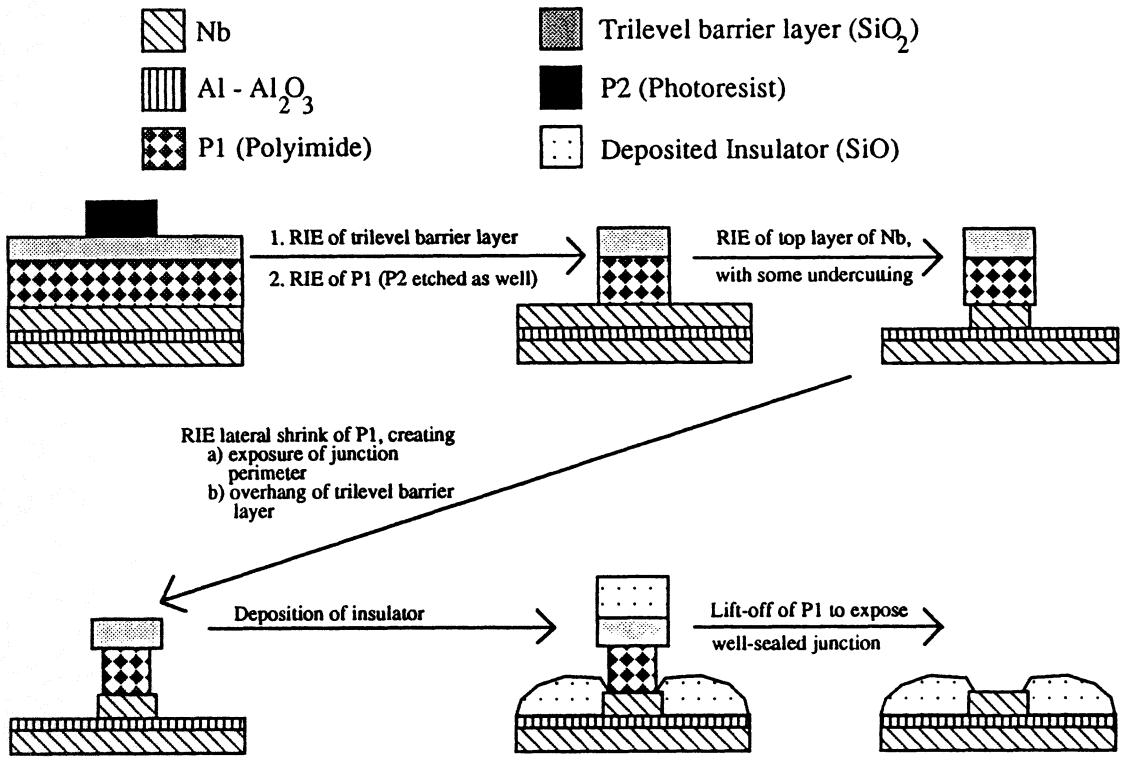

Figure 1. Outline of the trilevel resist insulation process.

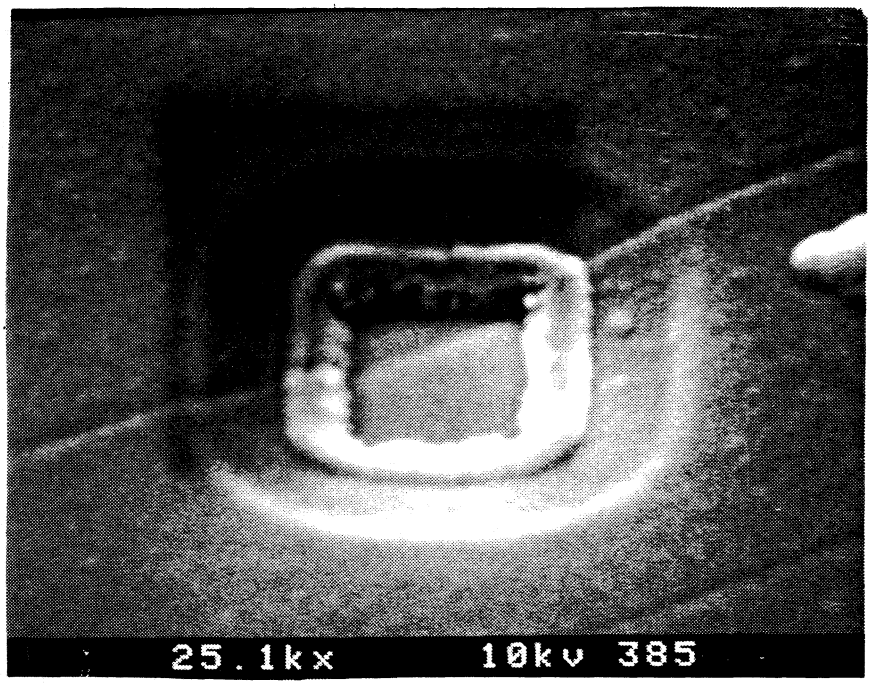

Figure 2. SEM view of an Nb junction area insulated with SiO. Due to the shadowing effect of the trilevel resist, the SiO deposition results in a gradual profile as the SiO reaches the Nb button.

For SIS mixers, the use of relatively large area junctions with relativity large $\omega R_N C$ has two advantages: (i) The large capacitance tends to short-circuit currents at the LO harmonics and harmonic sidebands, and (ii) Undesired effects of the AC Josephson currents in the junction are reduced. For good mixer performance it is necessary to tune out the junction capacitance at the signal frequency. To do this, we have used inductive tuning circuits integrated with the individual junctions [9,12,14]. The most recent results at 230 GHz are shown in Figure 3. An NRAO receiver [15] using these junctions has a DSB noise temperature (T_R) of 44K at 230 GHz, and a T_R below 50K from 205 GHz to 240 GHz. These figures are believed to be the lowest reported for a receiver operating over this frequency range.

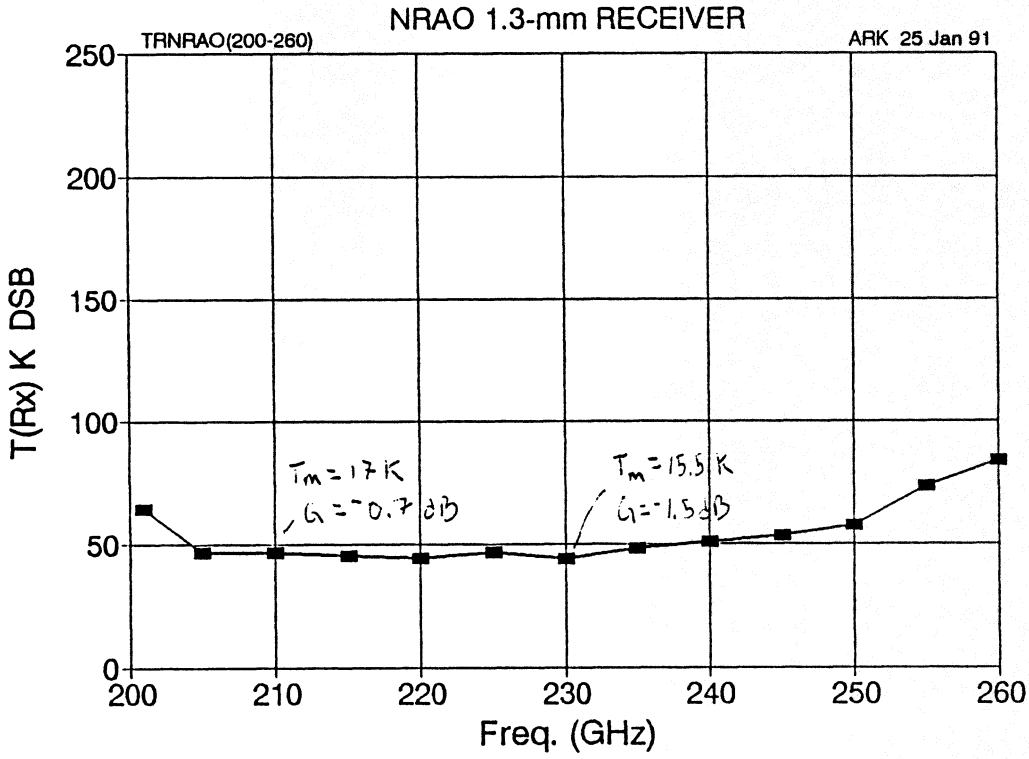

Figure 3. Noise temperature measurements from 205 GHz to 260 GHz for a NRAO receiver incorporating Nb/Al–Al_2O_3/Nb junctions fabricated at the University of Virginia [15]. The DSB mixer noise temperature at 230 was 44K.

III. Submillimeter Wavelength Device Research

A. Cr/SiO_2 Quadlevel Resist Insulation

The optimal performance of SIS mixers requires that the junction area be decreased as the frequency of operation increases. Consequently, we have attempted to apply our existing trilevel resist process to the fabrication of sub-square-micron area junctions. These efforts have now convinced us that repeatability in etching limits our present trilevel process to the fabrication of junctions with an area of $\approx 1\mu m^2$. The limitation arises from an unfortunate characteristic of the SiO_2 masking layer: the trilevel SiO_2 etches rapidly in low-pressure CF_4 based etches which are otherwise well-suited for defining the counter electrodes of our junctions. Because the SiO_2 masking layer must remain intact during the Nb counter electrode etch, it is necessary to perform this etch at a significantly higher pressure (300 mTorr) in order to minimize etching of the SiO_2. However, the higher pressure appreciably increases lateral etching, or "undercutting," of the Nb counter electrode; this is especially true for small features. In the case of submicron junctions, the undercutting either etches the feature away entirely or leaves an area so small that the subsequent shrink of the polyimide layer to expose the counter electrode perimeter can not be repeatably performed (Fig. 4).

Recently, we have developed what we believe to be a viable solution to this problem. The new approach involves the addition of a 1000 Å Cr layer sputtered on top of the 1500 Å SiO_2 layer to form a *quadlevel* structure (Fig. 5). The Cr layer's resistance to etching in a low-pressure CF_4+O_2 plasma allows it to protect the quadlevel structure; as a result, the Nb counter electrode layer may be etched with little or no undercutting. A vertical etch of the Nb is desirable because it reduces the required amount of shrinkage of the polyimide features in the next step of the process; it will only be necessary to perform the O_2 plasma shrink long enough

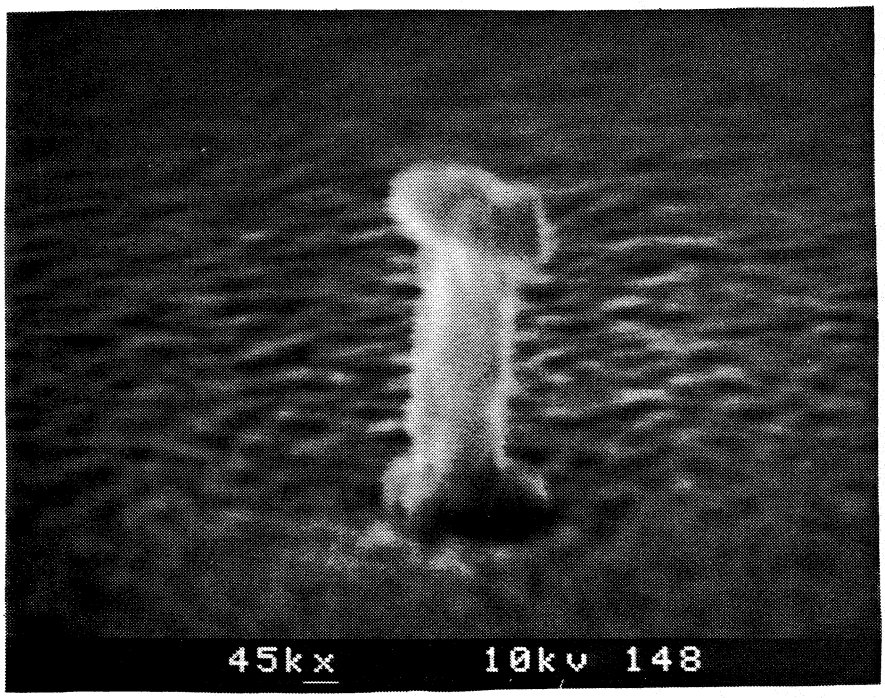

Figure 4. An SEM micrograph of a 0.3 μm x 0.3 μm Nb junction area for which a successful SiO_2 based trilevel resist feature was obtained. The shrinkage from the mask feature size of 0.8 μm x 0.8 μm is primarily due to the "undercutting" of the Nb film in the high pressure $CF_4 + O_2$ etch. A lateral shrinkage of 0.25 μm < x_{shrink} < 0.35 μm was therefore required for this successful polyimide shrink step. This step is performed, however, without quantitative information on the extent of the Nb undercutting, resulting in poor repeatability.

to create an adequate liftoff profile. A relatively thin Cr layer is desired to avoid undercutting from the wet etch used to define it. The SiO_2 layer is still required so that the SiO_2 and Cr together will form a masking layer thick enough to serve as the top layer of liftoff features. Initial tests of the quadlevel technique have resulted in Nb counter electrode buttons which are actually slightly *larger* than the defining quadlevel resist structure. We have also determined that the polyimide shrink step can be performed *prior* to the Nb counter electrode etch without any apparent effect on the subsequent Nb etch (Fig. 6). The anisotropic Nb etch results in a counter electrode circumference size which is controlled by the Cr/SiO_2 mask and not the pre-

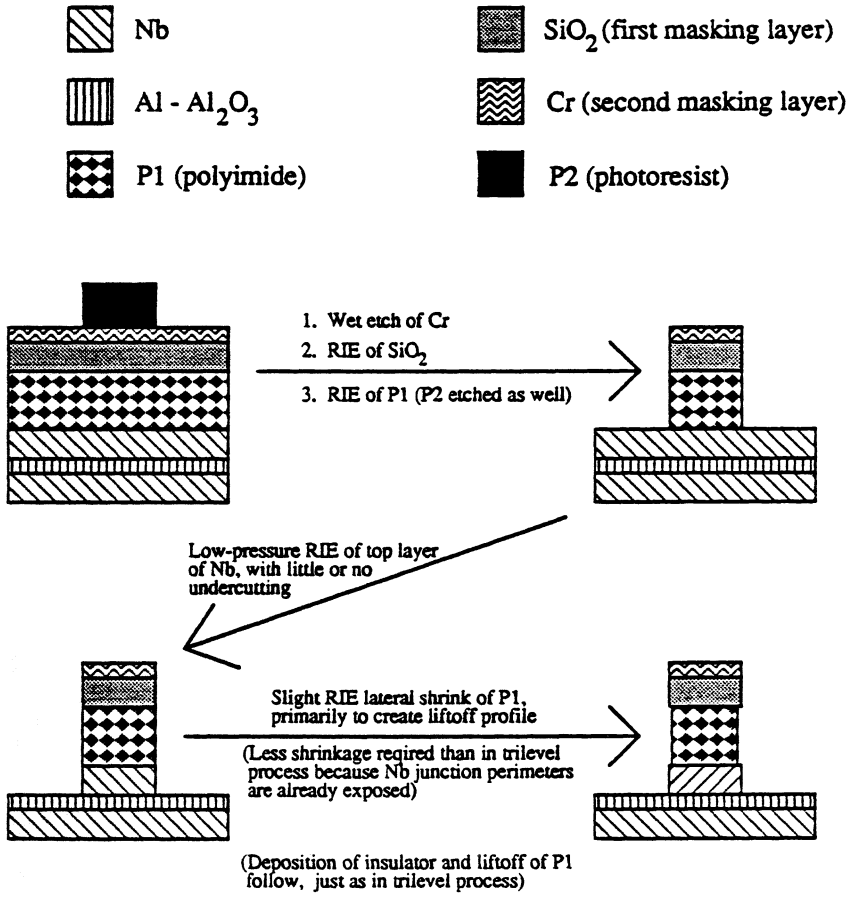

Figure 5. Outline of the quadlevel resist insulation process.

shrunk polyimide perimeter. Performing the polyimide shrink prior to the junction definition results in a more uniform and controlled shrink process since difficulties in polyimide shrinkage due to PRIST hardening [9] from the Nb etch are not encountered. It is expected that with the use of a new sub-micron feature mask, we will be able to accurately and repeatably fabricate sub-square-micron junction areas. We will also investigate the use of Cl based RIE chemistry for Al etch mask definition to replace the Cr/SiO_2 bilayer. The resulting Al based trilevel resist would have fewer steps and avoid the wet etch of the Cr based quadlevel technique.

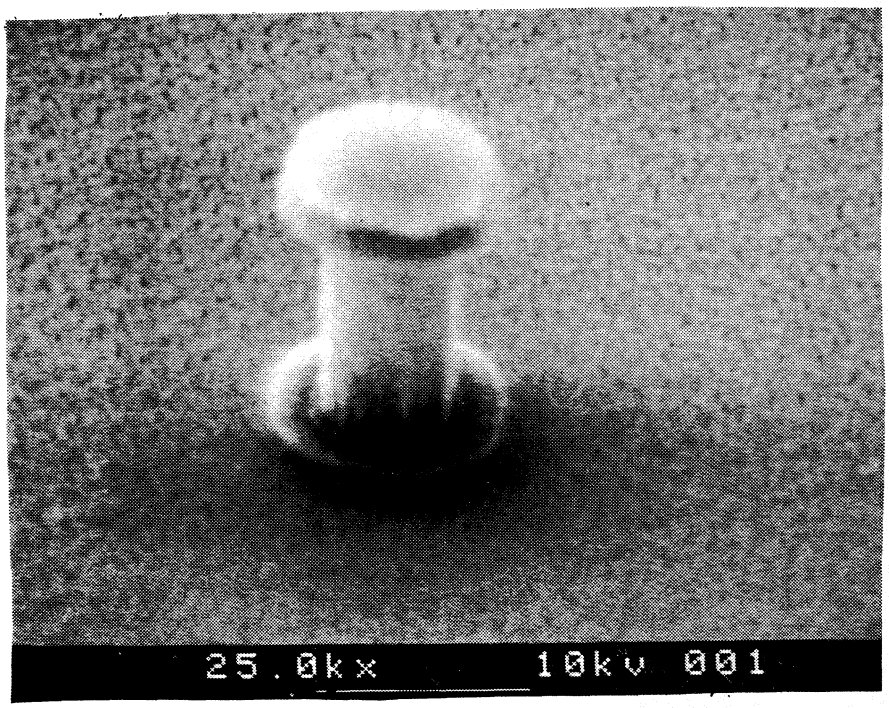

Figure 6. An SEM micrograph of a quadlevel resist defined Nb counter electrode. The excellent liftoff profile has been obtained with a pre-shrink of the polyimide prior to definition of the junction area. The subsequent SiO_2 deposition should easily insulate the junction area. Note that the perimeter of the counter electrode is slightly larger than the defining Cr/SiO_2 mask. By adjusting the RIE parameters, we should be able to control the size of the junction circumference, making it larger or smaller than the defining Cr/SiO_2 mask.

B. Trilayer Insulation Planarization

Although the use of self-aligned liftoff insulation techniques is common [12, 16-22], there is an intrinsic drawback in the use of the defining film as both an etch mask for junction definition and as a liftoff structure for junction insulation. If moderately thick base electrode and insulation layers are desired (e.g., for some tuning element designs), then a relatively thick liftoff structure with an overhang is required for a successful liftoff. Such structures may become unstable and difficult to define for sub-half-micron feature sizes.

We have been investigating an alternative trilayer insulation planarization (TIP) process [23] which avoids the difficulties of self-aligned liftoff techniques (Fig. 7). The basic idea of this process is to separate the junction definition from the junction insulation step while *not* requiring a machine-aligned or self-aligned liftoff process. Following RIE definition of the junction, the entire wafer is covered conformally with an insulator. The wafer is then planarized with an aggressive rf bias sputter deposition. The planarization is based on the dependency of sputter etching rate on angle. While a near zero deposition rate is occurring on the planar regions of the wafer, the edges of the surface features will be rapidly etched. A subsequent etchback of the planarized insulation layer, which reveals the Nb junction area, can be monitored with a surface profiler. The desired end result of the TIP process is an insulation layer which seals the edges of the junction and presents a planarized surface for the subsequent Nb wiring. This insulation technique should properly seal any size junction area, limited only by the ability to define submicron Nb features with lithography and RIE. The TIP process is also compatible with the incorporation of integrated tuning elements, permitting the use of a wide range of insulator thicknesses.

Our experiments with the TIP process have utilized a rf diode sputtering system for insulator planarization. It was initially determined that a light bias deposition was necessary in order to obtain good conformal coverage by the initial insulation layer. Excellent planarization was then obtained after 4 hours of more aggressive bias deposition at the following conditions: 5 μm Ar pressure, 3.9 W/cm^2 and 1900 Volts on the target electrode, and 0.38 W/cm^2 and 180 Volts on the substrate electrode. Uniform planarization was only obtained when the wafers were not heat-sunk to the H_2O cooled substrate platter.

Outline of TIP Process

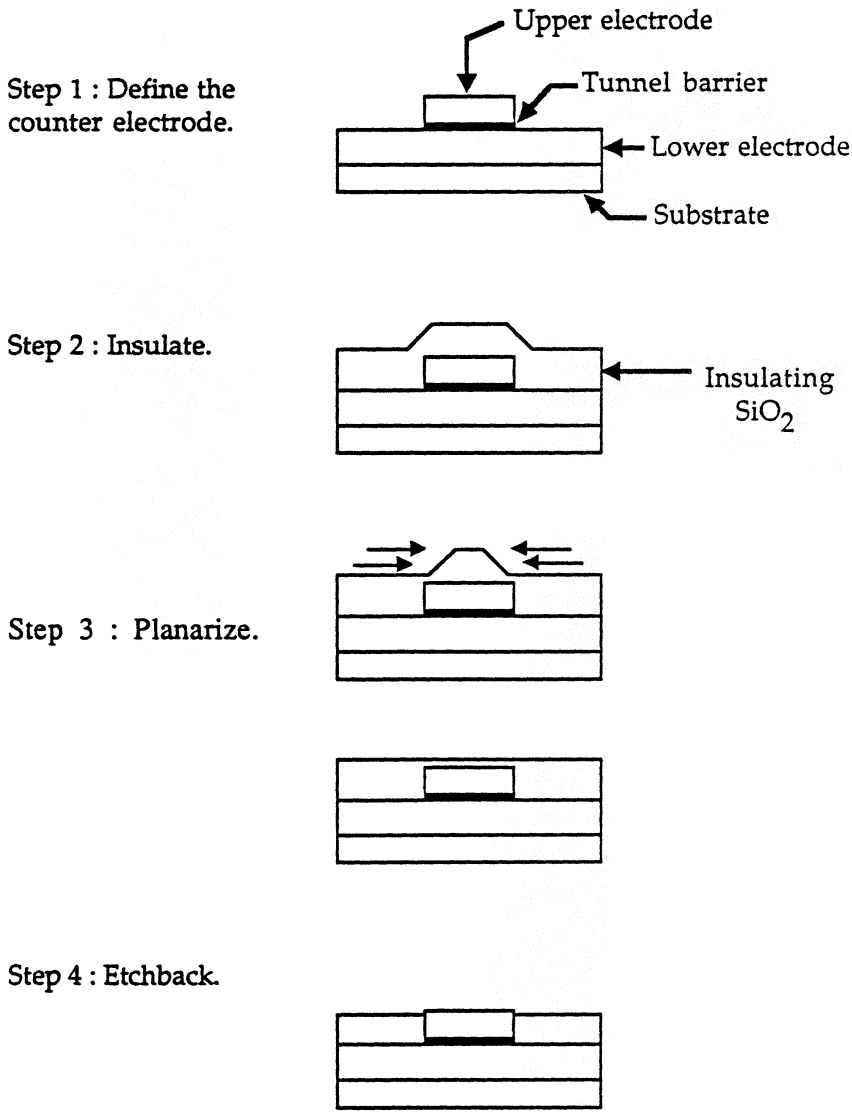

Figure 7. The trilayer insulation planarization TIP process

A CF_4 RIE etchback technique was initially investigated (under conditions similar to our trilevel SiO_2 etch), yet the planarized films had an extremely small etch rate (<10 Å/min). It was suspected that these low rates were due to film contamination from the chamber during the high power planarization process. Instead, a buffered hydrofluoric etch (BOE) was used successfully to thin the planarized SiO_2 film until the conformal SiO_2 layer was revealed. The CF_4 etchback technique was then utilized until the Nb counter electrode junction button was revealed (Fig. 8). The use of BOE for the entire etchback step resulted in a poor interface between the SiO_2 and the sidewalls of the Nb counter electrode (Fig. 9).

We are encouraged by these results; however, due to the lack of wafer cooling during the planarization process, the wafers are subjected to high temperatures, resulting in severe damage

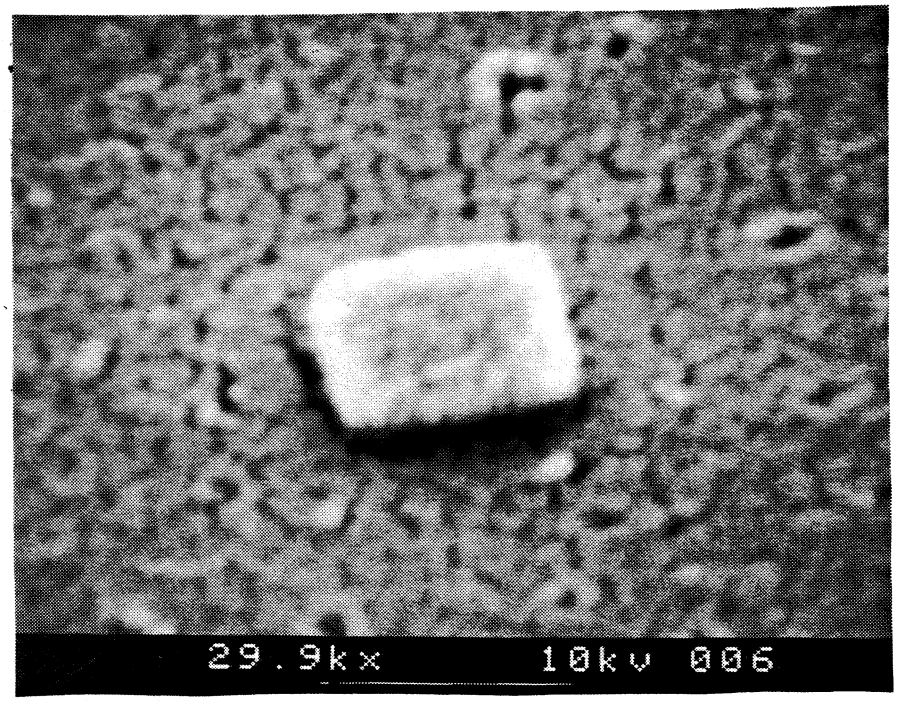

Figure 8. An SEM micrograph of a Nb counter electrode button insulated by the TIP process

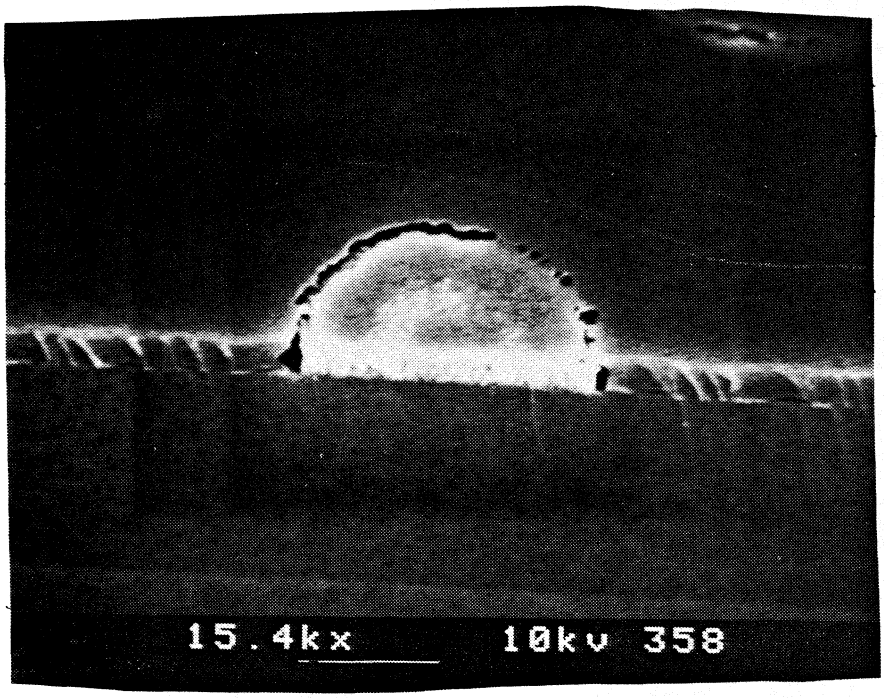

Figure 9. Trenches around the Nb counter electrode after a BOE etchback step.

to the Al_2O_3 trilayer tunnel barrier. An alternative insulator deposition technique for planarization which we are investigating is electron-cyclotron-resonance-chemical-vapor-deposition (ECR-CVD). Such systems are reportedly capable of rapid and uniform planarization of sub-micron features at low temperatures[24].

C. Nb/Al(thick)–Al_2O_3/Nb SNIS Elements

As the frequency of operation of an SIS mixer is increased into the submillimeter wavelength range, Josephson noise becomes a significant concern. However, because Josephson currents occur only between two superconductors, junctions consisting of an SIN (superconductor-insulator-normal metal) structure are free of Josephson noise. Chernin and Blundell, utilizing actual SIN I-V characteristics, have theoretically predicted good receiver

noise performance for SIN fundamental and subharmonic mixers at submillimeter wavelengths[25]. We propose to fabricate planar SNIS devices with integrated tuning elements composed of Nb/Al(thick)–Al_2O_3/Nb and NbCN structures (Fig. 10). These two SIN structures have 2Δ/h cut off frequencies of 700 GHz and 1200 GHz respectively. The materials, as well as the interfaces between them, are quite similar to our present Nb/Al–Al_2O_3/Nb SIS devices.

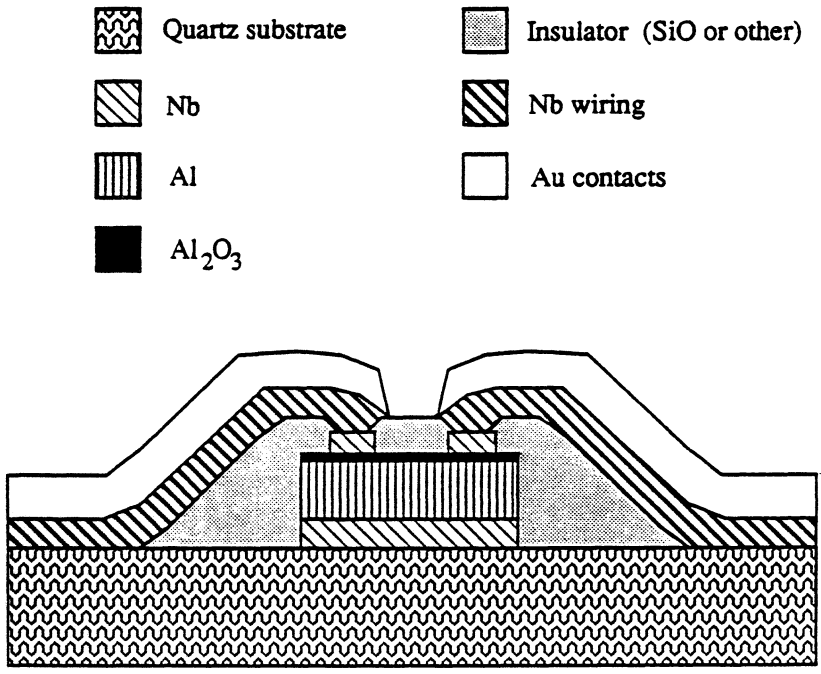

Figure 10. Cross section of Nb/Al(thick)–Al_2O_3/Nb structure

D. Direct Detection Results

The direct detector is an incoherent detector which can be utilized for continuum measurements. SIS direct detectors [26] do not require ^{3}He cooling as do the best Ge bolometers and therefore may be competitive for space applications. The theoretical response

of the dc tunneling current to radiation is given by the Tien-Gordon equation

$$I=\sum_{m=-\infty}^{m=\infty} J^2_m(\alpha)I(V_0 + mh\nu/e)$$

where $\alpha = \frac{eV_{rf}}{h\nu}$ [27]. This parameter can be used to give an estimate of the input power based on the equation

$$P=\frac{V_{rf}^2}{2R_D}$$

where R_D is the dynamic resistance [28]. The quantum limit for current responsivity (the amount of current produced by a given amount of incident radiation) is one electron per incident photon, which corresponds to a responsivity of 413 A/W at 585 GHz. Another parameter of interest is the noise equivalent power (NEP), the amount of power necessary for the signal be equal to the noise of the system. The value that we expect [26] is on the order of 10^{-15} W/$\sqrt{\text{Hz}}$, based on the leakage current of our junctions and the system bandwidth.

Nb/Al–Al_2O_3/Nb untuned junctions, described above, are used. The junctions are in series arrays of N = 2,4, and 6, and have a 90 degree integrated bow-tie antenna which is 1000 μm long. The bow-tie junction structure is placed on a copper mounting block behind a hemispherical quartz lens on an adjustable mount used to change the coupling of the radiation into the junction (Fig. 11). Free-standing metallic mesh bandpass filters which have a 10 per cent bandpass at the frequency of interest are placed in front of the lens [29]. One filter is at 4.2 K, and a dual filter is set at 77 K to block the room temperature radiation. The dual filters are offset from each other to block optical paths as well. The whole system is placed in an Infrared Laboratories HD 3-(8) dewar. In addition, we have external lenses to couple the radiation into the dewar. The radiation is provided by an Apollo far infrared laser system, Model 122.

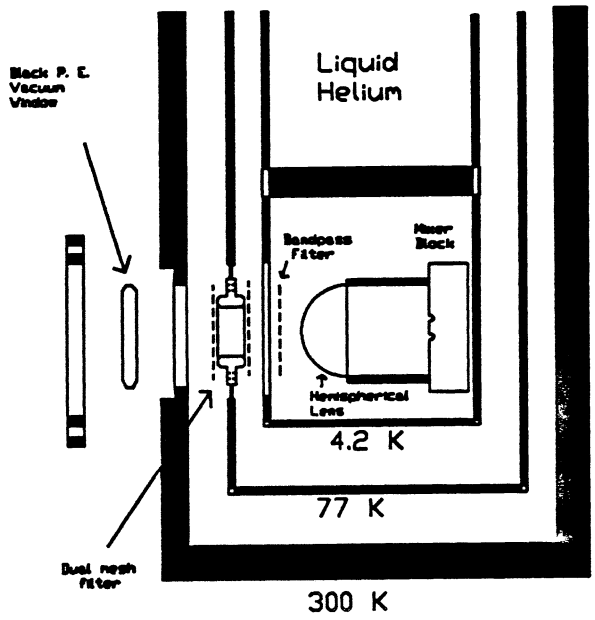

Figure 11. Schematic of the cryogenic dewar used for direct detection measurements.

The responsivity of these junctions has been measured for different power levels at 585 GHz and 763 GHz. Examples of the response at 585 GHz are shown for a two junction array with A = 1 μm^2 (Fig. 12a) and a six junction array with A = 2 μm^2 (Fig. 12b). An example of the response at 763 GHz taken for a six junction array is also shown (Fig. 12c). The measurements at 585 GHz show both quasiparticle and Josephson response. The Tien-Gordon equation was applied to the DC I-V curve and fitted to the experimental response curve in order to separate the two responses. As can be seen, the Tien-Gordon model works well above the gap at 585 GHz, but the Josephson effects interfere below the gap. This problem is particularly obvious in the six junction response ($\alpha = 0.66$) where a large Josephson step appears at about the half-gap. In the two junction array, the expected quasiparticle current, as predicted by the fit, was subtracted from the experimental curve, and the excess currents were found to follow qualitatively the expected power dependence of the Josephson response. We

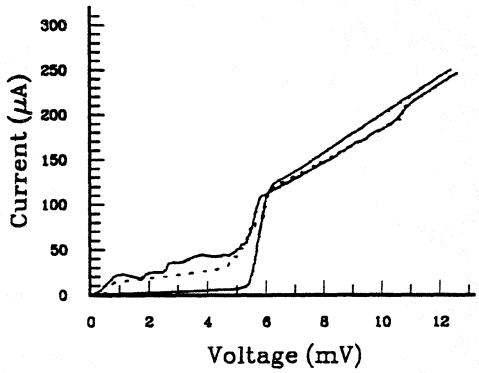

Figure 12a. D.C. I-V characteristic, experimental response, and fitted theoretical response (dashed) at 585 GHz with a two junction array.

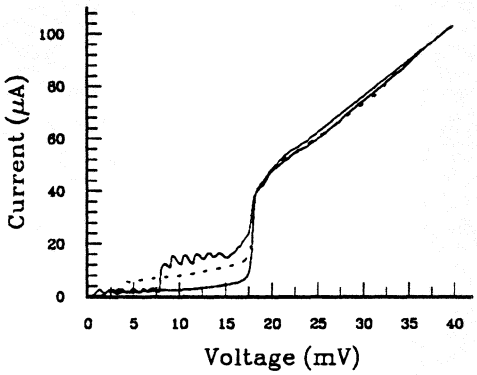

Figure 12b. D.C. I-V characteristic, experimental response, and fitted theoretical response (dashed) at 585 GHz with a six junction array.

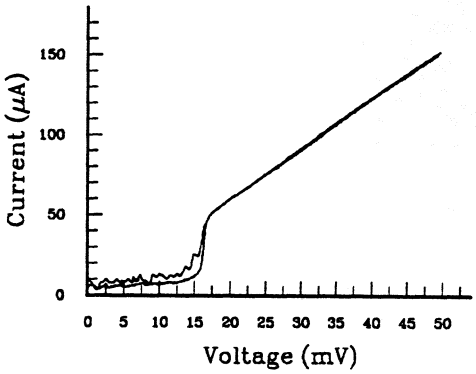

Figure 12c. D.C. I-V characteristic and experimental response at 763 GHz with a six junction array.

are currently extending our model to include the Josephson terms. Using the fitted value of $\alpha = 0.75$ and the theoretical dynamic resistance, the quasiparticle current response at 585 GHz was found to be 350 A/W, or $0.84(\hbar\omega/e)$. Our NEP measurements to date are not presented because they are amplifier-limited; future measurements will be made using low noise amplifiers.

IV. Summary

SIS mixer elements, based on the Nb/Al trilayer system, have given excellent results at millimeter wavelengths. Although other material systems and geometries (the NbN/MgO material system and the edge geometry in particular) appear attractive for submillimeter wavelengths, the Nb/Al trilayer system may prove to be a competitive technology. Our present research with the Nb trilayer system includes new fabrication techniques for sub-square-micron junction areas, SIS individually tuned and fixed tuned detector elements, and SIN structures. Direct detection experiments have been made at 585 GHz and 763 GHz with SIS junctions and a quasiparticle current response of $0.84(\hbar\omega/e)$ at 585 GHz was measured.

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