Sub-Millimeterwave InP-Based High Electron Mobility Transistors

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ABSTRACT

We report on a recent development of a 80 nm gatelength, InP-based Self-Aligned T-Gate High Electron Mobility Transistor (SAGHEMT) with an extrinsic current gain cutoff frequency (f_T) of 250 GHz. After subtracting a 10 fF gate pad capacitance, the intrinsic f_T of this device was estimated to be as high as 330 GHz. We believe that, with further scaling and optimization, the InP-based SAGHEMT holds great potentials as a planar, three-terminal semiconductor device at sub-millimeterwave frequencies.

INTRODUCTION

As the gatelength of a field-effect transistor (FET) approaches the nanometer regime, it becomes increasingly more difficult to improve the device speed by simply reducing the gate length. In this gate length regime, parasitic delays, such as drain delay (due to the extension of the drain depletion region) and capacitance charging time (gate pad and fringe), represent a large portion of the total delay and will ultimately limit the device extrinsic speed [1-3]. Evidences that support this claim are plenty and can be readily observed by plotting the f_T as a function of gate length. This is shown in Fig. 1 for a number of selected InP-based HEMTs fabricated in our laboratories [4, 5]. Due to parasitic delays, the rate of increase of f_T is significantly degraded as the gate length approaches the nanometer regime. In fact, we predict that a factor-of-2 reduction in gate length from the current 0.1 μm technology will only result in an approximately 50% increase in f_T.

Recently, however, a new, nanometer-scaled Self-Aligned Gate (SAG) process has been developed [5], in which the electron-beam-defined T-shaped gate serves as a shadow mask during

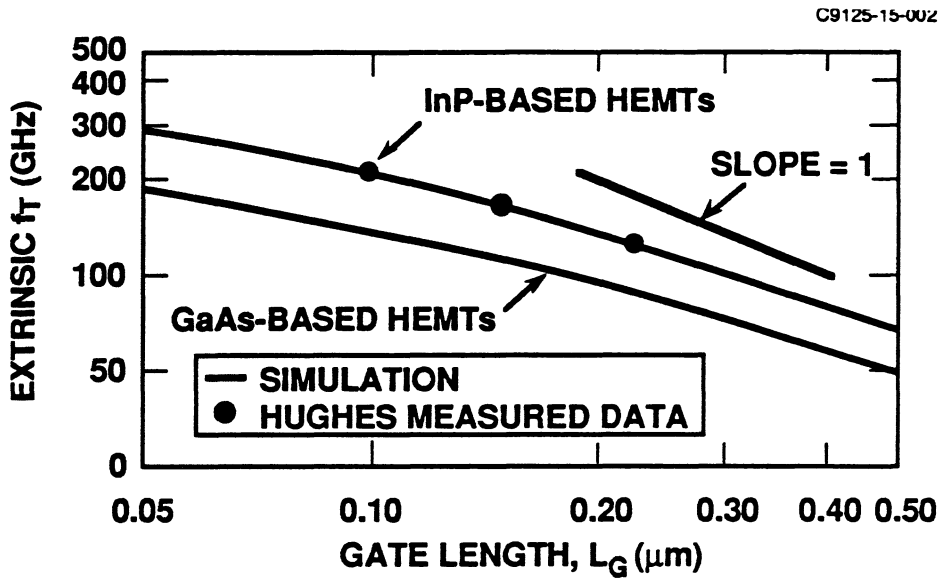


Fig. 1. Scaling of AlInAs/GaInAs HEMTs with gatelength. The effects of parasitics on f_T are evident at L_G <0.1 μm.

ohmic deposition, allowing the source and drain contacts to be "self-aligned" to the gate. This process has significantly reduced the device source and drain resistances, as well as the various parasitic delays associated with them [6]. Our recent work in this area and that of Mishra et al. have resulted in a record room-temperature f_T of 250 GHz for InP-based SAGHEMTs with gatelength between 80 and 120 nm [5, 7].

In the followings, we will present a characterization of the 80 nm gatelength InP-based SAGHEMT reported in Ref. [7], with particular emphasis on its potential scaling for sub-millimeterwave applications. With further optimization, we believe that it is possible to realize an ultrahigh performance InP-based SAGHEMT with 50 nm gatelength.

DEVICE FABRICATION

The process flow for the fabrication of our SAGHEMTs, as shown in Fig. 2, is identical to that in Ref. [4]. It typically consists of five major levels: (1) alignment marks, (2) device isolation, (3) T-gate definition by electron-beam lithography, recess, and metalization, (4) ohmic definition,

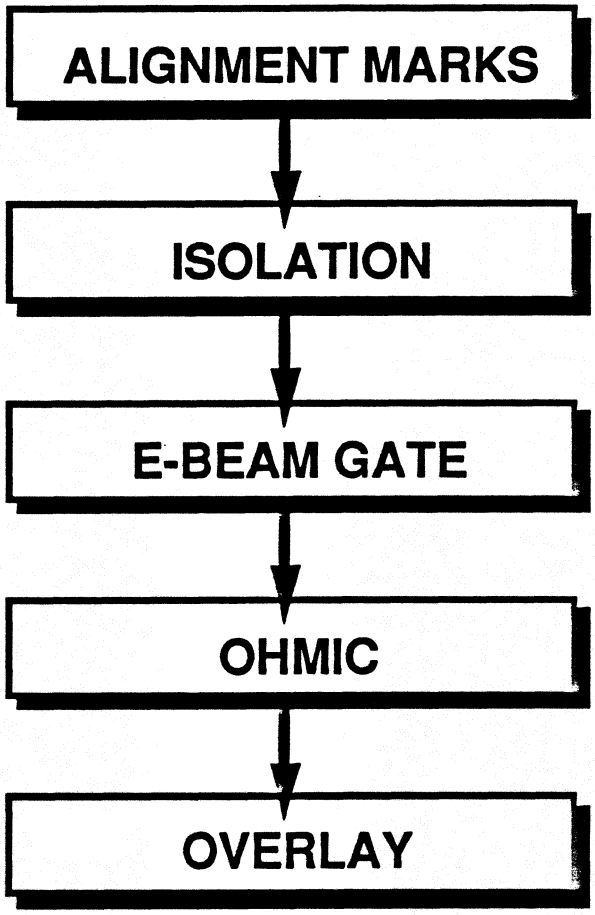


Fig. 2. Process flow for 80 nm SAGHEMTS.

metalization (with the T-gate serves as a shadow mask), and alloying, and (5) overlay metalization. In this self-aligned gate scheme, the ohmic level follows, rather than precedes, the gate level. Consequently, it is important that the ohmic alloying temperature not exceed some critical temperature beyond which the Schottky gate characteristic may be significantly degraded.

At the present time, we have routinely achieved a resolution of 80 nm for our T-gate process using a Phillips EBPG-4 electron-beam lithography system. This T-gate then serves as a shadow mask during ohmic deposition and effectively defines the source-drain contacts. A Scanning Electron Micrograph (SEM) of a typical SAGHEMT fabricated in this work is given in Fig. 3, which shows a gate length of approximately 80 nm and a source-drain spacing of 0.3 μm.

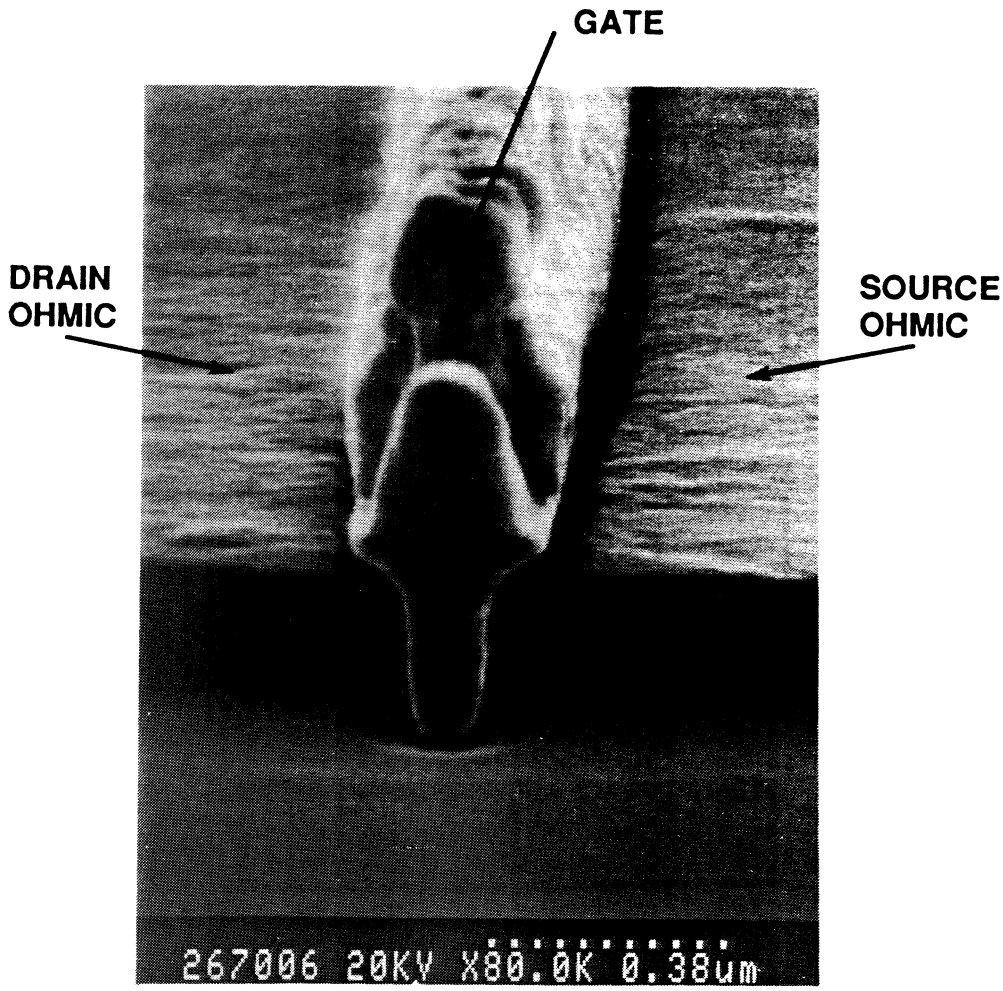


Fig. 3. SEM photograph of a 80 nm self-aligned HEMT with 0.3-μm source-drain spacing.

DEVICE RESULTS

We have successfully fabricated three (3) wafers with almost identical results using the above process. Typically, we have achieved a dc transconductance (g_m) of 950 to 1050 mS/mm for devices with a nominal threshold voltage (V_{th}) of - 0.5 V, and 1050 to 1150 mS/mm for those with a V_{th} of - 0.2 V.

The I-V characteristics of a typical 80-nm by 50-μm InP-based SAGHEMT with a g_m of 1050 mS/mm is given in Fig. 4. Despite the very short gatelength and source-drain spacing employed, the device exhibits excellent pinchoff characteristics and shows no apparent sign of "short channel" effects. As a result, we believe that further improvements can be obtained by reducing the gatelength to 50 nm.

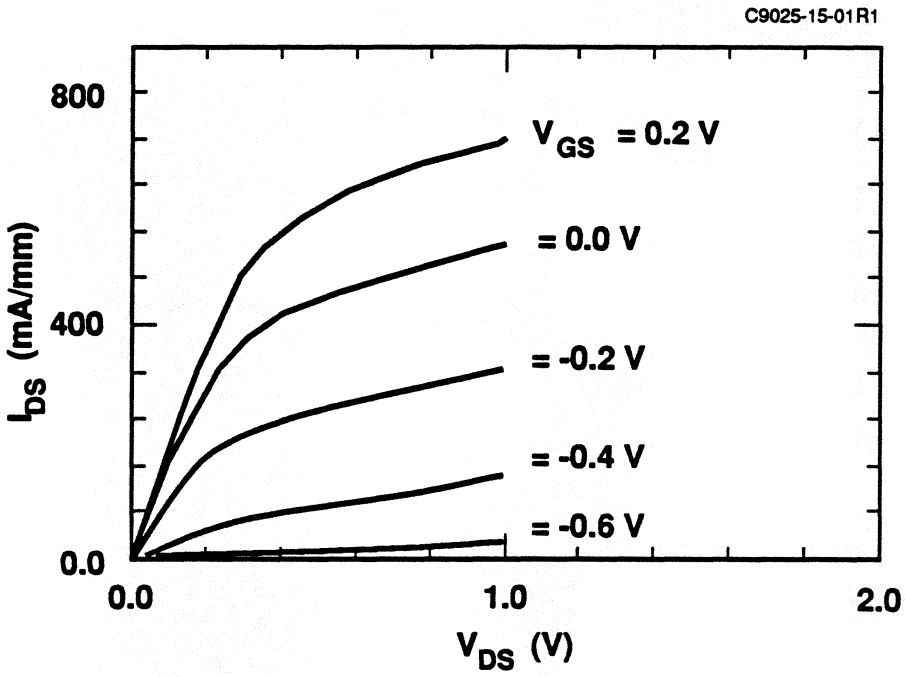


Fig. 4. I-V characteristics of a typical 80-nm by 50-μm AlInAs/GaInAs SAGHEMT.

As shown in Fig. 5, the extrapolation of the current gain versus frequency of a 80-nm by 50-μm SAGHEMT yields an extrinsic f_T of approximately 250 GHz. Without the presence of a 10 fF gate pad capacitance, the f_T (intrinsic) of the device was estimated to be as high as 330 GHz, which, we believe, is the highest value yet reported for any three-terminal semiconductor devices.

The potential scaling of our SAGHEMTs for sub-millimeterwave applications can be best examined with the aid of a small signal equivalent circuit model (see Fig. 6). Due to the very large gate periphery employed (e.g., 50 μm) and the presence of the gate pad capacitance, the power gain cutoff frequency (f_{max}) of our devices is currently limited to approximately 220 to 300 GHz. However, this limitation should be readily overcome by a simple scaling of gate width (W) since [8]

$$f_{max} = \frac{f_T}{\sqrt{4g_{ds}\left(R_s + R_i + R_g W^2 + \pi f_T L_s W\right) + 4\pi f_T C_{gd}\left(R_s + R_i + 2R_g W^2 + 2\pi f_T L_s W\right)}}$$

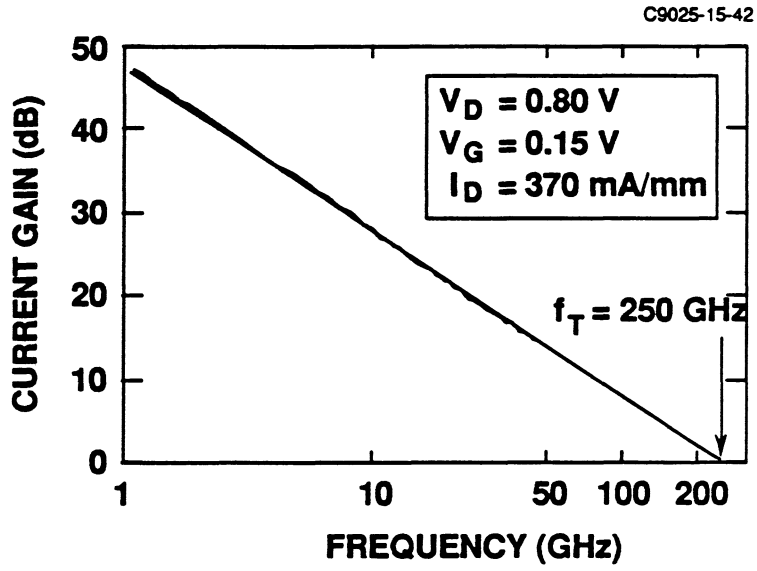
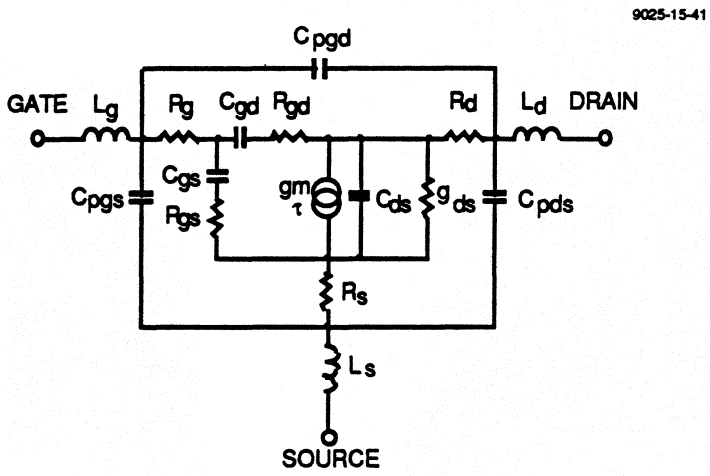


Fig. 5. Current gain versus frequency of a 80 nm by 50 μm AlInAs/GaInAs SAGHEMT (f_T = 250 GHz).

where f_T is the intrinsic value (ignoring the gate pad capacitance) and the various circuit elements are expressed in their respective units for a 1-mm-wide device. Thus, for the SAGHEMT presented in Fig. 6, f_T = 330 GHz, g_{ds} = 152 mS/mm, R_s = 0.11 Ω*mm, R_i = R_{gs} = 0.05 Ω*mm, R_g = 140 Ω/mm, C_{gd} = 0.1 pF/mm, and L_s = 6.0 pH. As shown in Fig. 7, our calculation suggests that a significant increase in f_{max} can be achieved with a smaller gate width device. In fact, an f_{max} in excess of 600 GHz has been estimated for a 10-μm-wide SAGHEMT, which clearly shows its great potentials as a planar, three-terminal semiconductor device for sub-millimeterwave applications.

We believe that even higher device performance can still be obtained with a further reduction in gate length and gate-to-channel separation. As shown in Fig. 8, we have simulated the dependence of the extrinsic f_T on gate length for an optimized InP-based SAGHEMT with a g_m of approximately 1400 mS/mm. At a gatelength of 50 nm, we predict an extrinsic f_T (including a 10 fF gate pad capacitance) approaching 400 GHz. This corresponds to an intrinsic f_T as high as 560 GHz and should result in significant improvements in device performance.



INTRINSIC DEVICE		PARASITIC ELEMENTS	
C_{gs}	= 33.0 fF	R_g	= 7Ω
R_{gs}	= 1.0 Ω	R_d	= 3Ω
C_{gd}	= 5.0 fF	R_s	= 2.2Ω
R_{gd}	= 240 Ω	C_{pgs}	= 6.5 fF
g_m	= 79 mS	C_{pgd}	= 2.5 fF
τ	= 0.6 ps	C_{pds}	= 12.0 fF
C_{ds}	= 2.0 fF	L_g	= 33 pH
g_{ds}	= 7.6 mS	L_d	= 27 pH
		L_s	= 6.0 pH

Fig. 6. An equivalent circuit model of a 80-nm by 50-μm AlInAs/GaInAs SAGHEMT.

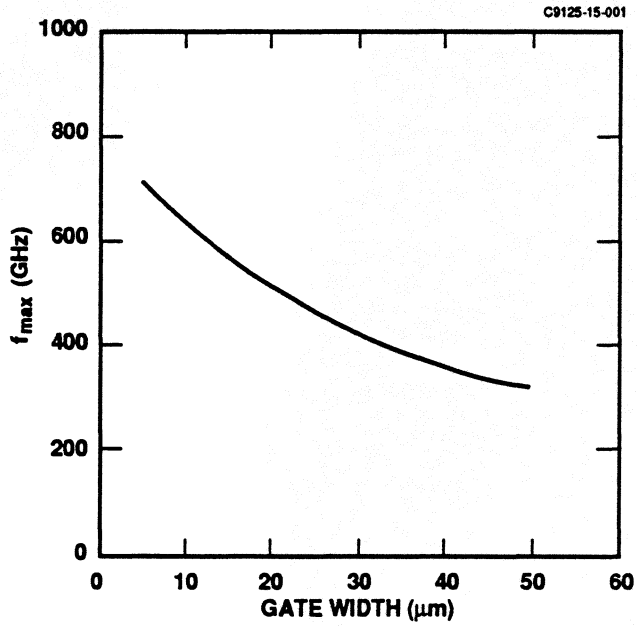


Fig. 7. Simulated results for F_{max} as a function of gate width.

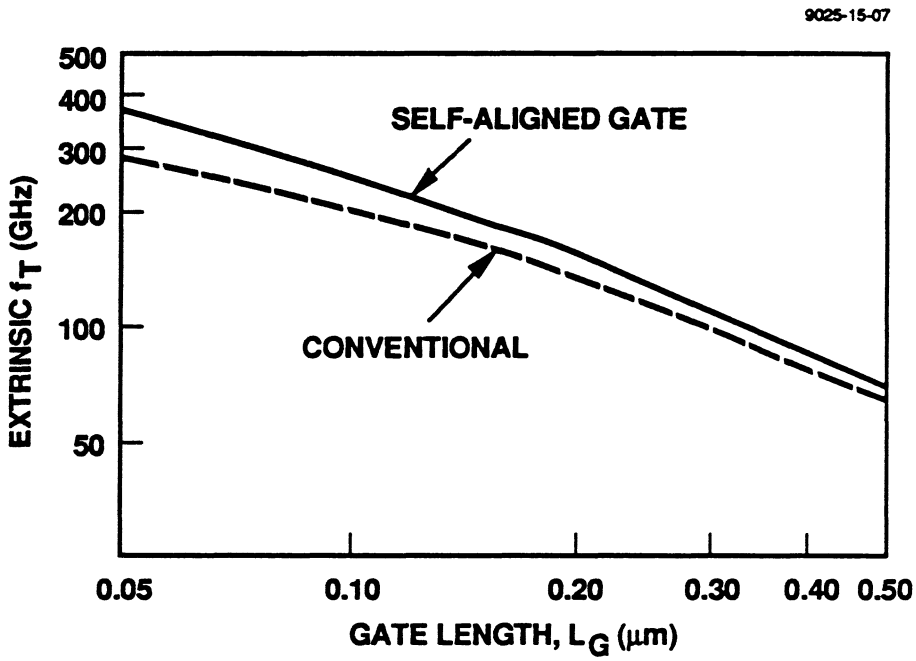


Fig. 8. Projected performance of self-aligned gate AlInAs/GaInAs HEMT in the early 1990s.

CONCLUSIONS

We have presented a characterization of a 80 nm gatelength InP-based SAGHEMT with good pinchoff characteristics and state-of-the-art f_T of 250 GHz. Our analysis indicates that it is possible to significantly improve the f_T by a further reduction of gate length, and the f_{max} by a simple scaling of gate width. We believe that, with further optimization, the InP-based SAGHEMT is an attractive candidate for sub-millimeterwave applications.

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