A 200 GHz TRIPLER USING SINGLE BARRIER VARACTOR

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ABSTRACT

The GaAs Schottky varactor diode is the non-linear device most commonly used for submillimeter wave harmonic generation. Output power adequate to serve as a local oscillator source for SIS tunnel junctions has been demonstrated with whisker-contacted GaAs Schottky varactor multipliers in waveguide mounts up to about 800 GHz. In this paper, we present results for a tripler to 200 GHz using a new multiplier device, the single barrier varactor (SBV). This new varactor has a potential advantages such as stronger non-linearities or special symmetry, which make it attractive for submillimeter wave frequency multiplication.

The performance of a tripler using a SBV over a output frequency range from 186 to 207 GHz has been measured in a crossed waveguide mount. The theoretical performance of the device has been calculated using large signal analysis. A comparison

of theoretical and measured results and a discussion of various losses in the mount and the varactor have also been presented.

INTRODUCTION

Heterodyne receivers are used for high spectral resolution shorter-millimeter and sub-millimeter wave astrophysics and earth remote sensing observations. Local oscillator, mixer and antenna are the critical components in a receiver. One approach to provide sub-millimeter power is to use the combination of a high-power millimeter-wave source with a harmonic multiplier for higher frequency generation. Frequency multipliers use a non-linear device to generate harmonics of the input frequency from a fundamental oscillator. Although the Manley-Rowe relations show that an ideal harmonic genarator with 100% efficiency is possible with a varactor, real multiplier circuits are limited by loss in the device and circuit and by impedance matching limitations at the input, output, idler and harmonic frequencies [1,2]. As the circuits become smaller with increase in frequency, impedances and losses become more difficult to control.

To achieve the full capability of the diode, appropriate embedding impedances must be provided by the multiplier mount. The impedances at the input and output frequencies must be set to maximize coupling power into or out of the device. In higher order multipliers, current flow at the intermediate harmonics (i.e. the idler frequencies) will enhance harmonic conversion. Therefore, the diode must be terminated with a lossless reactance at these frequencies. The embedding impedances are provided by the multiplier mount. Nonlinearities symmetric about zero bias will generate only odd

harmonics, greatly simplifying the multiplier mount design. For instance a tripler mount for a symmetric device will be equivalent to a doubler mount for a device without symmetry. Similarly, a quintupler mount will be equivalent to a tripler mount, both requiring one idler.

This paper presents the theoretical and experimental results of a 200 GHz tripler using a single barrier varactor (SBV) as the nonlinear device.

MULTIPLIER DEVICE

The single barrier varactor diode used as the multiplier device in our experiment, was developed at the Chalmers University of Technology [3,4]. These Chalmers devices were fabricated with the epitaxial GaAs/$Al_{0.7}Ga_{0.3}As$/GaAs material grown as indicated in Fig.1. It is inherently a symmetric device. The $Al_{0.7}Ga_{0.3}As$ barrier

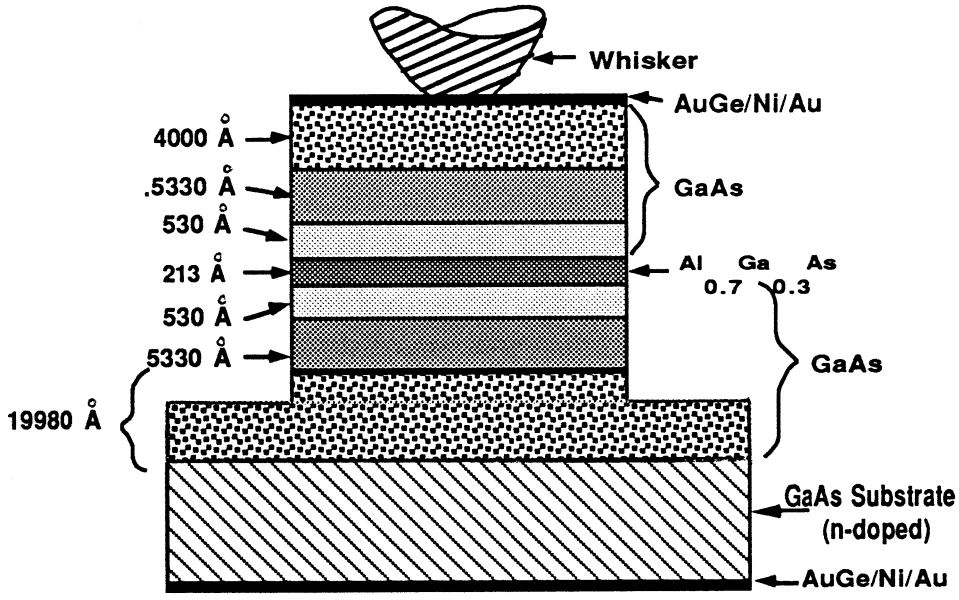

Fig.1: Schematic of the Chalmers Device

which blocks the current flow is in the center having a thickness of 213 Å. On either side of the barrier, there is an undoped GaAs spacer having a thickness of 53 Å. GaAs depletion region ($n=1x10^{17}$ cm^{-3}) on either side has a thickness of 5330 Å. Top and bottom contacts are formed on highly doped GaAs regions ($n=3.4x10^{18}$ cm^{-3}) using 1000 Å AuGe, 200 Å Ni and 1600 Å Au. The top contact is made with a whisker and the bottom is a large area ohmic contact. The $Al_{0.7}Ga_{0.3}As$ barrier will to a large extent prevent electrons from passing through the structure. Thus the conduction current through the device is very small. For moderate voltages, the conduction current is essentially caused by thermionic emission. The width of the depleted part of the moderately doped epitaxial layer will vary with bias voltage, thus forming a voltage dependent capacitance C(V). When the diode is biased in the forward direction, the depleted region will appear on one side of the barrier, and the depletion capacitance of the device will decrease with increasing voltage. Since the diode is symmetric, a reverse bias will in the same way cause a decrease in the capacitance value of the device. Hence, the maximum capacitance is obtained for zero voltage and is determined by the thickness of the $Al_{0.7}Ga_{0.3}As$ barrier. The minimum capacitance which occurs for maximum bias voltage, is determined by the doping concentration and the extension of the moderately doped drift region. For an appropriately designed device, similar capacitance swing with voltage as for the Schottky-varactor diode is expected [5].

The losses due to the series resistance may be larger in the SBV diode than in Schottky varactors, since the maximum current $i_{max}= CdV/dt$ will occur for $V(t) = 0$, i.e. when both dV/dt and C are maximum and n-doped drift regions on both sides of the barrier are undepleted and contribute to the series resistance. In addition, for small area device, the ohmic contacts exhibits higher resistance than Schottky contacts. However for a Schottky varactor tripler, the idler current at the second harmonic will degrade

the tripler performance, since any finite reactance termination will cause power losses in the series resistance. For the SBV tripler, this particular problem is virtually non-existent [4].

The Chalmers devices tested here, have a mesa height of about 2.5 microns and area of 5x5 micron^2. In order to evaluate the dc characteristics, the device has been mounted in a coaxial mount as shown in Fig.2. The S-parameters are measured using a HP 8510B Network Analyzer. The K-connector provides 50 ohms up to the whisker to allow accurate de-embedding of the mount [6]. The equivalent circuit of the diode mounted in a co-axial mount is shown in Fig.3. Chalmers device was measured to have a dc series resistance of 7 ohms. The measured C-V and I-V characteristics for the 5x5 micron^2 Chalmers device are shown in Fig.4. The measured maximum capacitance is

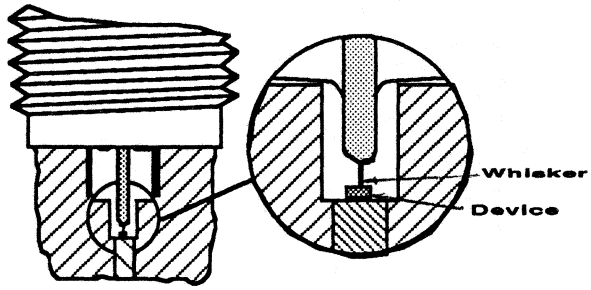

Fig.2 : Schematic diagram of the device mounted in a coaxial mount

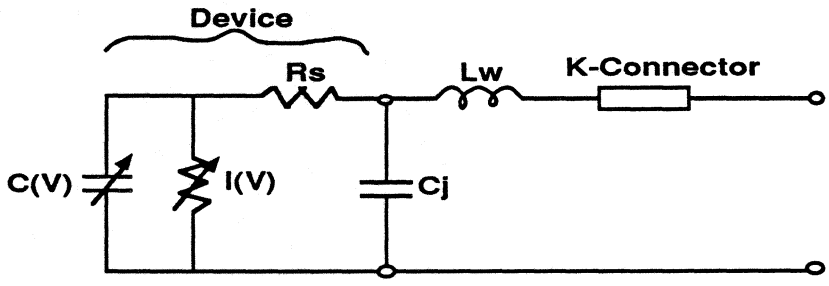

Fig. 3 : Equivalent circuit of a device in a coaxial mount

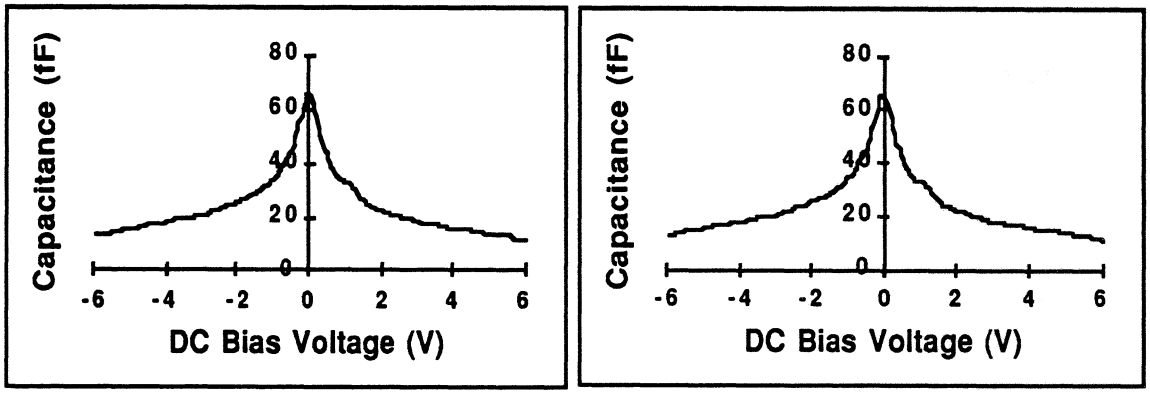

Fig.4 : Measured C-V and I-V characteristics of Chalmers device

65.6 fF and minimum capacitance is 12.4 fF. The figure of merit of the diode, which is its cut-off frequency, is given by,

$$f_c = \frac{1}{2\pi R_s} \left\{ \frac{1}{C_{min}} - \frac{1}{C_{max}} \right\}$$

Chalmers device has a cut-off frequency of 1200 GHz. The diodes are found to be damaged when the dc voltage exceeded about 6V.

LARGE SIGNAL ANALYSIS

The critical step in the multiplier analysis is to solve the voltage and current waveforms of the nonlinear device which is pumped and biased in an arbitrary embedding network. A common solution of this nonlinear problem is to use a type of harmonic balance technique. Time-domain current and voltage solution are sought which

satisfy the diode conditions and frequency-domain solutions are sought which satisfy the external circuit equations. In this work, a modified nonlinear program based on Siegel, Kerr and Hwang [5] has been used in order to calculate the tripling efficiency of the Chalmers single barrier varactor diodes. Fig. 5 shows the equivalent circuit of a

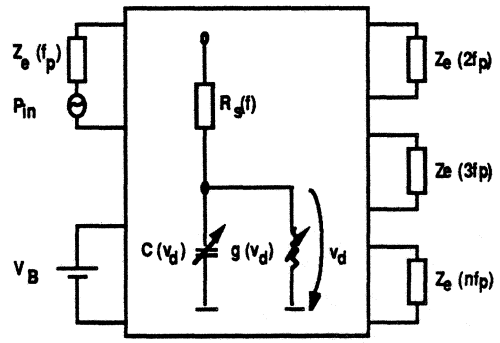

Fig.5 : Eduivalent circuit of a multiplier

multiplier. Harmonic triplers with 186 GHz,192 GHz, 200 GHz, 207 GHz output frequencies are calculated. We have optimized the impedance at the third harmonic frequency. The idler and the higher harmonics are set to open circuits. Impedance up to 12th harmonic are analyzed. In the analyses, the measured C-V and I-V characteristic shown in Fig.4 have been used. Since the series resistance is important in the device performance, the calculations are carried out for a range of resistances, 5 ohm, 10 ohm, 15 ohm and 20 ohm.

Fig.6 presents efficiency versus the input power for a SBV tripler to 192 GHz taking series resistance of the device as a parameter. In order to quantify the effect of current flow in the device on the multiplier performance, we have calculated the performance for a device with 5 ohm series resistance with no current. The theoretical efficiency is found to degrade from 45% to 20% when the measured current is included. Higher device series resistance degrades the tripler performance significantly as the

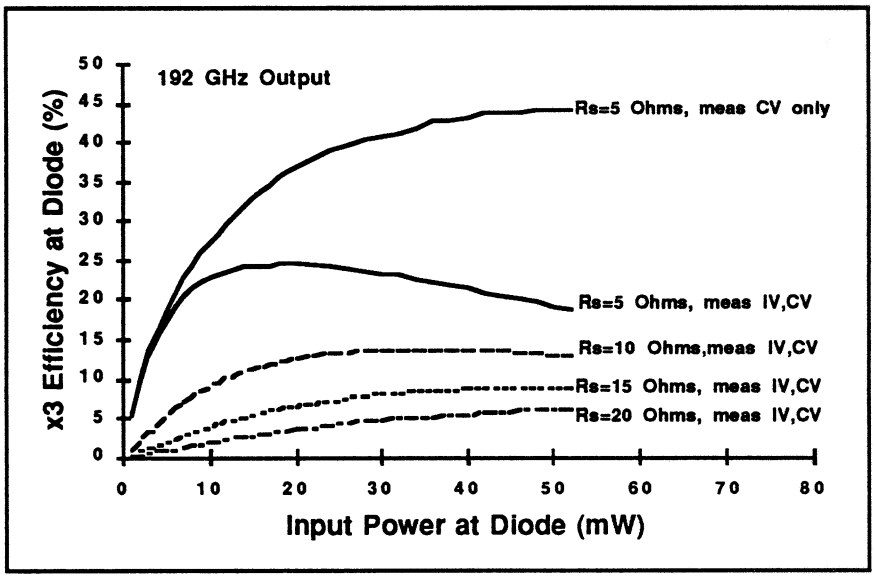

Fig.6 : Calculated tripling efficiency for Chalmers device

series resistance of 20 ohm results in about a factor of four worst performance than a series resistance of 5 ohm.

200 GHz WAVEGUIDE MOUNT

To achieve optimum performance of the device, it must be provided with the appropriate circuit embedding impedances. The impedances at the input and output frequencies must be set to maximize coupling power into or out of the device. In higher order multipliers, current flow at the intermediate harmonics i.e. the idler frequencies will enhance the harmonic conversion. Therefore, the diode must be terminated with a lossless reactance at these frequencies.

An output of the large signal analysis, used to optimize the device, is the

required embedding impedance. In fig.7, the real part of the optimum impedance is

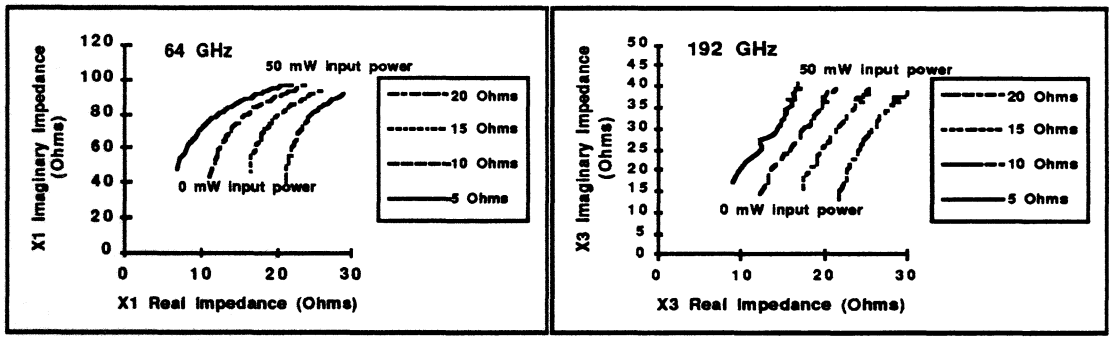

Fig. 7 : Input and output circuit optimum embedding impedances calculated by large signal analysis

shown on the horizontal axis and the imaginary part on the vertical axis, parameterized by the input power for both the input frequency (R_1, X_1) and the output frequency (R_3, X_3). Impedances are plotted for different series resistances of the device. Input power increases from 0 mW to 50 mW. At low input power the real part is same as the device series resistance. The input imaginary impedance is the impedance corresponding to the maximum capacitance at input frequency. As the input power increases, the device capacitance decreases increasing the impedance. The real impedances needed are in the range from 7-30 Ohms. The imaginary impedances range from 40-100 Ohms for the input circuit and from 15-42 Ohms for the output circuit respectively.

The embedding impedances are provided to the single barrier varactor (SBV) device by a crossed waveguide mount. In addition the mount distributes the power. A schematic drawing of the crossed waveguide mount is shown in Fig.8. The single barrier varactor device is mounted spanning the output waveguide. The output waveguide is actually oriented perpendicular to the plane of the paper. Power at the input frequency travels down the input waveguide. A low pass filter consisting of Au metallization on the

quartz substrate couples the input power from the waveguide to the whisker contacted

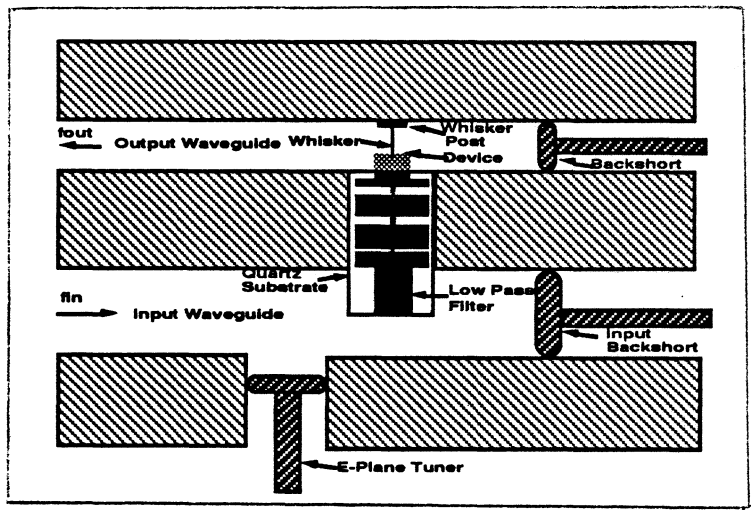

Fig.8 : Schematic diagram of the device in the mount

SBV device located at the output waveguide. An E-plane tuner and a backshort at the input waveguide provide adjustments to optimize the embedding impedance at the input frequency. The output waveguide is cutoff at the input frequency preventing propagation down it, thereby confining the input power to the vicinity of the SBV device. The tripled power is coupled out the output waveguide. The embedding impedance at the output frequency is adjusted by varying the whisker length and by a movable backshort. The low pass filter prevents the output frequency from traveling to the input waveguide. A scanning electron micrograph of the device in the mount is shown in Fig. 9.

EXPERIMENTAL RESULTS

The set-up for 200 GHz tripler measurements is shown schematically in Fig.10. A 60-70 GHz klystron is used as the pump source. The input power is monitored

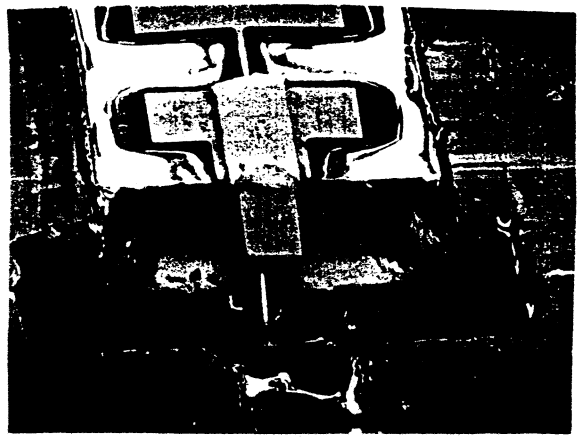

Fig. 9 : Scanning Electron Micrograph of the device in the mount

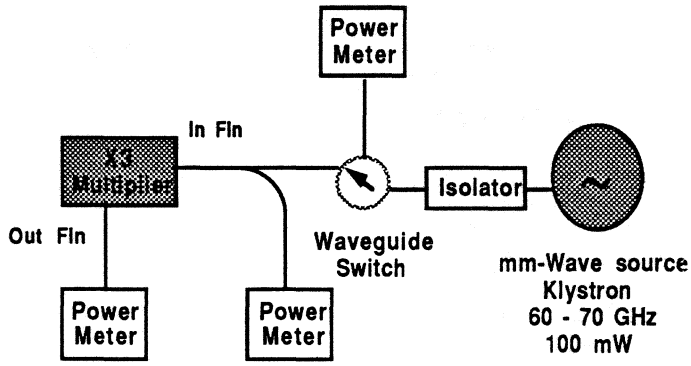

Fig.10 : Test setup for the 200 GHz tripler measurement

by a Anritsu power meter, calibrated to give the power at the input flange. The reflected power is measured using a directional coupler coupled to a second power meter. The third harmonic output power is measured by a third powermeter. We determine the loss at the third harmonic in the waveguide from the output flange to the powermeter by a substitution technique. The observed loss in the WR4 output waveguide is 0.032 dB/λ,

consistent with the resistive losses corresponding to the metal conductivity of $2x10^7$ mho/m. The flange-to-flange efficiency is defined as the ratio of the power at output flange to the power available at the input flange. Using various whisker lengths, the efficiency and output power were measured between 186-207 GHz. Measurements were taken with three different whisker lengths, 6 mil, 8.4 mil and 11 mil. It was seen that, the Chalmers 25 micron^2 device, contacted with a 8.4 mils long whisker gives best tripler performance. The measured efficiency versus input power for 186 GHz, 192 GHz, 196.5 GHz and 201 GHz output frequencies are shown in Fig.11 for a 8.4 mil long

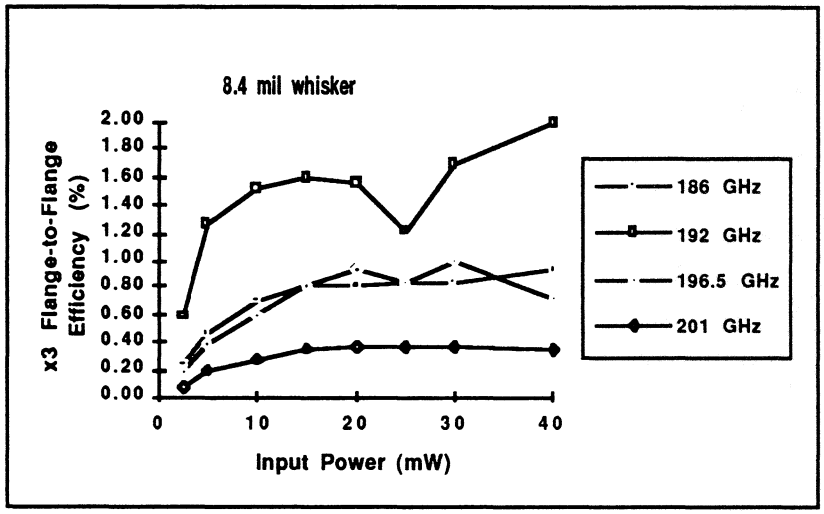

Fig.11 : Measured efficiency versus input power plot for the tripler

whisker contact. The best performance has been achieved at 192 GHz, giving an efficiency of more than 2% at 40 mW input power. This is similar to the results demonstrated by Rydberg et al. using the same device [3].

To compare the experimental results to the performance predicted by large signal analysis, the loss in the multiplier mount is assesed. Loss arises from several mechanisms. At the input frequency, the finite conductivity of the waveguide and

dielectric loss in the filter are very small. The primary loss mechanism is due to the impedance mismatch. By measuring reflected power at the input, less than 0.2 dB loss due to mismatch was observed, over the frequency range tested.

At the output frequency, the impact of finite conductivity is higher. In addition, losses due to imperfections in the backshort are critical. Other mechanisms include the impedance mismatch and higher harmonic generation.

Some of these loss mechanisms at the output frequency have been modeled using Hewlett Packard's Microwave Design System (MDS) package. Fig.12 shows the

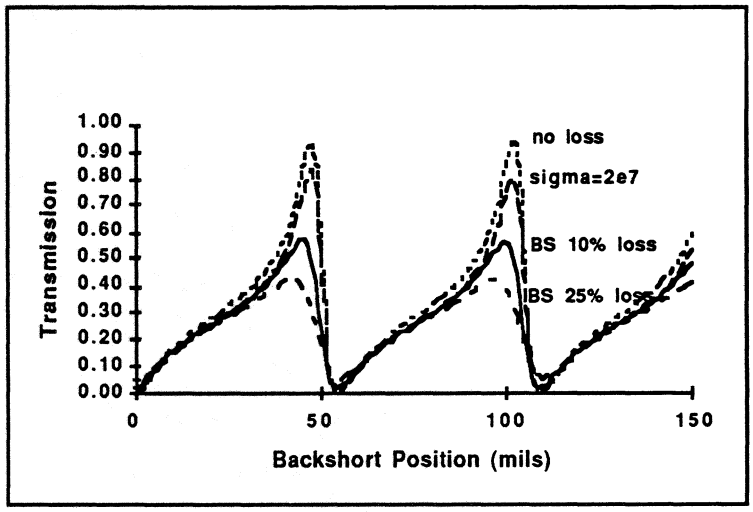

Fig.12 : Calculated transmission from the diode to the output flange of the tripler mount

calculated transmission from diode in the tripler mount to the output flange of the mount as a function of backshort position. When there is no loss, the transmission is 100% at resonant positions of backshort. If a finite conductivity of 2×10^7 mho/m, the measured conductivity of the WR4 output waveguide is included, the peak transmission reduces to about 90%. If in addition, the backshort has a 10% loss, the transmission reduces to

about 60%. For a backshort loss of 25%, the transmission goes down to 40%. The losses reduce the height of the peaks and the sharpness of the resonances out. In addition, the antiresonant backshort positions donot give zero percent transmission.

The measured results are plotted in Fig.13, which shows the relative

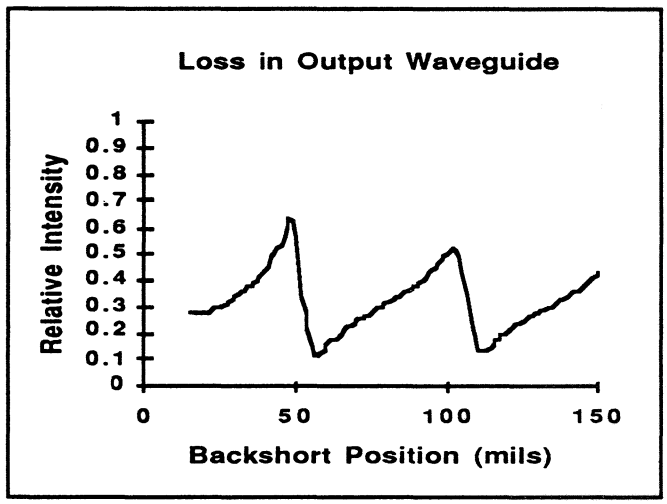

Fig.13 : Plot of measured output power as a fumction of output backshort position

output power as a function of output backshort position. This looks qualitatively similar to the theoretical results. The measured first peak match the theoretical results with 10% backshort loss, while the valley and second peak are closer to the 25% backshort loss.

Based on these observations, the multiplier mount loss budget is presented in Table-I. In the output circuit, the loss due to the finite conductivity is estimated as 1 dB. Loss due to backshort is 3 dB. Impedance mismatch loss and loss due to higher harmonics are not known. Therefore, the loss in the output circuit is estimated to be more than 4 dB. Input circuit loss is estimated to be less than 0.2 dB. Using these loss values, 0.2 dB at input and 4 dB at output, the measured flange-to-flange efficiency is

Table - I

	Loss
Output Circuit	
Finite Conductivity	**1 dB**
Backshort Loss	**3 dB**
Impedance mismatch	**?**
Higher harmonics	**?**
Total	**> 4 dB**
Input Circuit	
Impedance Mismatch (Reflected power)	**0.2 dB**

corrected to determine the efficiency at diode, which is plotted in Fig.14. Superimposed of diode efficiencies are the theoretical efficiency calculated from the measured CV and IV curves for series resistances 10 ohm, 15 ohm and 20 ohm. At low input power the measured efficiency follows the theoretical efficiency for a series resistance of about 12 ohm. The measured dc series resistance is 7 ohm. At 192 GHz, the series resistance is

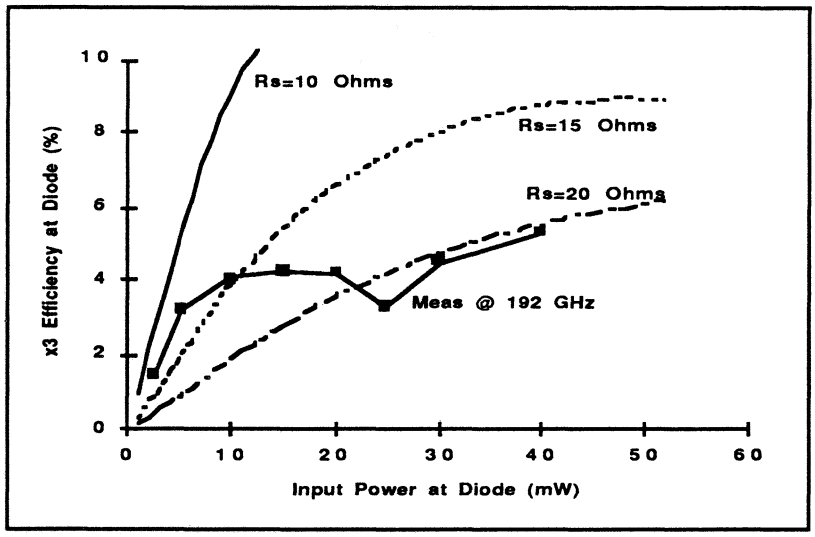

Fig.14 : Tripling efficiency at diode versus input power plot

expected to be somewhat higher due to skin effect. At higher power the efficiency falls off. This fall off corresponds to the power at which the device starts drawing significant current. This suggests that the impact of the current flow in the device on the multiplier performance is not well understood.

DISCUSSION AND CONCLUSION

The single barrier varactor diode has been shown to be able to provide more than 5% efficiency as a 200 GHz tripler. About 2% flange-to-flange tripling efficiency is obtained using the crossed-waveguide tripler mount for symmetric devices. The multiplier mount has a 0.2 dB input circuit loss due to the impedance mismatch, introduced by the reflected power. A total loss of more than 4 dB is estimated at the output circuit. This includes the 1 dB loss due to finite conductivity of the waveguide and 3 dB loss due to the backshort.

Development of devices with lower leakage current will significantly improve the tripler performance. Results can be further improved by reducing the output circuit 4 dB loss by improving the imperfect backshort.

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