New Approach to the Design of Schottky Barrier Diodes for THz Mixers

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Abstract

Near–ideal *GaAs* Schottky barrier diodes especially designed for mixing applications in the *THz* frequency range are presented.

A diode fabrication process for submicron diodes with near–ideal electrical and noise characteristics is described. This process is based on the electrolytic pulse etching of *GaAs* in combination with an in–situ platinum plating for the formation of the Schottky contacts. Schottky barrier diodes with a diameter of 1 μm fabricated by the process have already shown excellent results in a 650 *GHz* waveguide mixer at room temperature. A conversion loss of 7.5 *dB* and a mixer noise temperature of less than 2000 *K* have been obtained at an intermediate frequency of 4 *GHz*.

The optimization of the diode structure and the technology was possible due to the development of a generalized Schottky barrier diode model which is valid also at high current densities. The common diode design and optimization is discussed on the basis of the classical theory. However, the conventional formulas are valid only in a limited forward bias range corresponding to currents much smaller than the operating currents under submillimeter mixing conditions. The generalized new model takes into account not only the phenomena occurring at the junction such as current dependent recombination and drift/diffusion velocities, but also mobility and electron temperature variations in the undepleted epi–layer.

Calculated diode *I/V* and noise characteristics are in excellent agreement with the measured values. Thus, the model offers the possibility of optimizing the diode structure and predicting the diode performance under mixing conditions at *THz* frequencies.

Introduction

Schottky–barrier diodes have been recently applied for heterodyne receivers in the frequency range up to a few THz, the interesting point being how their realization and technology can be improved to obtain still better results at higher frequencies. Much effort has been done to reduce the feature sizes, but further reduction beyond approximately $0.5\mu m$ seems to be unpractical because of contacting difficulties. Since maximizing of the conversion efficiency requires a resistive mixing, the junction resistance at the operating point has to be much smaller than its capacitive reactance to avoid losses related with parametric downconversion.

Therefore, for the highest frequencies despite the decreasing diameter, the DC current at the operating point is always of the order of 0.5 mA, leading to an increased current density and therefore the bias approaches the so called flat–band voltage. The expressions for the I/V and the C/V characteristics of Schottky diodes are usually determined by the following well known formulas:

$$I = I_{sat}\exp\left(\frac{V_j}{nV_T}\right) \quad \text{giving} \quad R_j = \frac{nV_T}{I} \tag{1}$$

$$C_j = A\sqrt{\frac{q\epsilon N_d}{2(V_D - V_T - V)}} = \frac{C_{j0}}{\sqrt{1 - \frac{V_T}{V_D} - \frac{V}{V_D}}} \tag{2}$$

When the difference between the bias and the flat–band voltage is smaller than $3\,V_T = 3\,kT/q \sim 80\,mV$ at room temperature, eq. 1 and eq. 2 become invalid [1].

To avoid discrepancies between calculated and measured results some authors were forced to make unphysical assumptions like assuming that the flat–band voltage V_D equals the barrier height ϕ_b [2] and neglecting the V_T/V_D term in eq. 2 [3]. But these assumptions still do not solve the problem which results from the fact that under the so called flat–band condition, when the depleted layer disappears, the capacitance C_j becomes infinite, while the junction resistance R_j (eq. 1) is still finite and greater than zero. This phenomenon results from the approximations made in the derivation of eq. 1 and 2.

The examination of the I/V characteristics of the fabricated diodes shows that the dominating carrier transport mechanism is the thermionic field emission in the reverse bias and the thermionic emission and thermionic emission/diffusion for forward biases. In the frame of the diffusion theory, which determines the diode behavior near flat–band, eq. 1 is just an approximation of the solution given by the Dawson integral valid for $V \leq V_D - 4V_T$. A better approximation of this solution similar to that given already by

Schottky [4] is

$$I = I_{fb}\frac{1}{2\sinh\left(\dfrac{V_D - V}{nV_T}\right)} \quad \text{giving} \quad R_j = \frac{nV_T}{I}\tanh\left(\frac{V_D - V}{nV_T}\right) \tag{3}$$

In this bias range the depletion approximation utilized in the derivation of eq. 2 is also not valid any more and the space charge must be taken into account. This leads to a novel expression for the junction capacitance:

$$C_j = \frac{1 - \exp\left(\dfrac{V_D - V}{V_T}\right)}{1 - \dfrac{V}{V_D} - \dfrac{V_T}{V_D}\left[1 - \exp\left(\dfrac{V_D - V}{V_T}\right)\right]} \tag{4}$$

These expressions should be used if one wants to calculate the mixer performance when the diode is operating near flat-band conditions. They can be easily inserted into the generalised program, results of which are presented in this contribution. The actual program takes into account the current dependent recombination velocity, the field dependent mobility and electron heating at high forward bias. This program can therefore be efficiently used to calculate mixer or frequency multiplier performances enabling a more realistic analysis and optimization similar to the analysis given in [5].

The noise generating mechanisms in Schottky-barrier diodes are also well understood and are indicated in fig.1. The basic noise generating mechanisms are: a) shot noise in the junction with $i_j^2 = 2qI\Delta f$ and b) thermal noise in the series resistance with $e_s^2 = 4kT_0R_s\Delta f$.

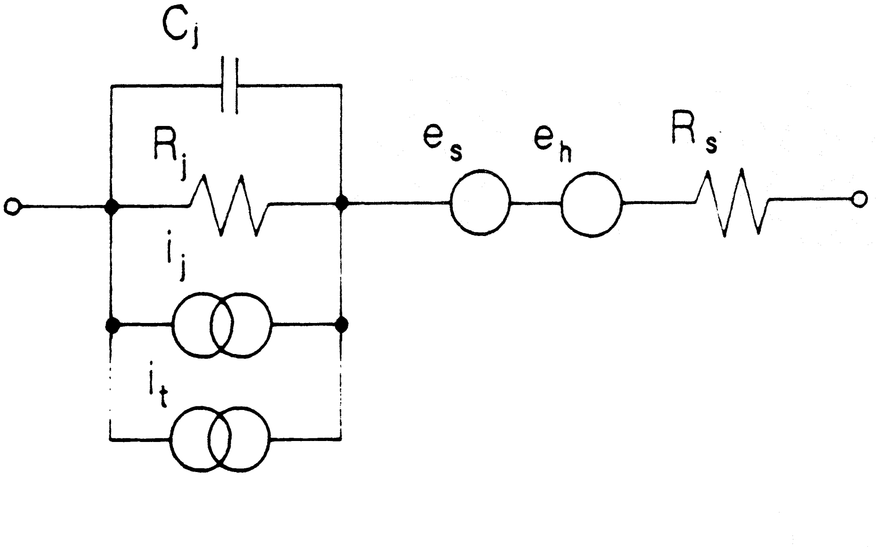

Figure 1: The equivalent circuit of the Schottky-barrier diode.

The well known expression first derived by Weisskopf in 1943 [6] gives the diode noise temperature for frequencies much lower than the junction cut-off frequency $\omega_j =$

$1/(R_jC_j)$.

$$T_n = \frac{nT_0}{2}\frac{R_j}{R_s + R_j} + T_0\frac{R_s}{R_s + R_j} \tag{5}$$

For higher forward biases and diodes with low doped epi-layers, electrons are heated by the high electric field in the undepleted epi-layer and the excess noise temperature T_h due to the increased electron temperature has to be added to the thermal noise [7, 8].

$$e_h^2 = 4kT_0K_hI^2R_s\Delta f \tag{6}$$

In some diodes an excess noise can be observed probably due to some trapping effects at the interface. This phenomenon has been described by [8, 9] and the noise source i_t should be added to i_j.

$$i_t^2 = 2\,I^2\,\frac{N_T}{N_D}\,\frac{\tau}{1 + (\omega\tau)^2} \tag{7}$$

where N_T is the concentration of presumed traps and τ is the time constant of this process.

The general expression to be compared with the experiment is then

$$T_n = \frac{nT_0}{2}\frac{R_j}{R_s + R_j} + \frac{C_T}{R_s + R_j} + T_0\frac{R_s}{R_s + R_j}\left(1 + K_hI^2\right) \tag{8}$$

where C_T and K_h are constants. If a good fitting is obtained with these 2 constants it means that the above simple model well describes noise generation mechanisms in measured diodes.

Diode fabrication

The first major requirement for *GaAs* Schottky diodes for mixing applications in the submillimeter frequency range is a small Schottky contact area in order to achieve junction capacitances in the low fF or even subfF region. Secondly, a homogeneous metal/semiconductor contact free of interfacial layers is required in order to achieve near-ideal electrical and noise performance. Since practical submm Schottky diodes have a metal/semiconductor contact area of less than 1 μm^2, the *GaAs* surface treatment and Schottky metal deposition techniques are much more important than for other semiconductor devices. Therefore, the fabrication of low-noise Schottky diodes requires an especially optimized device technology in order to avoid any damage to the *GaAs* surface. The diodes presented in this paper have been fabricated by applying a novel *GaAs* etching technique which is called anodic pulse etching [10, 11]. Since the initial fabrication steps such as SiO_2-deposition, ohmic backside contact and SiO_2-structuring are the same as commonly used, the main subject of the fabrication section will be the description of the anodic pulse etching in combination with the electrolytic *Pt* deposition for the formation of near-ideal small-area Schottky contacts.

For the fabrication of the diodes high-quality MBE-grown layers have been used [12]. Besides the diode diameter, thickness and doping concentration of these layers are the important process parameters for optimum device performance. Epitaxial layers having doping concentrations of $2 \cdot 10^{16}\ cm^{-3}$, $8 \cdot 10^{16}\ cm^{-3}$ and $2 \cdot 10^{17}\ cm^{-3}$ with an original epi-layer thickness of 200 nm have been used. In addition, one epi-layer with a graded doping profile has been used. This layer has a surface doping concentration of $2 \cdot 10^{16}\ cm^{-3}$ which is increased exponentially to $6 \cdot 10^{18}\ cm^{-3}$ within 90 nm. By controlled etching of the $GaAs$ surface, hence any surface doping concentration can be achieved.

After thinning the n^+-substrate to a thickness of 50–70 μm by mechanical lapping and polishing in order to reduce the substrate resistance, a 500 nm thick SiO_2 layer is deposited onto the epitaxial side by e-beam evaporation. The SiO_2 is necessary in order to avoid As outdiffusion during the following formation of the ohmic backside contact and finally separates the single Schottky diodes and serves as a mechanical guide for the whisker contact. The ohmic backside contact is formed by evaporation of $Ni/AuGe/Ni$ followed by a rapid thermal annealing step in H_2-atmosphere. Subsequently, the honeycomb diode structure is transferred to a photoresist layer on the SiO_2 by conventional UV-lithography. The structured photoresist serves as an etch mask for the reactive ion etching of the SiO_2. The applied RIE-process with CHF_3/O_2 assures highly anisotropic etching of the SiO_2. Thus, honeycomb structures with smallest hole diameters of 0.8 μm have been defined. The RIE-process is followed by a short dip in buffered HF in order to remove any possible SiO_2 residues.

The next step is the formation of the small-area Schottky contacts which is of course most important since it defines the quality of the Schottky contact. Because of the introduced $GaAs$ surface damage due to the SiO_2 e-beam evaporation and the plasma etching, it is necessary to remove some ten nanometers of GaAs before the deposition of the Schottky metal.

The etching step usually is performed by wet chemical etching [13, 14] or anodic oxidation of the $GaAs$ surface with subsequent dissolution of the anodic oxide in a Pt electrolyte [15]. Since wet chemical etching is isotropic it leads to an enlargement of the contact area and thus to larger junction capacitances. Furthermore, the etched GaAs surface is in contact with air, leading to the formation of a thin interfacial oxide layer. The anodic oxidation process allows the in-situ Pt plating avoiding these interfacial layers. The drawbacks of this technique are the rather isotropic etching and, as well as for the wet chemical process, the poor control of the etched depth. Nevertheless, the anodic oxidation process has become the standard technique for the fabrication of $GaAs$ Schottky diodes for submm applications.

The anodic pulse etching technique avoids the above stated problems [10, 11]. The principle of this technique is outlined below. The *GaAs* surface is brought into contact with a *Pt* electrolyte. The electrolyte/*GaAs* junction which behaves like a Schottky junction is driven into an Avalanche breakdown by the application of short voltage pulses. During the impact ionization in the space charge region electron–hole pairs are generated. The holes drift to the electrolyte/*GaAs* interface where they are essential for the anodic dissolution of *GaAs*. The short pulse width of 300 *ns* therefore enables an excellent control of the removed *GaAs* thickness by the number of applied voltage pulses. The short pulses are also essential for the anisotropic etching since saturation effects due to diffusion limited transport of reaction species are avoided. Since the solution for the anodic pulse etching is the same which is used for the electrolytic *Pt* deposition, the in–situ metallization is possible. The most important aspects of this technique are summarized below.

1. anisotropic etching ⇒ suitable for fabrication of submicron structures
2. excellent control and reproducibility ⇒ suitable for process–oriented modelling
3. in–situ metallization ⇒ suitable for fabrication of near–ideal Schottky contacts because surface damage and interfacial layers are avoided

By application of the anodic pulse etching technique, 100 *nm* of epitaxial *GaAs* have been removed, followed by the in–situ *Pt* deposition of 150 *nm* and a final electrolytic 150 *nm* thick *Au* deposition. After the formation of the Schottky junctions the samples are cut into single diode chips of $100 \cdot 100\ \mu m^2$.

I/V–, *C/V*– and noise characteristics at 1.5 *GHz* were recorded by whisker contacting the diode chips soldered to a *BeCu* whisker post. The whisker consists of a $15\,\mu m$ *AuNi* wire with an electrochemically etched tip. The whisker is soldered to another whisker post, which is mechanically advanced to the diode chip by a micromanipulator for contacting.

Experimental Results

Several Schottky diodes having different diameters, doping concentrations and doping profiles have been fabricated. All diodes show very good *I/V* characteristics in agreement with parameters predicted by the thermionic–field emission for reverse bias and ideality factors close to unity for forward bias. Fig.3 shows the measured and calculated values of the forward *I/V* characteristic of a Schottky diode with $1\mu m$ diameter and $2 \cdot 10^{17} cm^{-3}$ doping concentration. The higher value of the ideality factor are due to interfacial states and to thermionic–field emission for higher doping concentrations, as it can be inferred from fig.4 in which ideality factors of several diodes manufactured at the Technical University of Darmstadt and at the University of Virginia are presented as a function of doping concentration.

In fig.5 and 6 diode noise temperatures are presented. The diode examined in fig.5 does not exhibit any trap noise, however due to the low doping concentration, hot electron noise becomes appreciable at a relatively low current density, its characteristic being fairly well described by eq. 8 with negligible trap noise. The opposite situation can be inferred from fig.6. Noise originating from a mechanism described by eq.7 makes a major contribution and again the agreement between the measured and calculated values is excellent.

Noise measurements performed at 3 distinct frequencies give an estimation for the value of τ ($\tau \simeq 0.2ns$) corresponding to very shallow traps at the interface.

Noise characteristics of a diode with a graded doping concentration (fig.7) in the epi–layer exhibits the noise temperature similar to the diodes with moderate doping in the region of the diode operation and lower than that for the $1\mu m$ diode, but the increase of the noise temperature at higher current densities as is the case for highly doped diodes.

The $1\mu m$ diode has already shown excellent results in a $650GHz$ waveguide mixer at room temperature. A noise temperature smaller than $2000K$ and a corresponding conversion loss of $7.5dB$ have been obtained at an intermediate frequency of $4GHz$ [16]. These results are comparable to others obtained with smaller diodes. It is expected that the lower noise temperature in the operating current region of the $0.8\mu m$ diode with a graded doping profile in the epi–layer will enable to even improve these results.

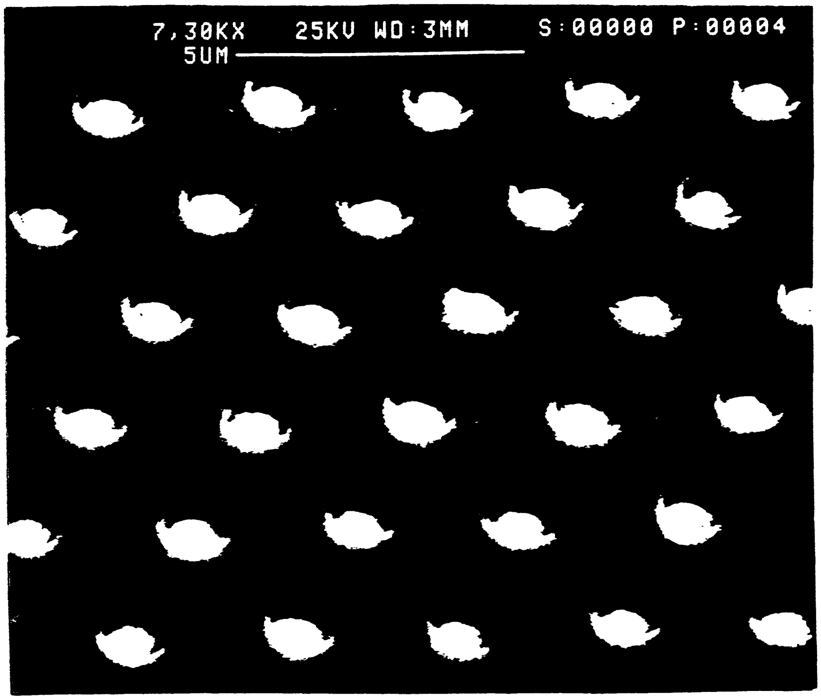

Figure 2: SEM photograph of the fabricated Schottky diode chip with $0.8\mu m$ diodes

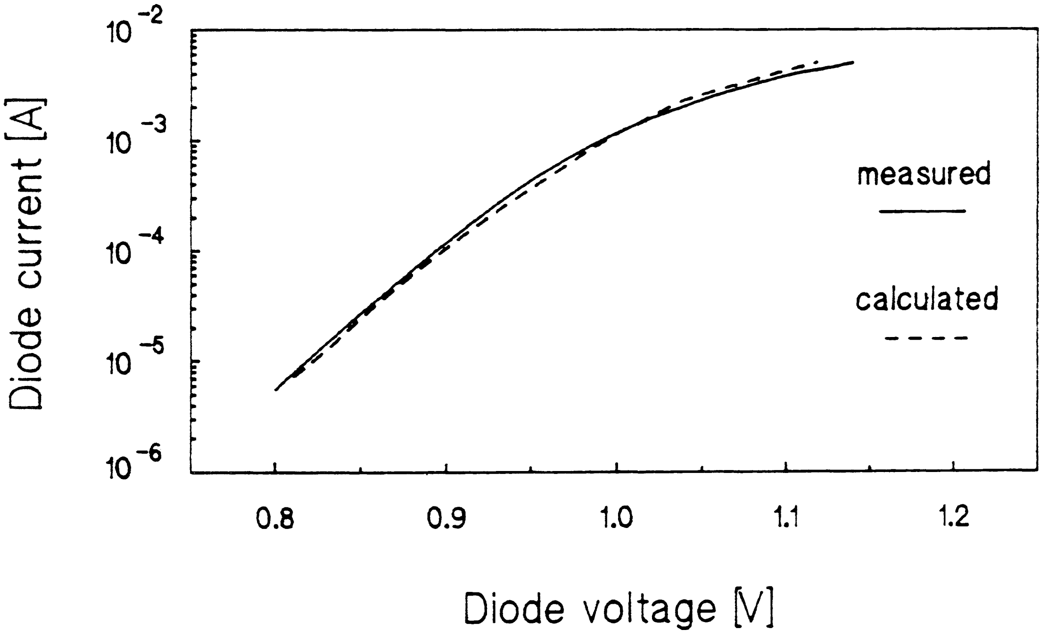

Figure 3: Measured and calculated values of the forward I/V characteristic for a diode with $1.0\mu m$ diode diameter and $2 \cdot 10^{17} cm^{-3}$ doping conctration.

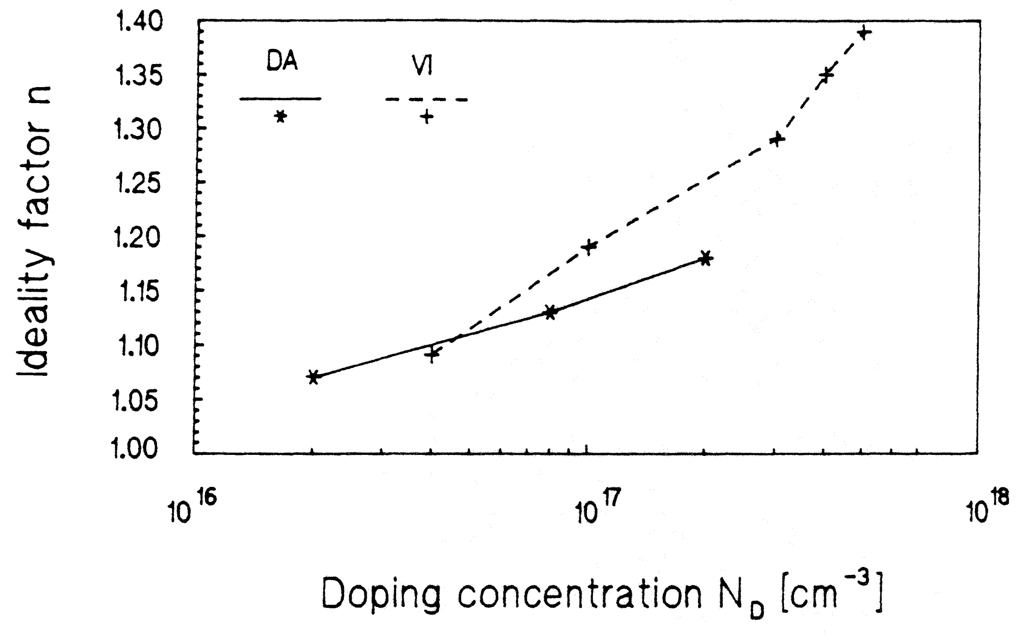

Figure 4: The ideality factor of Schottky-barrier diodes as a function of the doping concentration for diodes fabricated by the Technical University of Darmstadt (DA) and the University of Virginia (VI)

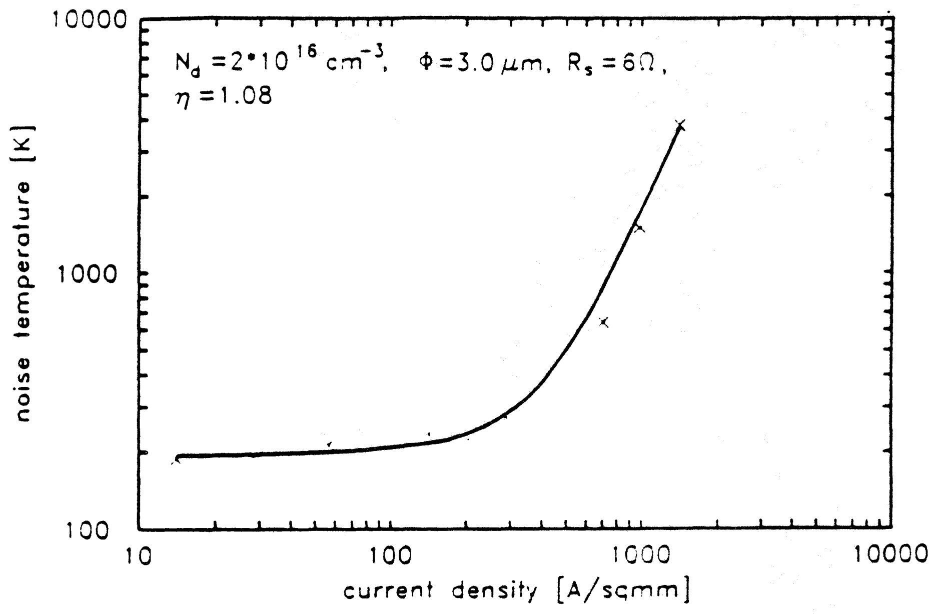

Figure 5: Comparison between measured and calculated (from eq. 8) noise characteristics of a low doped Schottky diode. The crosses indicated the measured data, the solid line stands for $T_n + T_h$ and the dotted line is $T_n + T_h + T_t$.

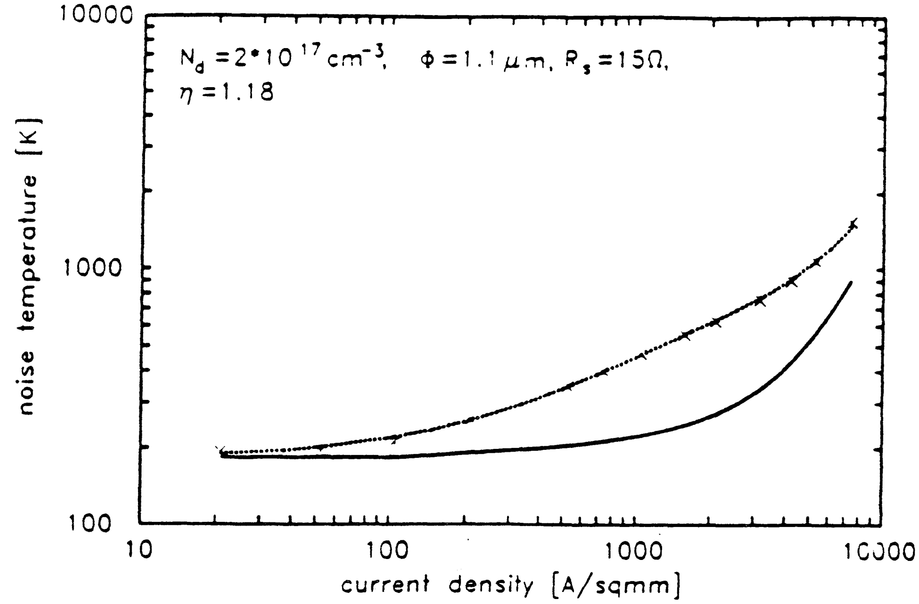

Figure 6: Comparison between measured and calculated (from eq. 8) noise characteristics of a highly doped Schottky diode. The crosses indicated the measured data, the solid line stands for $T_n + T_h$ and the dotted line is $T_n + T_h + T_t$.

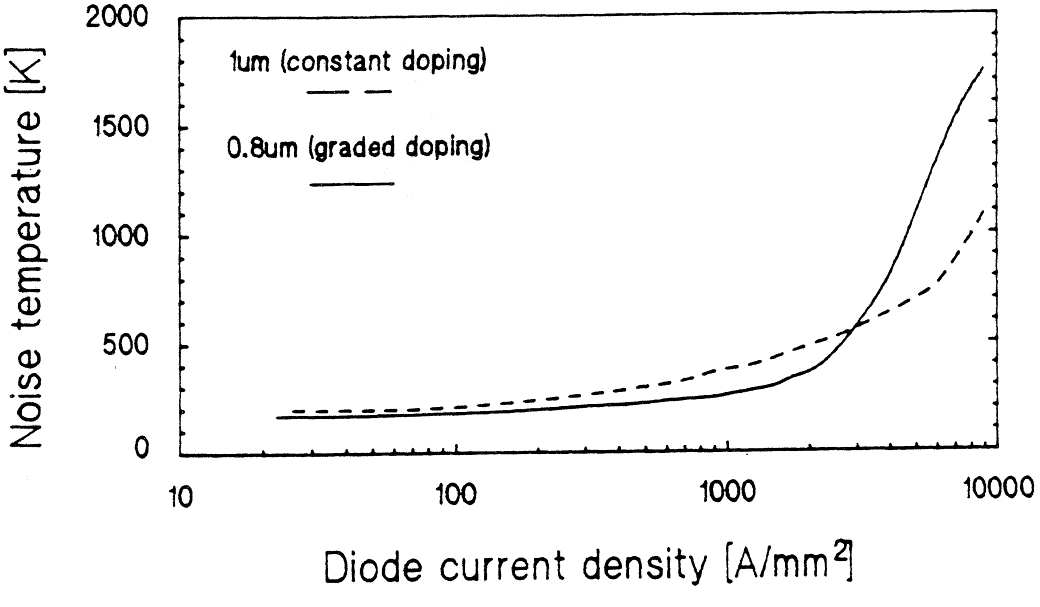

Figure 7: Noise characteristics of a 0.8μm diode with graded junction in comparison to the 1μm diode with constant ($2 \cdot 10^{17} cm^{-3}$) doping concentration

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