PLANAR THZ SCHOTTKY DIODE BASED ON A QUASI VERTICAL DIODE STRUCTURE

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Abstract

Whisker contacted GaAs Schottky barrier diodes are presently the standard devices for heterodyne mixing applications at THz frequencies. Due to reliability and handling problems and with regards to the recently proposed integrated antenna structures, much effort has been undertaken to develop planar whiskerless Schottky diodes. Recent approaches to planar diodes, based on FET–like structures, could not overcome the principal problems leading to a high parasitic shunt capacitance and a high series resistance. In this paper we present a novel approach for the planar diode concept. It is directly deduced from the vertical structure of the whisker contacted diode, making use of the many advantages and mature technology of the whisker contacted Schottky diode concept. On top of a mesa, the anode is connected with an airbridge to a contact pad. By means of via hole etching, the backside ohmic contact is connected with a contact pad at the surface. We have developed a technology for fabricating these diodes and describe the structure and the main technological aspects. Simulations have shown that in comparison to the recent approaches this concept shows some very promising features. In particular the minimum series resistance is comparable to the series resistance of the whisker contacted diode, due to the vertical current flow through the mesa, which is similar to the whisker Schottky diode structures operable at THz frequencies. This structure also exhibits a low parasitic shunt capacitance, due to a combined via hole and air bridge technology.

Introduction

For a variety of applications including radio astronomy, atmospheric studies and plasma diagnostics, heterodyne reception is the most promising technique in the Terahertz frequency range. There exist two different approaches to the realization of the nonlinear mixer element which is the key component of the receiver front end. The SIS device, which demonstrated record sensitivity at millimeter and long sub-millimeter wavelengths [1] and the GaAs Schottky barrier diode. Due to the required cryogenic cooling and a frequency limitation to about 700 GHz of SIS elements, GaAs Schottky barrier diodes are at the moment the most widely used mixer elements at submillimeter wavelengths and also in applications where cryogenic cooling is either too expensive or too heavy.

Whisker contacted Schottky barrier diodes have demonstrated excellent performance up to 2.5 THz [2]. They benefit from a minimum parasitic capacitance and a simple and highly mature fabrication. However, they are costly to assemble, show reliability problems due to the whisker contact and are impractical for systems using more than one diode. With the need for cheap and reliable mixer elements, the developement of planar Schottky diodes is an important topic of investigation. The essential drawback of these devices with respect to THz applications is the high parasitic capacitance and the increased series resistance compared to whisker contacted diodes.

In this paper we present a new approach to planar GaAs Schottky diodes which are designed for minimum parasitic capacitance and series resistance. The first section illustrates the design of the novel planar diode and gives an analysis of the parasitic resistance and the capacitance of FET–like planar diodes and the quasi–vertical diode. The second section describes the technological steps for the fabrication of the diode.

Concepts of planar diodes

In contrast to whisker contacted diodes an insulating substrate is used for planar diodes. The anode is connected to a contact pad by means of an air bridge. The common approach to the realization of planar Schottky diodes utilize FET–like structures [3]. Fig. 1 illustrates the structure. The ohmic contact pad is placed on the n^+–layer as closely as possible to the Schottky contact [3, 4]. The anode of the diode is contacted by an air bridge to the second contact pad.

The novel approach proposed in this contribution, is the quasi vertical structure il-

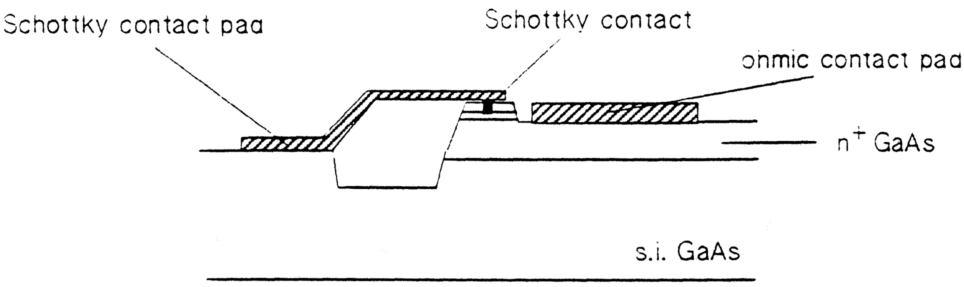

Figure 1: Structure of a FET–like planar diode

lustrated in fig. 2. This planar diode is directly derived from the whisker contacted diode. The Schottky contact is located on top of a small n/n^+ mesa. The mesa is placed on a metal island, forming the ohmic backside contact. The ohmic contact pad at the surface is connected to this backside metallization. The anode of this diode structure is also contacted by means of an air bridge to the second contact pad.

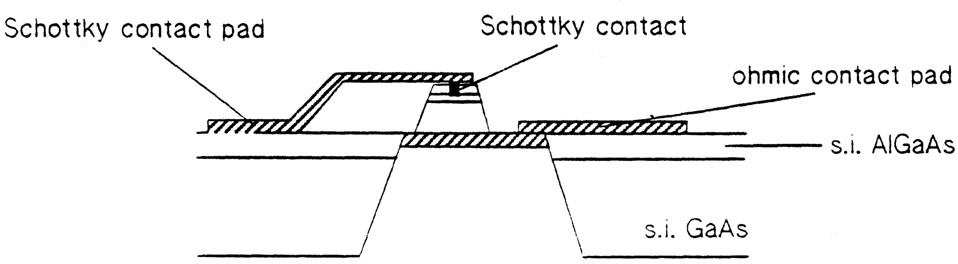

Figure 2: Structure of the quasi vertical planar diode

In the following sections, a comparison of the two concepts concerning the most important parameters for high frequency applications, the series resistance and the capacitance of the diodes, is presented.

With respect to future developements a possible resolution of 0.5 μm for the seperation between the Schottky and the ohmic metallization, an anode diameter of 0.5 μm

and a width of the air bridge of 1 μm have been assumed for the FET–like structure. For the quasi vertical diode a smallest mesa diameter of 2.5 μm, a possible via hole width of 2.5 μm, an anode diameter of 0.5 μm and a width of the air bridge of 1 μm have been chosen.

Analysis of the series resistance

The analysis presented here, gives an estimate of the parasitic resistance R_p for the two diode concepts. This resistance takes into account the ohmic contribution of the n^+ layer R_{n^+} and the ohmic contact resistance R_{con} between the n^+ layer and the ohmic contact pad. For the total series resistance the contribution of the epi layer R_n has to be added to R_p. R_n depends on the anode diameter and the thickness and doping concentration of the epi layer. Typical values of THz diodes for R_n are in the range of 10–20 Ω.

Integrated antenna structures for THz applications require the smallest possible structure size [3]. Due to the required reduction of the contact areas the influence of the parasitic resistance increases dramatically. For a realistic estimation a calculation of the R_p dependance on the structure dimensions has been made. It will be demonstrated that the influence of R_p is a limiting factor for the reduction of the planar diode structures.

For the calculation of R_{con} and R_{n^+} of the planar contact the following equations have been used [5]:

$$R_{con} = \frac{R_s\, L_T}{-2\pi R_b} \left\{ \frac{I_0\left(\frac{R_b}{L_T}\right) - \frac{I_0'(R_c/L_T)}{K_0'(R_c/L_T)} K_0\left(\frac{R_b}{L_T}\right)}{I_0'\left(\frac{R_b}{L_T}\right) - \frac{I_0'(R_c/L_T)}{K_0'(R_c/L_T)} K_0'\left(\frac{R_b}{L_T}\right)} \right\} \tag{1}$$

with

$$L_T = \sqrt{\rho_c / R_s} \tag{2}$$

I_0 and K_0 represent the modified Bessel functions of the first and second kind. R_b is the shortest distance between the center of the anode and the edge of the radial ohmic contact pad. R_c denotes the distance between the center of the anode and the far end of the ohmic contact pad.

$$R_s = \frac{1}{q\, N_{ds}\, \mu \min(d_{n^+},\, R_b)} \tag{3}$$

$$R_{n^+} = \frac{1}{2\,\pi\, q\, N_{ds}\, \mu\, R_a} \tan^{-1}\left(\frac{R_b}{R_a}\right) + \frac{1}{2\,\pi\, q\, N_{ds}\, \mu\, \delta_s} \ln\left(\frac{R_b}{R_a}\right) \tag{4}$$

Due to the vertical contact, the calculation of R_p for the quasi vertical structure is straight forward.

The following material and technological parameters have been used:

specific contact resistance	ρ_c	$5 \cdot 10^{-7}\, \Omega cm^2$
electron mobility	μ	$1500\ \frac{cm^2}{V\,s}$
doping concentration of n^+ layer	N_{ds}	$5 \cdot 10^{18}\, cm^{-3}$
thickness of n^+ layer (FET–like)	d_{n^+}	$1.5\ \mu m$
bridge width	L_g	$1\ \mu m$
anode diameter	R_a	$0.25\ \mu m$
skin depth at 1 THz	δ_s	$1.5\ \mu m$

Fig. 3 shows the results for a FET–like structure and a quasi vertical structure. For mesa heights smaller than the skin depth the effective contact area is not affected by the skin effect. Therefore, a mesa height of 1 μm has been chosen. It can be inferred that for all values of the structure width the parasitic resistance of the quasi vertical structure is smaller than that of the FET–like structure. The difference increases with a reduction of the structure width. For structure widths between 5 and 20 μm the difference between the two concepts is about 10 Ω. This lower series resistance would enable to reduce the typical epi–layer doping concentration of $1 \cdot 10^{18}\, cm^{-3}$ to $2 \cdot 10^{17}\, cm^{-3}$. A quasi vertical diode with the same series resistance as a FET-like diode therefore could achieve a lower ideality factor and a smaller junction capacitance. For both diodes a reduction below $\sim 2.5\, \mu m$ leads to a strong increase of R_p values which even exceed the epi–layer resistance. This is due to the rapid decrease of the contact area. Therefore, apart from the technological problems, the fabrication of diodes seems not to be reasonable with an overall structure width of less than $\sim 2.5\, \mu m$.The resulting high values of R_p ultimately limit the performance of both concepts.

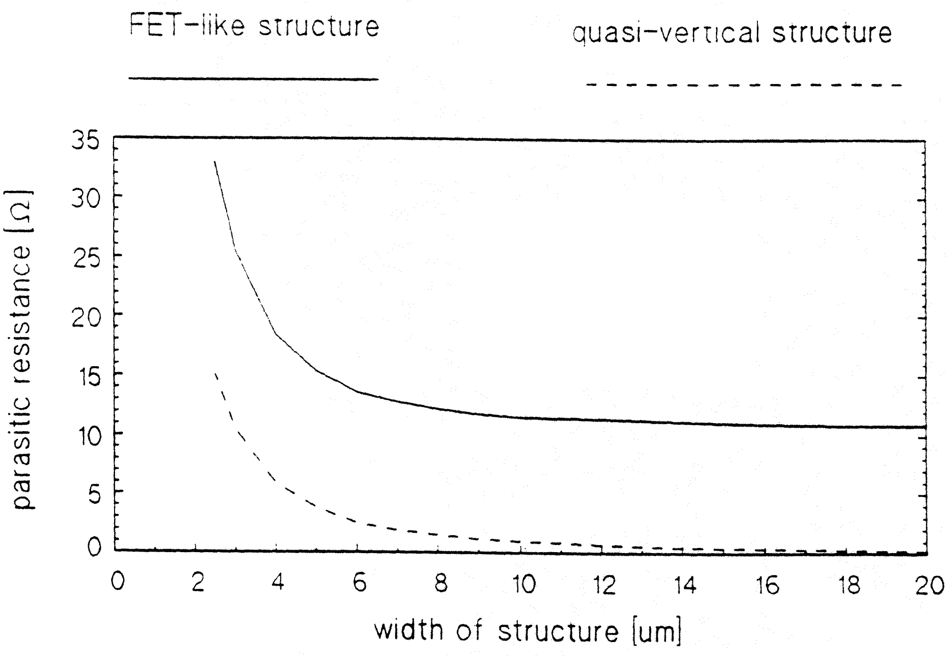

Figure 3: The parasitic resistance R_p for the two diode concepts as a function of the structure width

Analysis of the parasitic capacitance

The parasitic capacitance of the quasi–vertical structure is mainly determined by the area of the ohmic contact and the air bridge dimensions. In the FET–like structure, the main contribution to the parasitic capacitance originates from the small distance between the anode and the ohmic contact. A general–purpose 3–dimensional CAD finite–difference (F3D) program package has been developed for the calculation of passive microwave structures in the frequency domain and for static problems [6, 7]. The capabilities of the F3D CAD–package have been utilized for the calculation of the static parasitic capacitance of the quasi vertical diode structure. Based on these capabilities, simulations with varying dimensions have been carried out.

The main contribution to the capacitance of a single diode is caused by the contact pads. However, in typical applications this parasitic capacitance can be incorporated into the circuit design and is therefore generally less important. Giving an estimation of the performance of integrated diodes, the influence of these contact pads has been neglected. Assuming a via hole size of (mesa diameter)· (mesa diameter + 5 μm) the following capacitances depending on the mesa diameter, mesa height and air bridge length were calculated:

Mesa diameter [μm]	Mesa height [μm]	Bridge length [μm]	Capacitance [fF]
10	3	0	0.24
10	1	20	0.82
10	3	20	0.71
10	1	0	0.27
4	1	20	0.74
4	3	20	0.60
2	1	5	0.41
2	3	5	0.29
2	1	20	0.67
2	3	20	0.50

The decreasing mesa diameter and mesa height lead to a slight change of the parasitic capacitance. The length of the air bridge influences the capacitance to a much higher extent. However, the parasitic capacitance of this basic diode element does not exceed 1 fF and is comparable to the junction capacitance of a 0.5μm anode. This indicates that the total capacitance of the quasi vertical diode can be close to that of a whisker contacted diode. Simulations of the parasitic capacitance of FET–like structures show that there is no remarkable difference between the two planar diode concepts if the structure size is reduced.

Simulating a single quasi vertical diode with 50 $\mu m \cdot$50 μm contact pads, a 2μm anode, 50μm air bridge length and 5μm air bridge width we obtained a parasitic capacitance of 13 fF.

Technological Aspects

The fabrication process of the quasi–vertical diode is described in this section. The technological process is very similar to the fabrication of whisker contacted diodes, only the $GaAs$ material differs considerably. As substrate semi–insulating (s.i.) GaAs ($50 - 100\,\mu m$) is used. The epitaxial structure consists of a s.i. AlGaAs etch stop layer ($1\,\mu m$), a several micron thick and heavily doped epitaxially grown n^+–GaAs layer ($1 - 5\,\mu m$) and a thin epitaxial n–GaAs layer ($50 - 100\,nm$) at the top. A thin SiO_2 film is evaporated onto the top of the wafer, providing passivation of the surface for the following technological steps. Using AlGaAs as an etch stop layer, holes necessary for the backside ohmic contact are etched into the s.i. substrate. After a selective etching of the remaining AlGaAs an ohmic contact consisting of Ni/AuGe/Ni is formed to the n^+-layer followed by an annealing step and a subsequent Au plating (fig. 4). The n/n^+ mesa is defined using a HCl based etching solution (fig. 5). The

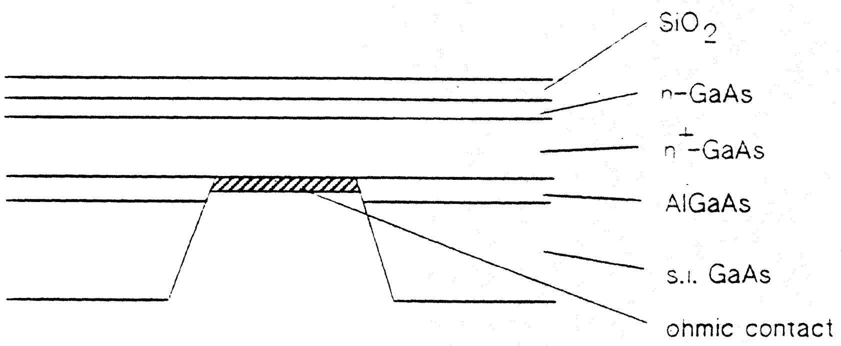

Figure 4: Structure with SiO_2 layer and ohmic contact

anode is formed by a RIE process with subsequent electrolytic Pt deposition (fig. 7). Then the air bridge and the contact pads are defined. The plating of the bridge and the contact pads completes the fabrication procedure (fig. 6). Fig. 8 and 9 show SEM photographs of the diode structure without the ohmic backside contact.

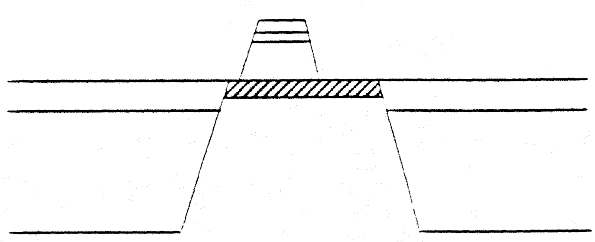

Figure 5: Definition of the mesa

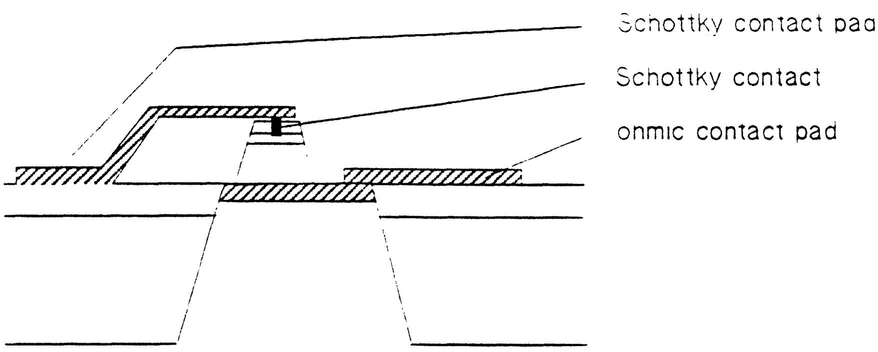

Figure 6: Quasi vertical diode

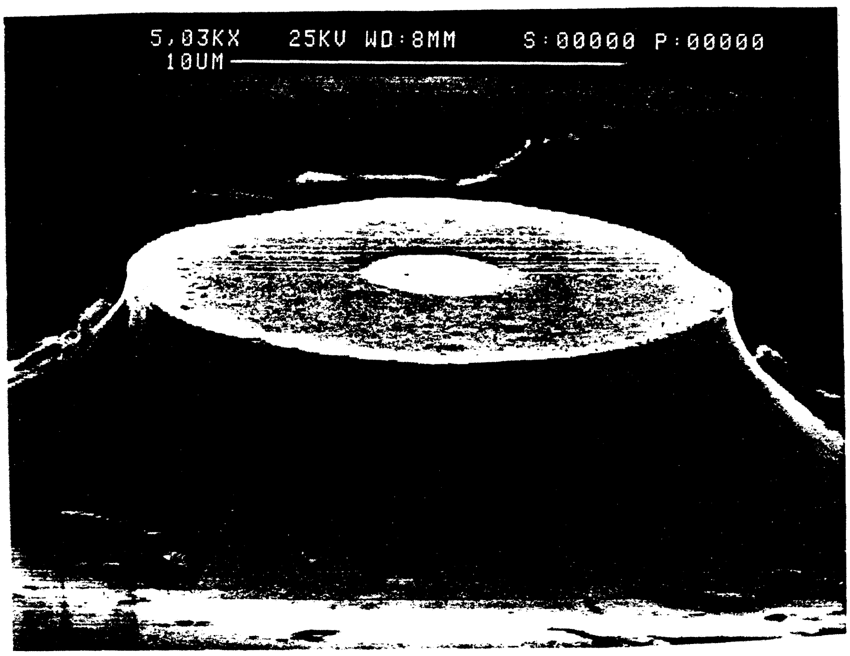

Figure 7: Mesa structure with 3 μm anode

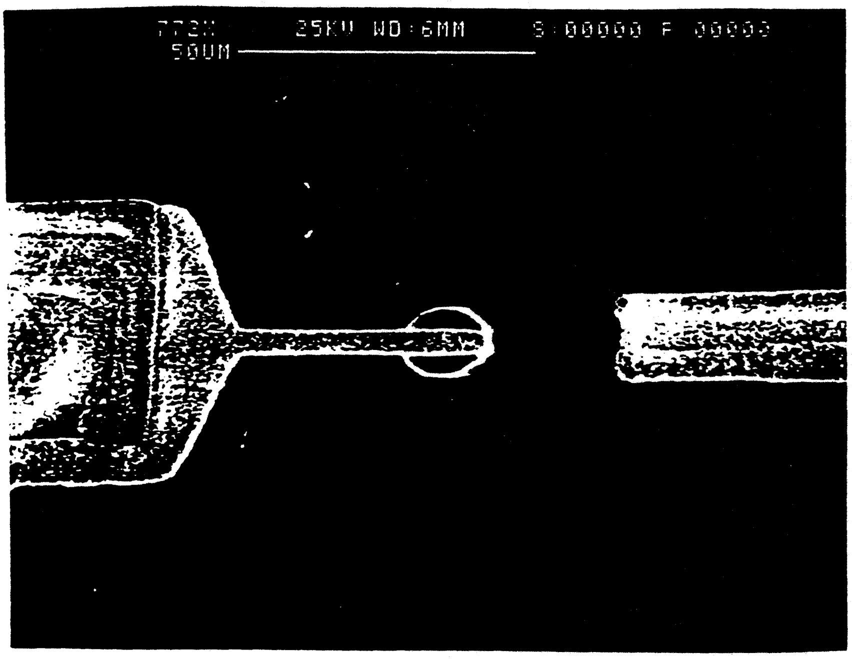

Figure 8: Top view of the diode with mesa (diameter 14 μm, height 5 μm) and air bridge (length 40 μm, width 4 μm)

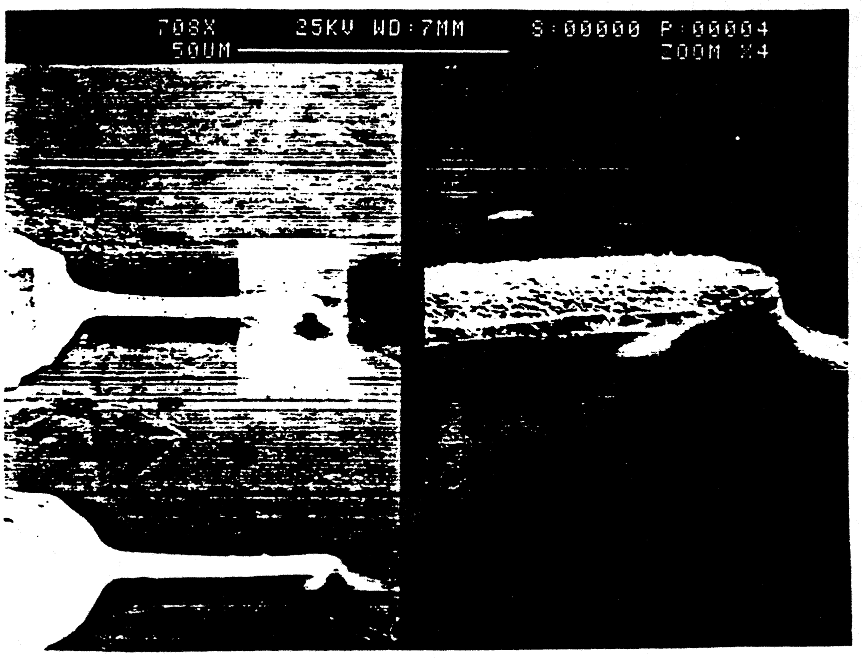

Figure 9: Side view of a diode with mesa (diameter 3.5 μm, height 5 μm and air bridge (length 40 μm, width 4 μm)

Conclusion

In this paper a novel approach has been presented for the realization of planar Schottky diodes suitable for operation at THz frequencies. The features of this structure as compared to the FET–like structure have been discussed in detail. Especially, the values for the parasitic diode capacitance and series resistance for both structures have been determined and a comparison reveals that the proposed novel structure exhibits a lower series resistance and similar shunt capacitance. The strong increase of the series resistance seems to be a limitation for the reduction of the total diode width below values of $\sim 2.5\,\mu m$. The simulations have shown that further technological improvements are necessary to reduce the shunt capacitance of planar structures to values which are comparable to whisker contacted diodes.

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