QUASI-OPTICAL 2-D JOSEPHSON JUNCTION ARRAY OSCILLATORS WITH ON-CHIP INDUCTIVE TUNING STRUCTURES

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ABSTRACT

Progress in understanding the mechanism of coherent oscillation in two-dimensional (2-D) Josephson junction arrays has been made through analysis of the coupling circuit between two Josephson junctions. For a 2-D array to oscillate in phase, capacitive coupling is required for adjacent junctions in the same row and inductive coupling for adjacent junctions in the same column of the array. Computer simulation has been developed for two junctions coupled through a general circuit to find the optimum coupling between two junctions. The junctions in the array are also integrated with inductive tuning elements to tune out the junctions' parasitic capacitance. We have built 2-D Josephson junction arrays but no coherent oscillation has yet been observed.

I. INTRODUCTION

A Josephson junction is a voltage tunable oscillator with typical voltage scales of mV and an oscillation frequency f_J = 484 GHz per mV of dc bias. It is a natural choice for a millimeter and submillimeter oscillator. Such an oscillator will find many applications, e.g., as a local oscillator for SIS receiver systems. There are several problems commonly associated with a single Josephson oscillator: very low output power, broad radiation linewidth, poor coupling between a Josephson oscillator and the outside world, and a large harmonic content in the oscillation. One solution to these problems is to use an array of junctions. Josephson junction array oscillators have been demonstrated at Stony Brook [1] and NIST [2].

Recently we proposed a new scheme of Josephson array oscillators [3]. It is a two-dimensional Josephson junction array with integrated coupling structures called the Quasioptical Josephson Oscillator (QJO). Fig. 1 shows a functional schematic of the QJO. The junction array is fabricated on one side of a substrate. The other side of the substrate is metalized to form a cavity behind the array. The cavity functions in two ways. In one way it provides a mean field to the array to lock all junctions in phase. In the other way it

tunes out the junctions' capacitance. Such distributed arrays have been fabricated but no coherent oscillation has been observed [4, 5]. Two possible problems are those of phase-locking and the junction parasitic shunt capacitance. The back mirror is proposed to tune out the junctions capacitance. But this requires the array to oscillate in phase. Therefore the local coupling circuit between junctions is crucial in determining the mutual phase-locking of the junctions in the array. On the other hand, the large capacitive shunt reduces the locking range dramatically even if the local coupling circuit makes the junctions locked in phase. The small locking range will be easily broken up by the noise in the system. One solution to this problem is to integrate junctions in the array with inductive tuning elements to tune out junction capacitances at one particular operating frequency. In this paper we discuss the coupling circuit for in-phase and out-of-phase locking between junctions and their implication to 2-D arrays, and the on-chip integrated tuning structures.

II. MUTUAL PHASE-LOCKING IN 2-D DISTRIBUTED ARRAYS

To solve the mutual phase-locking problem in 2-D distributed arrays is an immense task. As a first step we can look the mutual phase-locking of two junctions and infer the results to 2-D arrays. Here only high frequency electromagnetic coupling is investigated, and low frequency coupling associated with flux quantization is not considered in this paper.

A. Circuit model of two coupled junctions

A real tunnel junction can be modeled as a bare Josephson junction shunted by a parasitic capacitor and resistor. We apply a two port network to the circuit connecting the two junctions (as shown in Fig. 2). Here J_1 and J_2 are bare Josephson junctions with parasitic capacitors and resistors included in the two port network. In general a two port network can be represented by a Y-matrix:

$$Y = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix}$$

For a reciprocal two-port network the Y matrix is symmetric. The terminal currents are related to the voltages by the Y matrix:

$$I_1 = I_{11} + I_{12} = Y_{11} \times V_1 + Y_{12} \times V_2 \qquad (1)$$

$$I_2 = I_{21} + I_{22} = Y_{21} \times V_1 + Y_{22} \times V_2. \qquad (2)$$

An equivalent circuit described by (1) and (2) is the Π network as shown in Fig. 2 (b).

B. Phase relation of two weakly coupled junctions

Both perturbation analysis [6] and two-port network analysis [7] indicate that two resistively shunted junctions (RSJ's) will be locked in phase if they are coupled by a capacitor, and will be locked out of phase if they are coupled by an inductor (as shown in Fig. 3). To find the phase relation between two Josephson junctions through all the coupling range including strong coupling, we developed a computer simulation program. Some interesting results will be discussed below.

C. Computer simulation of two Josephson junction phase-locking

The algorithm for simulation of two junctions is an extension of the algorithm we developed for a single junction circuit [8]. We still use the harmonic balance method and update the voltage waveforms across the two terminals in the two-port network in each iteration. The following normalized variables are used in our computer simulation:

impedance:	$z = Z/R_N$
current:	$i = I/I_C$
voltage:	$v = V/V_N$, $V_N = I_C R_N$
capacitance:	$c = C/C_N$, $C_N = \Phi_0/I_C R_N^2$
inductance:	$l = L/L_N$, $L_N = \Phi_0/I_C$
time:	$t = T/T_N$, $T_N = 1/\Phi_0 I_C R_N$
frequency:	$f = F/F_N$, $F_N = \Phi_0 V_O$
power:	$p = P/P_N$, $P_N = I_C^2 R_N$.

Here I_C is the critical current of the junction, R_N is the normal state resistance of the tunnel junction, v_O is dc biasing voltage, and $\Phi_0 = 2e/h$ is the flux quantum. In normalized units, $f_J = v_O$ and the Josephson relations become:

$$i(t) = \sin(\phi(t)) \tag{3}$$

$$\frac{d\phi(t)}{dt} = 2\pi v(t). \tag{4}$$

For a typical niobium junction used in our arrays, the junction area A = 12 μm^2, I_C = 120 μA, R_N = 18 Ω, C = 456 fF. The normalization units for this junction are: V_N = 2.16 mV, C_N = 53 fF, L_N = 17 pH, F_N = 1045 GHz.

Simulation algorithm

1) Assume the junction voltage $v_{J1}(t)$ and $v_{J2}(t)$. We always set $v_{J1}(t) = v_{J1}(t) = v_O$ as the initial value, where v_O is the dc bias voltage.
2) Fourier transform $v_{J1}(t)$ and $v_{J2}(t)$ to $v_{J1}(\omega)$ and $v_{J2}(\omega)$.
3) Use the Fourier transform of the second Josephson relation (4)

$$j\omega\phi_1(\omega) = 2\pi v_{J1}(\omega)$$

$$j\omega\phi_2(\omega) = 2\pi v_{J2}(\omega)$$

to find $\phi_1(\omega)$ and $\phi_2(\omega)$.

4) Inverse Fourier transform $\phi_1(\omega)$ and $\phi_2(\omega)$ to $\phi_1(t)$ and $\phi_2(t)$.

5) Use the first Josephson relation (3) to find the junction current in the time domain $i_{J1}(t)$ and $i_{J2}(t)$.

6) Fourier transform $i_{J1}(t)$ and $i_{J2}(t)$ to $i_{J1}(\omega)$ and $i_{J2}(\omega)$.

7) Find the voltage across the two-port terminals

$$v_1(\omega) = (-i_{J1}(\omega))z_{11}(\omega) + (-i_{J2}(\omega))z_{12}(\omega)$$
$$v_2(\omega) = (-i_{J1}(\omega))z_{21}(\omega) + (-i_{J2}(\omega))z_{22}(\omega).$$

8) Compare $v_1(\omega)$ and $v_2(\omega)$ with $v_{J1}(\omega)$ and $v_{J2}(\omega)$. If the magnitude of the error is larger than the preset precision parameter, go back to step 3) and use $v_1(\omega)$ and $v_2(\omega)$ as $v_{J1}(\omega)$ and $v_{J2}(\omega)$. Otherwise the simulation is done.

In all the iterations, the dc component of the junction voltage is kept constant at v_O, the dc bias voltage. The initial phase of one junction is fixed at 0 as the phase reference and the phase of the other junction is allowed to vary. The second junction is current biased at i_{BIAS} and the phase is found by applying the following load line constraint:

$$\phi_{NEW}=\phi_{OLD} - p^*(i_{DC} - i_{BIAS})$$

where p is a positive constant, i_{DC} is the dc component of Josephson current, ϕ_{OLD} is the junction initial phase in current iteration and ϕ_{NEW} is the initial phase for next iteration.

Simulation Results

All simulations presented here were made at a fixed biasing voltage v_O=1 in normalized units.

1) Two coupled resistively shunted junctions

Our simulation results confirm our analysis above about the phase relation between two coupled resistively shunted Josephson junctions. Besides phase relations, the simulation also gives a quantitative locking range. For two mutually phase-locked junctions coupled by a capacitor, the dc currents through the junctions are depicted in Fig. 4. The horizontal axis in Fig. 4 is the phase difference between the two junctions. If we define the maximum allowable current difference between the junctions as the locking range ΔI, and the maximum allowable phase variation across the locking range as the phase span $\Delta\Psi$, we found that locking ranges are small at both weak and strong coupling. The maximum locking range is at intermediate coupling strength. Another interesting thing we found with the simulation is that the phase span $\Delta\Psi$ decreases with increasing coupling strength. Such locking behavior is depicted in Fig. 5 for two capacitively coupled resistively shunted Josephson junctions. The locking behavior for inductive coupled two

junctions is similar to that of capacitive coupled two except the phase difference is centered around π.

Another interesting thing we checked with the simulation is the pure resistively coupled two resistively shunted Josephson junctions. The locking range is zero for two identical junctions. The results we obtained are consistent with previous work [6, 9].

2) Two inductively coupled resistively-capacitively shunted junctions
Even though two inductively coupled resistively shunted junctions oscillate out of phase, the junction parasitic shunt capacitors change the two junction phase relation when they convert the inductive coupling to capacitive. A realistic circuit for two coupled tunnel junctions looks like that shown in Fig. 6. The simulation result for L = 4, $C_1 = C_2 = 8.6$ in the normalized units, which are typical parameters of Nb tunnel junction we used, showed that the phase difference between two Josephson junctions is around 0 at the center of locking range, opposite to the pure inductive coupling situation. The locking range is very small , $\Delta I = 1.4 \times 10^{-5}$, in this situation because of the large capacitive shunts.

Implication of the results of two junction mutual phase-locking to 2-D arrays
If the coupling circuit between two adjacent junctions in the same row of a 2-D array is right to have the two junctions locked in phase, the whole row will be locked in phase. The interesting thing here is that we need inductive coupling for the adjacent junctions in the same column of a 2-D array to lock in phase. This is the only situation a 2-D array will oscillate coherently. Any other situation, such as inductive coupling between two adjacent junctions in the same row or the capacitive coupling between two adjacent junction in the same column, will not have a 2-D array oscillate coherently.

III. On-Chip Integrated Matching Circuit

Various tuning structures have been used by people working on SIS mixers [10]. We mainly adapted these designs because we use the same tunnel junctions. The concern, however, is different. We are concerned about the effect of scattering of junction capacitances in the array. If the capacitance variation is δC, the resonant frequency will shift by $\delta\omega = (d\omega/dC)\delta C$. In design of tuning elements we want to ensure that the maximum resonant frequency shift due to the capacitance variation is within half of the 3 dB bandwidth of the resonant circuit. That is:

$$\delta\omega_{max} < \Delta\omega. \qquad (5)$$

Here we use $\delta\omega$ for resonant frequency shift due to the capacitance variation and $\Delta\omega$ for half of the 3 dB bandwidth of the resonant circuit. The interesting thing we found is that for a given δC, $\delta\omega$ scales with $\Delta\omega$. This scaling relation can proved easily as shown in the following.

A. Effect of junction capacitance scattering

In general a tuning circuit can be represented as $jB(\omega)$ in parallel with the capacitor it tunes out as shown in Fig. 6. The total admittance of the circuit including junction parasitic resistor and capacitor is:

$$Y_{total} = G + j\omega C + jB(\omega). \tag{6}$$

At resonance:

$$\omega_0 C + B(\omega_0) = 0. \tag{7}$$

To find the bandwidth of the circuit we consider the change of admittance with frequency:

$$\frac{dY_{total}}{d\omega} = jC + j\frac{dB(\omega)}{d\omega}. \tag{8}$$

With $\Delta\omega$ approximated by the change of admittance with frequency scaled by the real part of the admittance at resonant frequency:

$$\Delta\omega \approx \left| \frac{Re(Y_{total})}{\frac{dY_{total}}{d\omega}} \right|_{\omega=\omega_0} = \left| \frac{G}{C + \frac{dB(\omega)}{d\omega}} \right|. \tag{9}$$

Now assume the capacitance variation is δC, the resonant frequency shift can be found from eqn. (7):

$$(\omega_0 + \delta\omega_0)(C + \delta C) + B(\omega_0 + \delta\omega_0) = 0.$$

After expansion, we got:

$$\delta\omega_0 = \frac{1}{\omega_0} \left| \frac{\delta C}{C + \frac{dB(\omega)}{d\omega}} \right|. \tag{10}$$

The ratio of $\delta\omega_0$ and $\Delta\omega$ is:

$$\frac{\delta\omega_0}{\Delta\omega} = \frac{\omega_0 \delta C}{G} = Q\frac{\delta C}{C} \tag{11}$$

where $Q = \omega_0 C/G$. This result shows that a wider bandwidth tuning element has no advantage than a narrower bandwidth one in covering the resonant frequency shift due to the junction capacitance parameter scattering. But

wider bandwidth tuning structures do have advantage if we want larger tunability around the designed operating frequency. From equation (11), we can see that for given $\frac{\delta C}{C}$, if we want the resonant frequency shift no larger than half of the 3 dB bandwidth, there is a upper frequency limit for a given C or there is a upper capacitance limit for a given frequency.

B. Applicability of different tuning elements

Here we list in table 2 some tuning elements. All parameters are calculated for the HYPRES Nb fabrication process [11]. The parameters used to calculate transmission lines and 3 dB bandwidths are summarized in table 1.

Table 1. Parameters used in calculation of transmission lines and 3 dB bandwidths

Junction Capacitance	490 fF ± 5%
Gap Voltage	2.8 mV
Normal State Resistance	18 Ω
Physical Temperature	4.2 K
Center Frequency	100 GHz
Film Thickness of Bottom Electrode	150 nm
Film Thickness of Top Electrode	300 nm
Penetration Depth of Nb	90 nm
Thickness of Dielectric	200 nm
Dielectric Constant	4.7

Table 2. Different inductive tuning elements and their fractional bandwidths

Tuning Elements	Fractional Bandwidth
Lumped Inductor	18 %
Open-ended Stub	6.3 %
Short-ended Stub	14 %
End-loaded Stub	18 %

Essentially all the listed tuning elements can be use with 2-D arrays. The lumped inductor requires somehow a dc open circuit, which will make design more difficult. Among the listed tuning elements, the shorted-ended stub is a good choice. It has reasonably large bandwidth, and simple design when considering the coupling circuit. The end of the stub is RF shorted but

dc open. This can be achieved by using a quarter wave radial stub, which is a broad band short. Another tuning element we considered is the resistor-terminated stub as shown in Fig. 8. The advantage of this tuning circuit is that the termination resistor cuts the low frequency noise on the junction, and make the resonant steps easier to bias on. The tradeoff is the power loss to the termination resistor.

IV. TESTING RESULTS

2-D Arrays with capacitive coupling and on-chip resistor terminated tuning elements have been fabricated and tested. The optical micrograph of one of the arrays and the I-V curve are shown in Fig. 8 and Fig. 9. The adjacent junctions in the same row are coupled capacitively, and the coupling capacitor also serves to break the two junction SQUID loop. The I-V curve is close to that of a RSJ and showed a very slight bump corresponding to the resonant frequency 100 GHz of the tuning circuit. Using a liquid helium cooled bolometer, the output power from the arrays was determined to be less than 50 pW, indicating a lack of coherent oscillation. More analysis is under way.

V. CONCLUSION

For a 2-D array to oscillate in phase, capacitive coupling is required for adjacent junctions in the same row and inductive coupling for adjacent junctions in the same column of the array. Computer simulation of two coupled junctions showed that stronger coupling does not yield a larger locking range above a certain coupling strength. There is an optimal coupling strength which results in a maximum locking range. Integrating junctions in an array with tuning elements is a good solution to the parasitic capacitive shunt of junctions. For any inductive tuning structure, the resonant frequency shift due to capacitance variation is proportional to the 3 dB bandwidth of the tuning circuit.

ACKNOWLEDGMENT

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REFERENCES

[1] K. Wan, A.K. Jain, and J.E. Lukens, "Submillimeter wave generation using Josephson junction arrays," *Appl. Phys. Lett.*, vol.54, pp. 1805-1807, 1989.

[2] S.P. Benz and C.J. Burroughs, "Coherent emission from two-dimensional Josephson junction arrays," *Appl. Phys. Lett.*, vol.54, pp. 1805-1807, 1991.

[3] M.J. Wengler, A.Pance, B. Liu, and R.E. Miller, "Quasioptical Josephson Oscillator," *IEEE Trans. Magn.*, vol. 27, pp. 2708-2711, March, 1991.

[4] J. A. Stern, H. G. LeDuc and J. Zmuidzinas, "Quasi-optical josephson-junction oscillator arrays," *Proceedings of 1992 Applied Superconductivity Conference*

[5] B. Liu, M.J. Wengler and Arthur W. Lichtenberger, "Two Dimensional Josephson Junction Array Oscillators," to be published in *Digest of Technical Papers of the 17th International conference on Infrared and Millimeter Waves,*, December, 1992

[6] A.K. Jain, K.K. Likharev, J.E. Lukens, and J.E. Sauvageau, "Mutual phase-locking in Josephson junction arrays," *Physics Reports*, Vol. 109, pp. 309-426, 1984.

[7] B. Liu, "Mutual Phase-Locking of Two Josephson Oscillators due to High Frequency Coupling," Internal Report, Superconducting Electronics Group, University of Rochester, Feb., 1993

[8] B. Liu and M.J. Wengler, "Modeling of Quasioptical Josephson Oscillator," *IEEE Trans. on Applied Superconductivity*, Vol. 1, pp. 150-156, 1991

[9] M. A. H. Nerenberg, J. A. Blackburn and D. W. Jillie, "Voltage locking and other interactions in coupled superconducting weak links. I. Theory," *Physical Review*, B, Vol. 21, pp. 118 - 124, 1980.

[10] M. J. Wengler, "Submillimeter-wave detection with superconducting tunnel diodes," *Proc. IEEE*, Vol. 80, pp. 1810-1826, 1992.

[11] Niobium Design Rules, HYPRES Document Number 22-80601

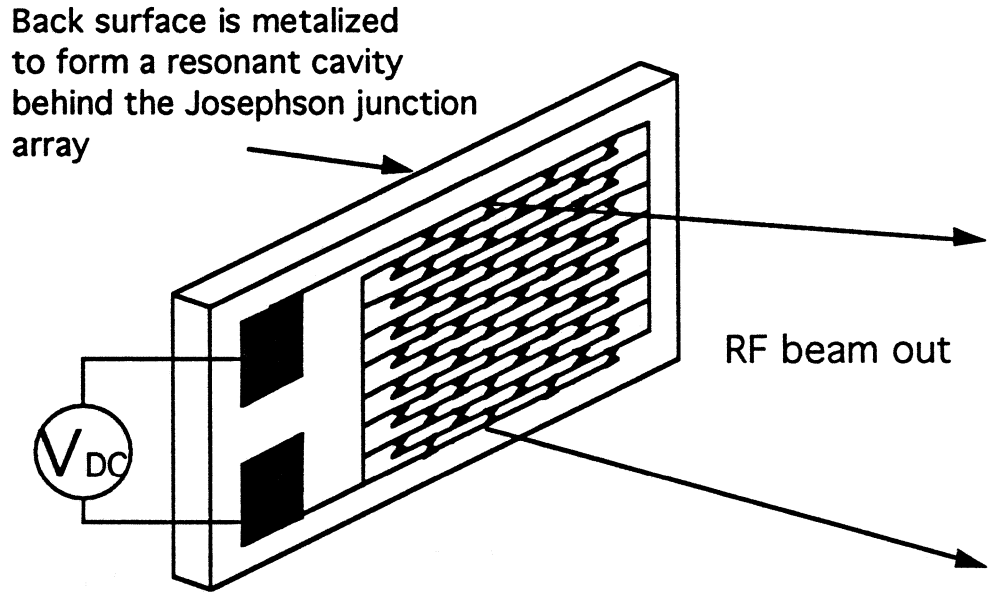


Fig. 1. A schematic design of the quasi optical Josephson oscillator with integrated bowtie antennas. There is one junction at the center of each bow-tie dipole antenna. The power is combined quasi-optically and coupled out from the broad side of the 2-D array of Josephson junctions. The dc wiring is shown so that all junctions are biased in parallel.

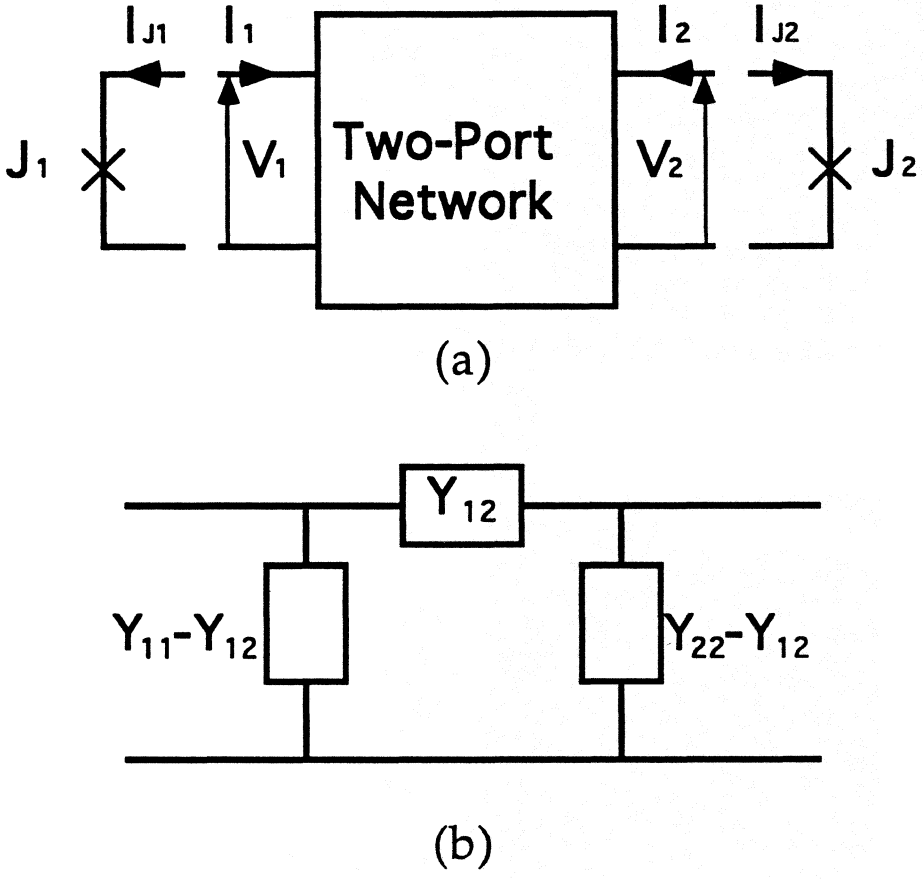
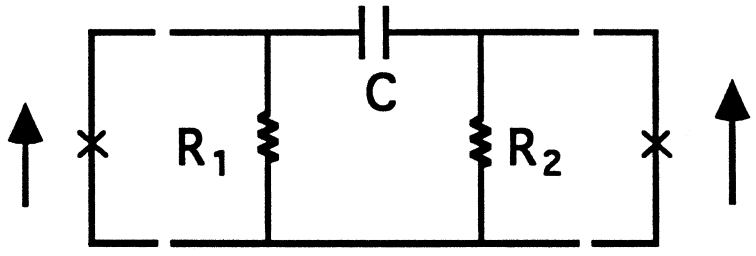
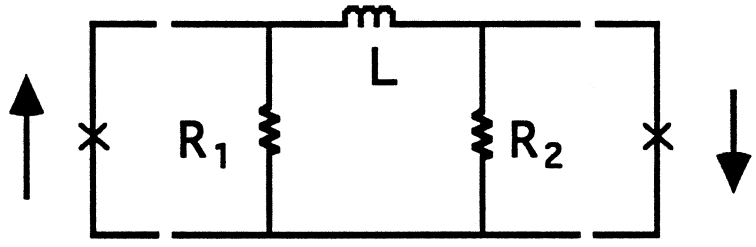


Fig. 2 Circuit model for two Josephson junctions coupled through a general complex circuit which is modeled as a two-port network (a), and the Π network equivalent circuit (b). Here J_1 and J_2 are bare Josephson junctions with parasitic capacitors and resistors included in the two port network.



$\phi_1 - \phi_2 \approx 0$ at center of the locking range

(a)



$\phi_1 - \phi_2 \approx \pi$ at center of the locking range

(b)

Fig. 3 Circuits of capacitively (a) and inductively (b) coupled two RSJs. The arrows indicate the Josephson current in the junctions. The ϕ_1 and ϕ_2 are phases of the two junctions respectively.

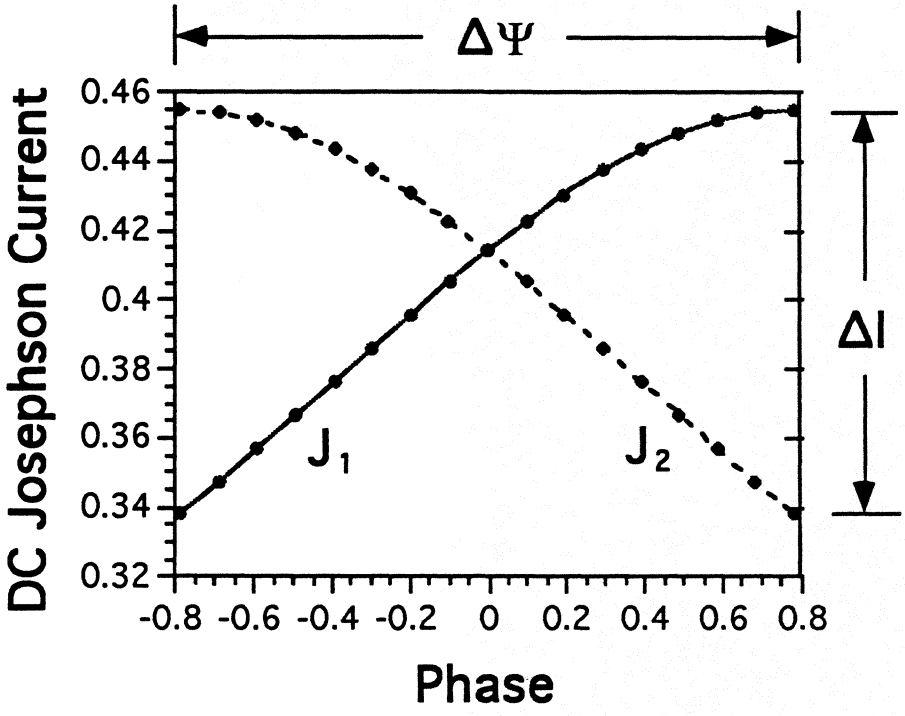


Fig. 4 The dc Josephson currents through two mutually phase-locked junctions by capacitive coupling versus the phase difference between the two junctions. The phase difference is $\Delta\phi = \phi_1 - \phi_2$. The locking range ΔI and the phase span across the locking range $\Delta\Psi$ are also shown in the graph.

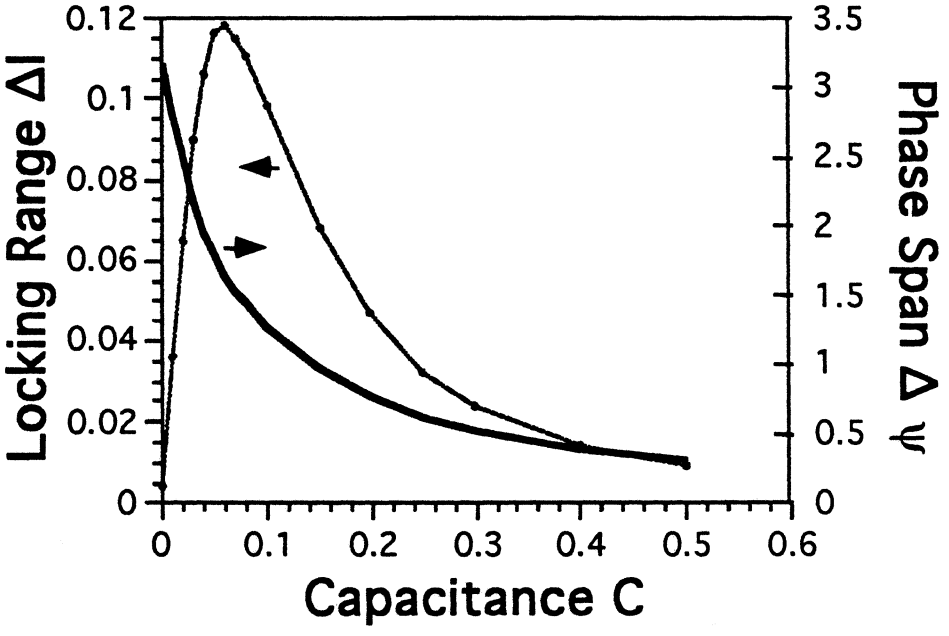


Fig. 5 The locking behavior for two capacitively coupled resistively shunted Josephson junctions as shown in Fig.4 (a). The left hand vertical axis is the locking range and the right hand vertical axis is the phase span across the locking range. Both ΔI and C are in the normalized units.

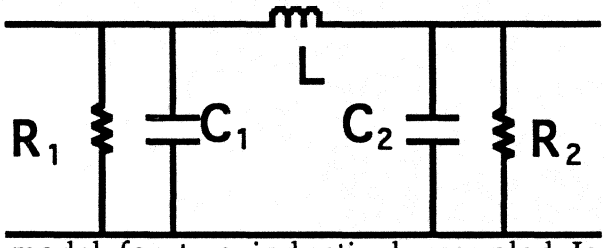


Fig. 6 Circuit model for two inductively coupled Josephson tunnel junctions. The ideal Josephson junctions are not shown.

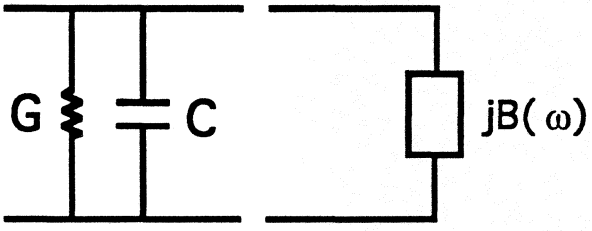


Fig. 7 The circuit model of a Josephson junction with an integrated tuning element. The G and C are the junction parasitic conductance and capacitance, and B(ω) is susceptance of the tuning element.

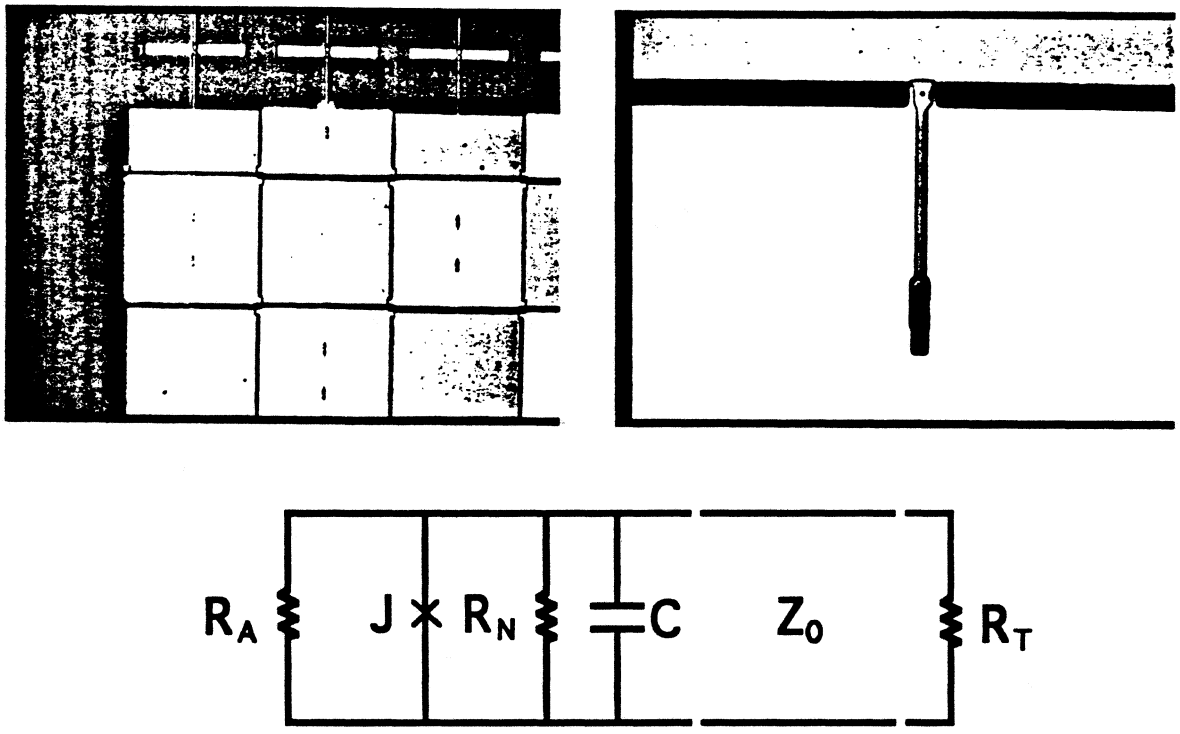


Fig. 8 Optical micrographs of a 2-D array of Josephson junctions with on-chip tuning elements fabricated at HYPRES, and the equivalent circuit of a unit cell in the array. There is a capacitor between two adjacent junctions to make the coupling between them capacitive. The tuning element is a resistor terminated microstrip transmission line. The Z_0 is the transmission line characteristic impedance, R_T the terminating resistor, R_N and C the junction parasitic resistance and capacitance, and R_A the antenna impedance.

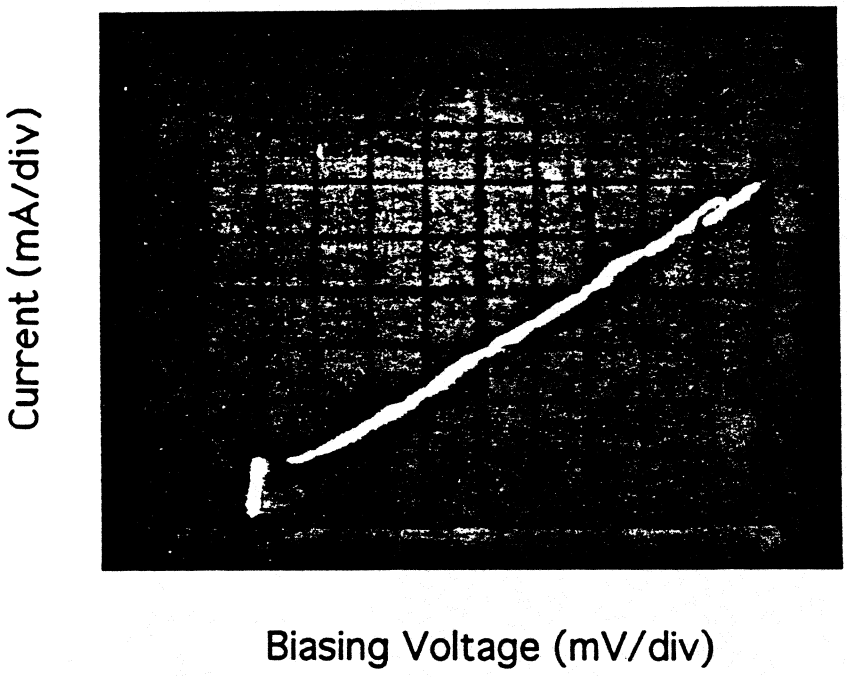


Fig. 9 I-V curve of a 2-D array of 14x14 Josephson junctions with on-chip resistor terminated tuning elements. The biasing scheme is that junctions in a same column are series biased, and all columns are parallel biased.