Effect of Parasitic Capacitance on the Performance of Planar Subharmonically pumped Schottky Diode Mixers

I. Mehdi and P. H. Siegel
California Institute of Technology
Jet Propulsion Laboratory,
Pasadena, CA 91109

ABSTRACT

Planar integrated Schottky diodes represent a robust alternative to whisker contacted diodes for space borne applications. However, compared to whisker contacted diodes, today's planar diodes possess larger values of parasitic capacitance. The effect of parasitic capacitance on the performance of a subharmonically-pumped antiparallel-pair planar Schottky-barrier-diode mixer is investigated. It is shown, that with appropriate design, one can obtain mixer performance from planar diodes that is comparable to the performance of low parasitic whisker contacted diode circuits at least up to 200 GHz.

I. INTRODUCTION

In recent years there has been a considerable amount of interest in utilizing planar integrated diodes in millimeter and sub-millimeter wave radiometers[1-5]. Perhaps the main driving force behind this interest has been the apparent reliability problems associated with whisker contacted devices in such risk prone systems as space-borne instruments. It is also hoped that by using an integrated device the rf circuit would attain some repeatability enabling one to optimally design the embedding circuit. Use of integrated devices also enables one to utilize circuit topologies requiring more than one diode since it is easier to fabricate a chip with two similar anodes than to design with two whisker contacted anodes.

The physical difference between an integrated whisker-less diode and a whisker contacted diode lead the two circuits to have different associated parasitics even though the metal-semiconductor contact is essentially the same. The nonlinear behavior of a mixer circuit makes the prediction of the effect of particular elements non trivial. In this paper the effect of parasitic capacitance and inductance on the performance of a 200 GHz subharmonically pumped mixer with anti-parallel pair Schottky diodes is investigated.

II. DEVICE AND CIRCUIT MODEL

A number of technologies are available that enable one to fabricate whisker-less planar Schottky diodes. In [6], some of these technologies, such as mesa etching and proton bombardment, have been discussed and it is concluded that due to the ease of fabrication and relatively low parasitics the Surface Channel Technology (SCT) presents the best potential. This technology has been developed at the University of Virginia and has been discussed in detail in [1,3,6,7]. In the SCT diodes, the Schottky anode is first contacted by a metal finger akin to an air bridge and then the anode and cathode pads are isolated by etching a channel in the highly doped semiconductor. Fig. 1(a) depicts a schematic of a planar SCT diode showing the various components of the parasitic capacitance. In a whisker contacted diode, the whisker is perpendicular to the anode and the capacitance between the whisker and the diode cathode is rather small [8]. The total shunt capacitance for a whisker diode has been reported to be as low as 1 fF [6]. However, in the planar device, the metal contact finger is horizontal to the anode and thus the parasitic capacitance between the metal finger and the semiconductor tends to be much higher. This parasitic capacitance has several components as shown in Fig. 1(a). C_{pp1} is the capacitance between the cathode and anode pad. C_{pp2} is the capacitance between the cathode pad and the n+ GaAs material under the Schottky anode. C_{pp3} is the capacitance between the two n+ GaAs regions of the device separated by the surface channel. Thus C_p which, we will call the parasitic capacitance from pad-to-pad, can be defined as $C_p=C_{pp1}+C_{pp2}+C_{pp3}$. C_f is defined as the capacitance between the anode contact finger and the n/n+ GaAs and we divide it into two components. C_{fp1} is the part of the capacitance that results primarily from the finger overlap on the anode pad, while C_{fp2} is the capacitance due to the overlap between the finger tip and the generally smaller anode. The total of C_{fp1} and C_{fp2} we will call C_f. The capacitance between the finger and the GaAs, is divided between C_{pp2} and C_{fp1}. It is assumed that since the finger gets closest to the GaAs around the Schottky anode most of the finger-to-pad capacitance should be accounted for by C_{fp1}. At high frequencies, these capacitances, especially C_{pp2}, are distributed, however in this study it has been treated as lumped elements and the equivalent circuit shown in Fig. 1(b) has been used.

Another important difference between the whisker contacted diode and the planar diode is the value of L_S. For whisker contacted diodes the whisker generally is fairly thick (10-20 microns) and the inductance per unit length is expected to be fairly small, although the whisker length tends to be large (100 microns or more). In integrated devices the fingers are typically 2-4 microns wide and perhaps a micron thick. This causes the integrated device to have non-negligible inductance even though it is very short (10-50 microns). This inductance is of paramount interest because of the role it plays in the subharmonic mixer circuit where it has been shown [9,10] that the loop inductance causes the mixer circuit to resonate with the chip capacitance.

For this analysis the semiconductor-metal junction (Schottky anode) is modeled in the usual way as a nonlinear capacitor in parallel with a nonlinear resistance. The capacitance and resistance of the device are related to the semiconductor doping, epi-layer thickness and anode geometry. R_s is the parasitic series resistance associated with the undepleted epi layer, n+ GaAs and the ohmic contact. This resistance is assumed to be constant with voltage. The diode I-V relationship is assumed to follow the standard thermionic emission theory. The capacitance of the diode is given by

$$C_j(V)=C_{j0}\left(1-\frac{V}{\varphi_b}\right)^{-\gamma},$$

where V is the applied voltage, C_{j0} is the zero bias capacitance, γ is 0.5, and φ_b is the barrier height.

In order to accurately simulate the performance of a mixer with the circuit of Fig. 1(b) it is essential to use circuit parameters that are consistent with presently available device technology. The total measured capacitance for an anti-parallel pair diode chip can be written as

$$C_{tot}=C_j+C_j+C_p+C_f+C_f,$$

where finger to finger capacitance is assumed to be small and has been neglected. C_{tot} can be directly measured with a capacitance bridge on the actual circuit. The junction capacitance, C_j, can be extrapolated by measuring the total capacitance of various size anodes with all other geometrical parameters a constant. C_p can be measured by knocking off the fingers on a chip and measuring the capacitance across the contact pads. To distinguish between C_p and C_f we have made devices with metal fingers but no anode contact. Measuring the total capacitance of such a device and then subtracting the C_p gives us an upper limit to C_f.

The parasitic capacitance is dependent on a number of fabrication parameters. The surface channel width, the finger width, finger length, the GaAs pad sizes, and the quality of the dielectric constant will all effect the C_{tot}. These parameters can vary considerably from laboratory to laboratory and even from batch to batch. Typical values of C_p range from 3 fF to 12 fF. Typical values for C_f range from 0.7 fF to 3 fF. Based on this data a reasonable parameter space can be defined which would encompass present day diode fabrication technology. The correct value for the finger inductance remains a bit uncertain till direct measurements can be successfully conducted. The model measurements of [11] give the finger inductance as 0.53 pH per micron plus 18 pH attributed to fringing current inductance associated with the abrupt change in metallization width. Thus for a finger that is 50 microns long the total inductance according to [11] would be about 45 pH.

III. MIXER SIMULATIONS

The circuit used for the subharmonically pumped mixer is shown in Fig. 2(a) [9,10]. The planar diode is represented with the equivalent circuit of Fig. 1(b). The diode electrical characteristics have been discussed earlier and it is assumed that both diodes are identical and are connected with opposite polarity so they conduct on alternate half-cycles of the local oscillator (LO). For even harmonics and DC the diodes are out of phase and thus produce zero voltage across Z_3. This is shown in Fig 2(b). For odd harmonics the circuit of Fig. 2(a) simplifies to the circuit of Fig.

2(c). During simulations, all linear elements are incorporated into the embedding network as shown in Fig. 2(a) and Z_3 represents the source or load impedance. The IF load Z_3(IF) is conjugate matched to the output impedance of the mixer. The embedding impedance is set to 50 Ohms for the first and second harmonics while at other harmonics a short circuit is assumed.

The mixer simulation that has been developed follows the procedure described by Kerr in [9,10]. Obviously the admittance matrix of the mixer is slightly different from the admittance matrix developed in [10] because of the addition of the parasitic capacitance. The admittance matrix of the mixer circuit of Fig. 2 (a), taking into account the parasitic capacitance, is as following:

$$Y = \begin{bmatrix} Y_{11} & 0 & Y_{13} \\ 0 & Y_{11} & Y_{13} \\ -Y_{11} & -Y_{11} & Y_{33} \end{bmatrix}$$

where

$$Y_{11} = \frac{1-\omega^2 L_s C_f}{R_s-\omega^2 R_s L_s C_f+j\omega L_s}$$

$$Y_{13} = \frac{1-\omega^2 L_s C_p+j\omega[R_s C_f+R_s C_p-\omega^2 C_p R_s C_f L_s]}{R_s+j\omega L_s-\omega^2 R_s L_s C_f}$$

$$Y_{33} = -Y_{13}-Y_{23}+\frac{1}{Z_3}$$

The mixer simulation assumes that both diodes are identical and only eight harmonics of the LO are considered. The rectified current in the diodes is set at 1 mA and the LO power is varied to obtain the desired current flow. LO, signal and IF are 108, 216 and 1.4 GHz respectively. Fig. 3

shows the effect of C_p on the performance of the subharmonic mixer for a diode with ideality factor, η=1.25, saturation current Is= 2.5E-16 A, barrier height φ_b=1.10 V, series resistance R_s=12 Ω and zero bias junction capacitance C_{jo}=3 fF. The single sideband (SSB) conversion loss, input noise temperature and the real part of the IF output impedance are plotted as a function of the finger inductance, L_s, present in the circuit. One can clearly observe that the mixer performance is a strong function of the loop inductance. The observed peaks in the conversion loss and noise temperature occur at even harmonics of the LO when the loop inductance resonates with the device capacitance. Note that the resonance is getting broader as C_p is increased from 0 fF to 12 fF. As is evident from the equivalent circuit in Fig. 2, as C_p increases it essentially provides a short for the RF power. Fig. 3(b) shows the effect of C_f on the mixer performance in the absence of C_p. The main effect of increasing C_f is to reduce the value of the inductance necessary for resonance thus restricting the values of loop inductance that can be tolerated.

Figure 4 shows the mixer performance for an identical circuit with a diode whose series resistance has been halved to 6 Ohms and whose zero bias junction capacitance has been doubled to 6 fF (maintaining a constant RC product). Figure 4(a) shows the effect of C_p on this mixer. Again, the resonance is broadened but now they occur at smaller values of L_s as compared to Fig. 3(a). Fig. 4(b) shows the effect of C_f on the mixer. As before, increasing C_f moves the resonance towards smaller values of L_s, thus restricting the range that can be tolerated.

Figure 5 shows the computed mixer performance, using a diode with R_s=12 Ohms and C_{jo}=3 fF, for two different sets of parasitic values. The solid curve shows a circuit whose parasitic capacitance is zero, approximately simulating a whisker contacted diode. The dashed curve uses a

C_p of 4 fF and C_f of 1 fF simulating a planar SCT diode, which in fact has been tested as a 200 GHz subharmonic mixer [3]. From Fig. 5 it can be seen that for a loop inductance below 45 pH the performance of the planar diode mixer and the whisker contacted diode are similar at least up to 200 GHz.

An exact comparison with experimentally obtained mixer results is not possible due to a lack of measurements on the actual value of L_s. The performance of whisker contacted diodess and planar diodes with similar characteristics in fundamental mixers is now equivalent up to 300 GHz [7,12]. Similarly, it has been shown that at least up to 200 GHz, planar diode subharmonically pumped mixer perform as well, if not better than, their whisker contacted counterparts [3].

IV. CONCLUSION

The equivalent circuit of a planar SCT Schottky diode chip with two diodes in anti-parallel configuration has been used to study the effect of parasitic capacitance on the mixer performance. The model incorporates realizable values of the parasitic capacitance that have been reported previously. Based on computer simulations it is shown that reasonable values of the parasitic capacitance can be tolerated at least up to 200 GHz as long as the loop inductance is low enough so that it does not resonate with the device capacitance. This study also stresses the need for measuring or precisely calculating the inductance associated with the planar device.

V. ACKNOWLEDGEMENT

The research described in this talk was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

REFERENCES

1 D. Garfield, R. Mattauch, and S. Weinreb, "RF Performance of a Novel Planar Millimeter-Wave Diode Incorporating an Etched Surface Channel," IEEE-MTT , vol. 39, no. 1, pp.1-5, January 1991.

2 T. Newman, W. L. Bishop, K. T. Ng, S. Weinreb, "A Novel Planar Diode Mixer for Submillimeter-Wave Applications," IEEE-MTT vol. 39, no. 12, pp. 1964-1971, December 1991.

3 P. H. Siegel, R. J. Dengler, I. Mehdi, J. E. Oswald, W. Bishop, T. Crowe, and R. J. Mattauch, "Measurements on a 215 GHz Subharmonically Pumped Waveguide Mixer using Planar back-to-back Air Bridge Schottky Diodes," IEEE-MTT Vol. 41, No. 11, November 1993.

4 T.-H. Lee, PhD dissertation, University of Michigan, May 1994.

5 P. H. Siegel, I. Mehdi, R. J. Dengler, J. E. Oswald, A. Pease, T. W. Crowe, W. Bishop, F. Li, R. J. Mattauch, S. Weinreb, J. East and T. H. Lee, "Heterodyne Radiometer Development for the Earth Observing System Microwave Limb Sounder," SPIE Conference Proc. #1847-Infrared and Millimeter-Wave Engineering, May 1993.

6 W. Bishop, K. McKinney, R. Mattauch, T. Crowe, and G. Green, "A Novel Whiskerless Diode for Millimeter and Submillimeter Wave Applications," 1987 IEEE-Int. Microwave Symposium Digest, pp. 607-610, June 1987.

7 R. J. Mattauch, et. al., "Recent results on : Surface-channel Schottky, InGaAs Schottky, and Nb based SIS mixer element research," First International. Swamp. on Space Terahertz

Technology, p. 279, March 1990.

8 A. R. Kerr, J. A. Grange, J. A. Lichtenberger, "Contact whiskers for millimeter wave diodes," NASA Technical Memorandum no. 79616, Goddard Space Flight Center, Institute for Space Studies, Aug. 1978.

9 A. R. Kerr, "Noise and Loss in Balanced and subharmonically pumped mixers: Part I--Theory," IEEE-MTT, vol. 27, no. 12, December 1979.

10 A. R. Kerr, "Noise and Loss in Balanced and subharmonically pumped mixers: Part II--Application," IEEE-MTT, vol. 27, no. 12, December 1979.

11 R. T. Newman, Jr., PhD dissertation, University of Virginia, August 1991.

12 T. Newman, W. L. Bishop, K. T. Ng, and S. Weinreb, " A novel planar diode mixer for submillimeter-wave applications," IEEE-MTT vol. 39, no. 12, pp.1964-1971, December 1991.

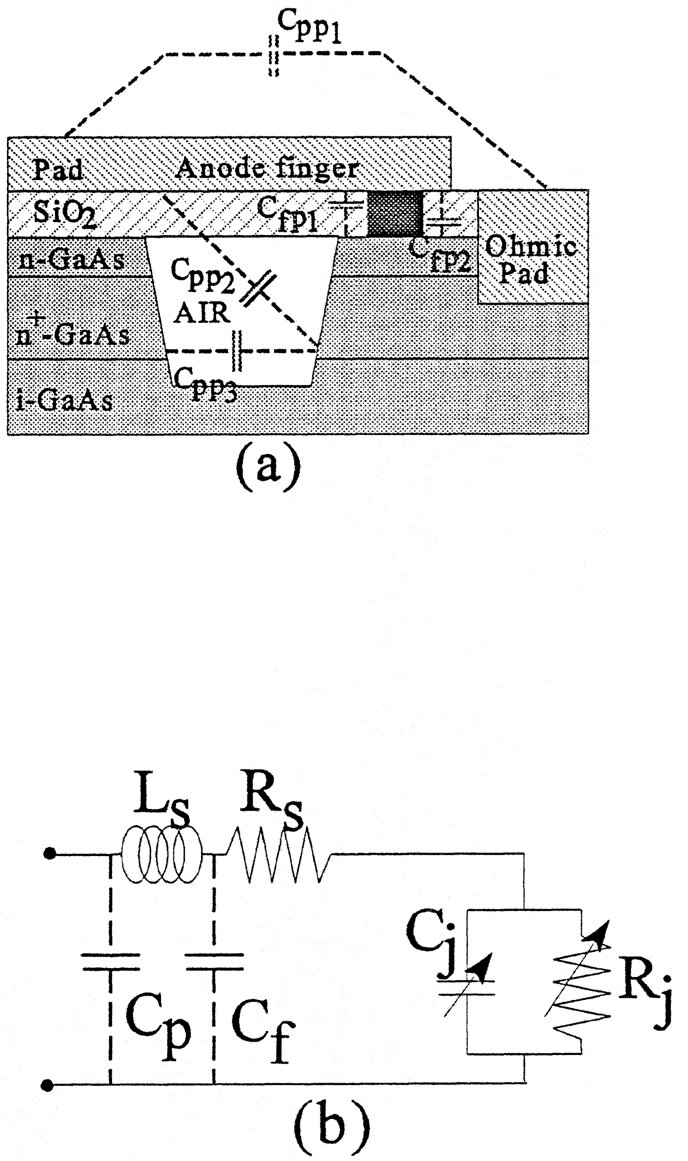


Figure 1: (a)Schematic of a planar integrated Schottky diode chip using Surface Channel Technology. (b) A representative equivalent circuit using lumped elements. C_p=C_{pp1}+C_{pp2} +C_{pp1} and C_f = C_{fp1}+C_{fp2}.

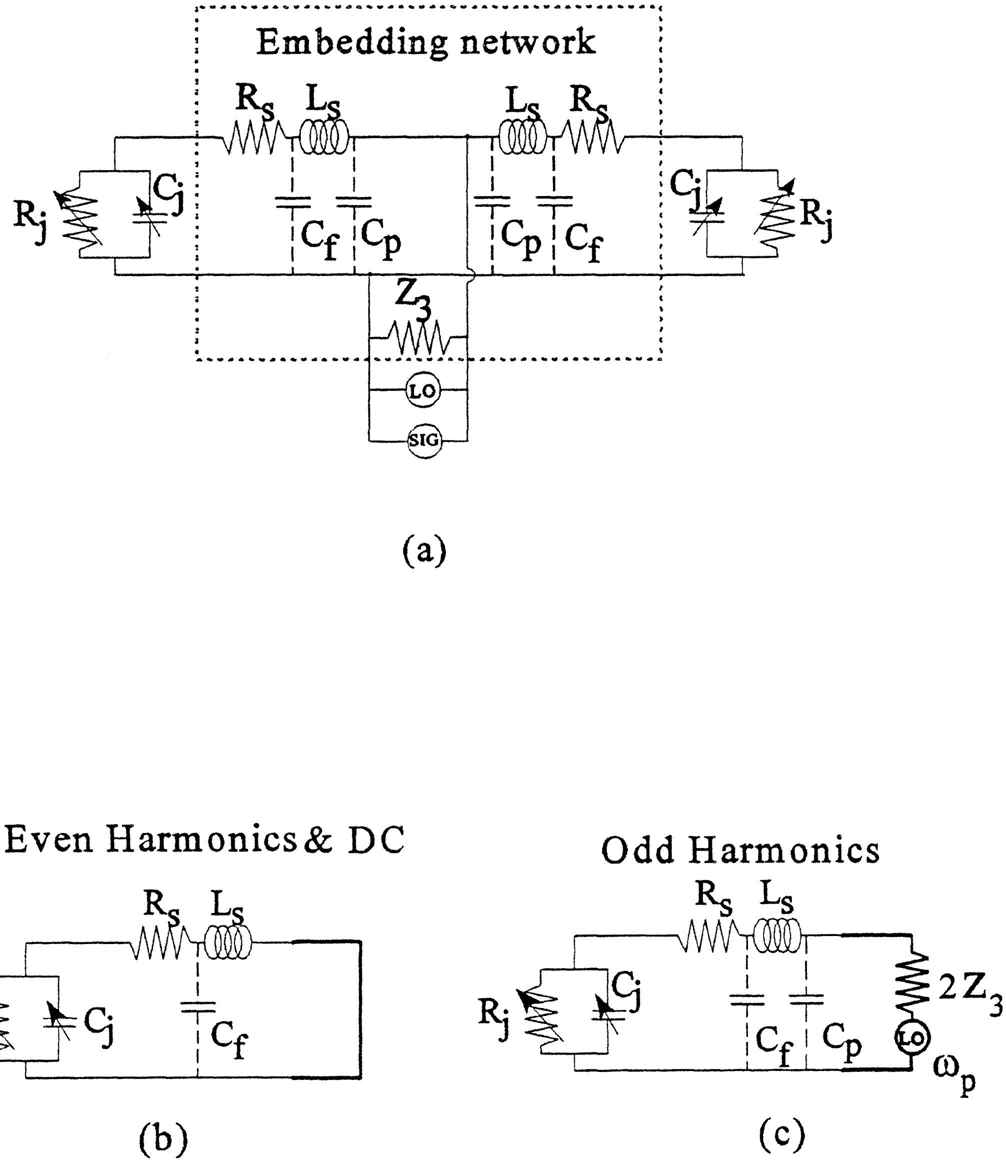
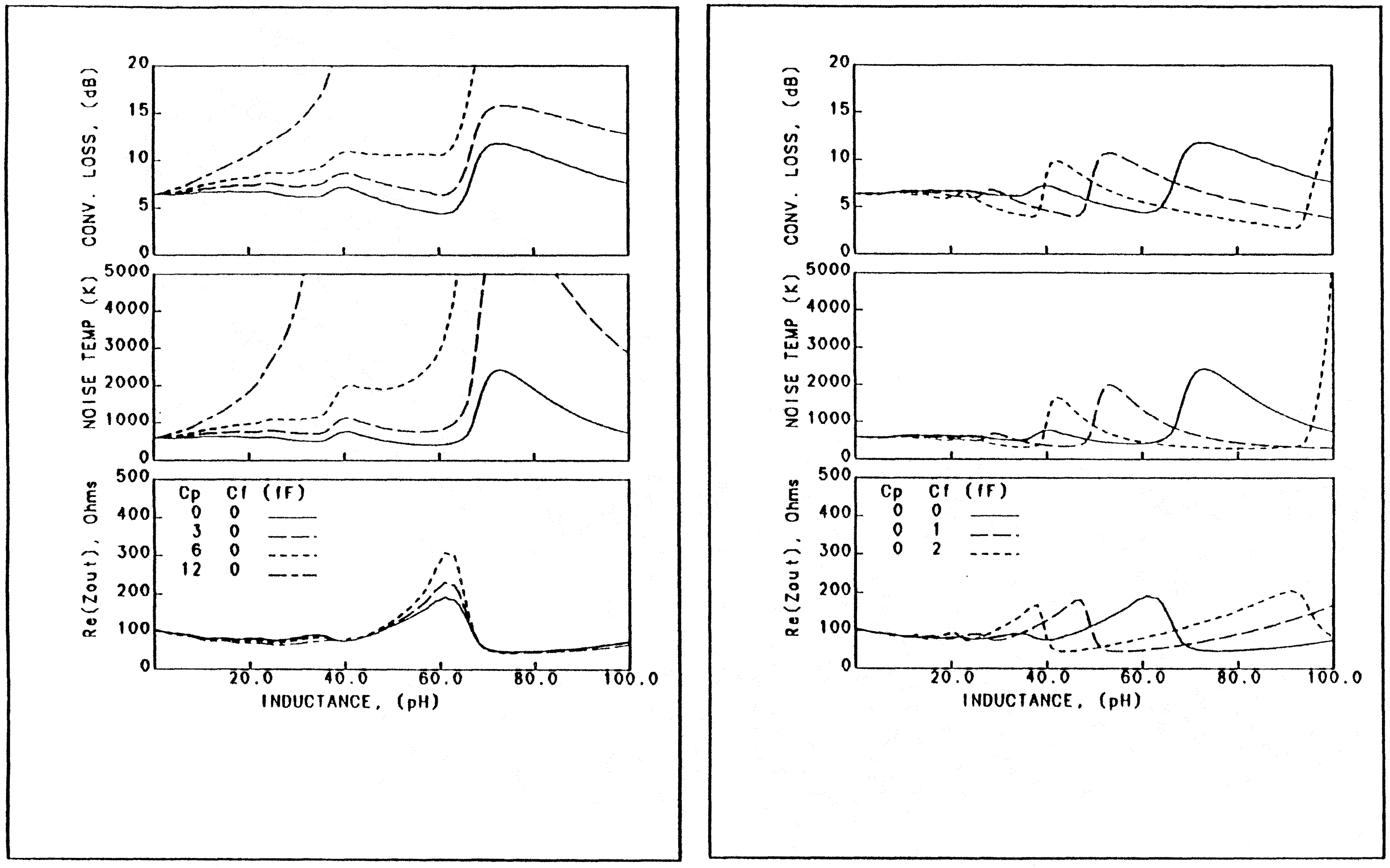


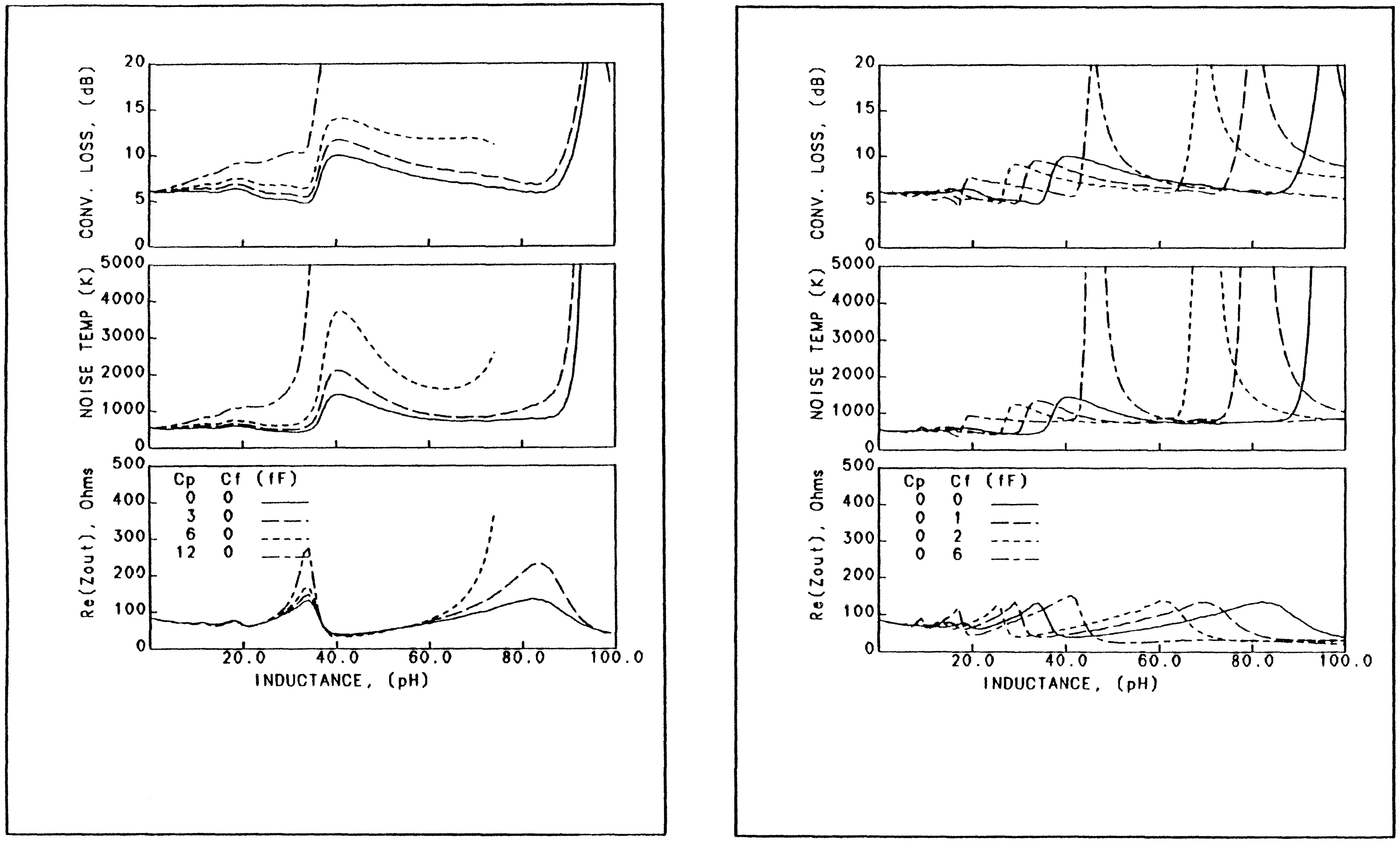
Figure 2 (a) Subharmonic mixer circuit used in simulation after [9,10], (b) assuming identical diodes the equivalent circuit for DC and even harmonics of the LO, (c) equivalent circuit for odd harmonics of the LO.



3(a)

3(b)

Figure 3: Effect of the parasitic capacitance on the performance of a 216 GHz subharmonically pumped mixer as a function of loop inductance for a diode with R_s=12 Ω and C_{jo}=3 fF. (a) C_p is varied from 0 fF to 12 fF, (b) C_f was varied from 0 fF to 2 fF.



4(a) 4(b)

Figure 4: Effect of the parasitic capacitance on the perfomrmance of a 216 GHz subharmonically pumped mixer as a function loop inductance for a diode with R_s=6 Ω and C_{jo}=6 fF. (a) C_p varied from 0 fF to 12 fF. (b) C_f varied from 0 fF to 2 fF.

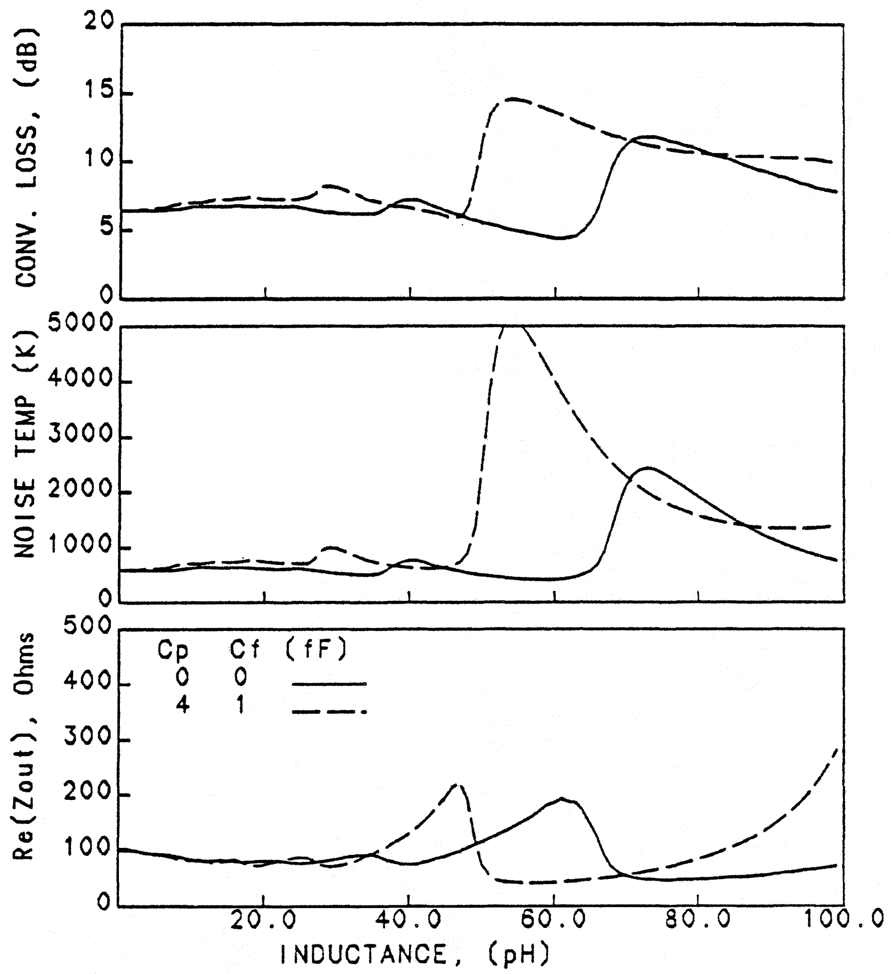


Figure 5: Subharmonic mixer performance comparison between a low capacitance (whisker contacted) and a higher capacitance (planar) diode. The solid curve represents the whisker contacted diode. LO, signal and IF are 108, 216, and 1.4 GHz respectively. R_s=12 Ω and C_{jo}=3 fF for both diodes. C_p, C_f = 0 for the whiskered diode and 4 and 1 fF respectively for the planar diode.