NOVEL CHIP GEOMETRIES FOR THz SCHOTTKY DIODES

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Introduction

For THz applications involving low noise heterodyne receivers, the whisker-contacted Schottky barrier diode provides excellent room temperature and cryogenic performance. The traditional chip structure consists of a honeycomb anode array on top of a chip which is typically 100μm square and 100μm thick, with ohmic contacts on the back, or occasionally on the side, so-called notch-front chips [1]. The chip is mounted in a variety of structures such as across waveguides, on planar filter metallisations, or at the end of coaxial filters, and the ideal chip shape for these differs. It is important to build the chip structure into the electrical design, especially at short wavelengths where chip dimensions are comparable to waveguide dimensions.

Fabrication Options

In light of the above, we explore in this paper the possibilities for fabricating new or improved chip structures using advanced processing techniques such as reactive ion etching (RIE), etch-stop layers, epitaxial lift-off (ELO), and bonding by atomic rearrangement (BAR). RIE enables the etching of deep features (up to hundreds of micrometers) into the surface of the semiconductor wafer [2]. Additionally, the side profiles of the etched features can be controlled, varying between purely isotropic to highly anisotropic. Etch-stop-layers are often used to enable accurate control of vertical etching. ELO is a technique involving the use of chemical etching and often etch-stop-layers, in which the surface layers including the active devices are lifted off one substrate and transferred to another [3]. For example, active optoelectronic devices can be fabricated on InP or GaAs substrates and transferred to Si wafers where they can be interconnected with electronic circuitry [4]. In respect to millimetre wave devices, it can be envisaged as a good technique for producing very thin planar chips. BAR [5] is an alternative for achieving this result, in which pieces of one semiconductor can be

attached to another using a high temperature controlled environment anneal to create the bond. These various techniques enable processes to be developed for the fabrication of chips with arbitrary cross-sectional shape with high yield and with little if any limitation on the electrical characteristics of the anode junction.

Fabrication Process

The most straightforward technological solution involves RIE. We have developed a process which allows diode chips of circular, square or rectangular cross-section to be fabricated in thicknesses down to about 20μm. The process commences by the deposition of a layer of passivation, usually SiO_2, to a thickness of about 0.5μm. This is followed by the lithography for the anode definition. We use an electron beam lithographic system along with dry-developable sylilated resist technology for this step. The anode holes are defined in the SiO_2 layer using RIE with CHF_3/Ar gas. The chip shape is then defined by a second level of lithography, 30μm circles in the case of the chips described here, followed by deep RIE in $SiCl_4$ gas. An ohmic contact is electroplated on to the mesa sidewalls and alloyed prior to Pt/Au anode metallisation. The substrate is removed by a chemical/grinding process and a back contact metallisation is evaporated on to the chips before separation for electrical characterisation.

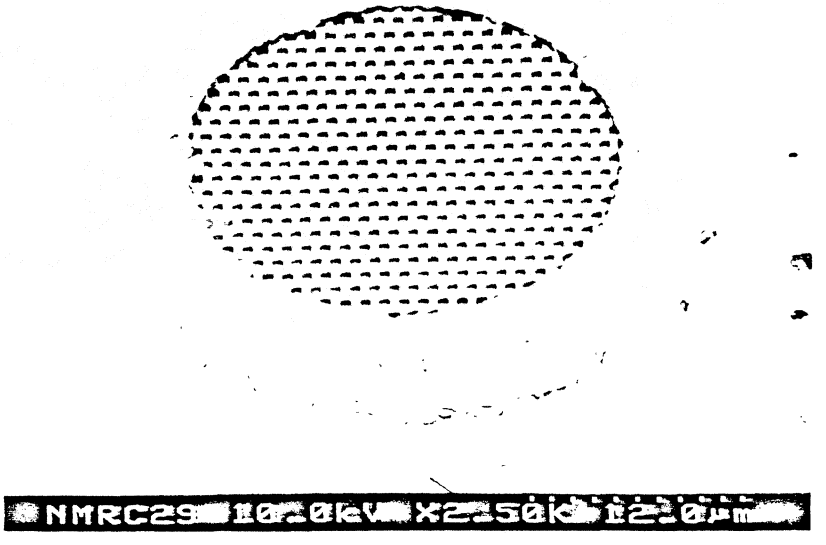

Figure 1. Micrograph of 30μm diameter cylindrical Schottky diode chip. The chip is 30μm high and is patterned with 0.9μm anodes.

The micrograph in figure 1 shows for example a single 30μm diameter by 30μm high cylindrical diode chip with an array of micron-sized Schottky anodes on the top surface. This chip is ideally shaped for location at the end of a coaxial RF choke filter.

Device Characteristics

The above procedure has been used to fabricate a batch of demonstrator cylindrical diode chips with anode diameter of 1.3μm on MOVPE grown GaAs. This material had a 5μm buffer layer of doping $4x10^{18}$ cm^{-3}, with a 600Å epilayer doped to $5x10^{17}$ cm^{-3}. DC electrical characteristics of a typical diode are shown in figure 2.
The data is presented as a plot of log(I) against V, together with a curve of $I = I_o exp(q(V-IR_s)/\eta kT)$. The series resistance of the device has been measured as R_s = 5.5Ω at a current of 10mA, consistent with the expected epilayer resistance and ohmic contact area. The diodes exhibit an ideality factor of η = 1.2 and a zero-bias junction capacitance of 6fF. Thus it can be seen that this new process can be used for the fabrication of smaller chip geometries without adversely affecting the electrical characteristics of the resulting devices.

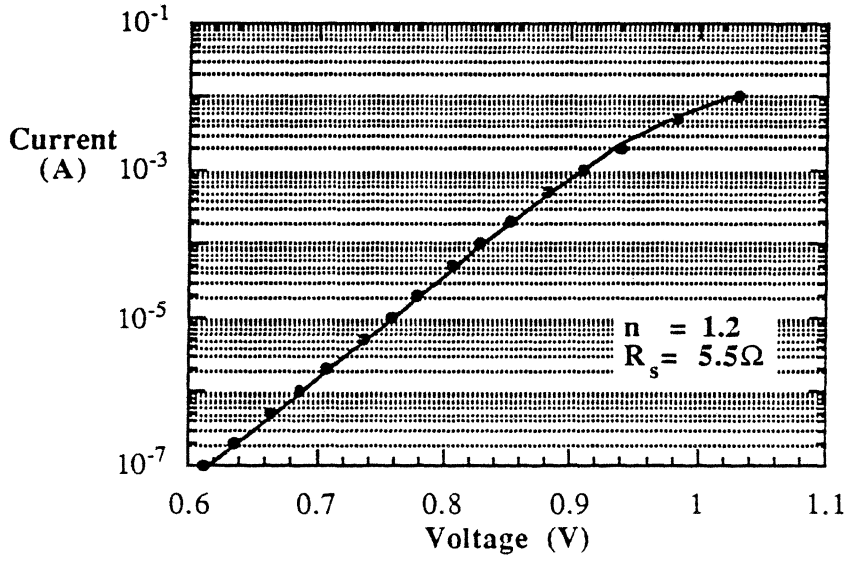

Figure 2. I-V characteristic of 1.3μm diameter diode on cylindrical chip

We have also made devices with square anodes and high packing density as in figure 3, allowing for easy whisker contacting.

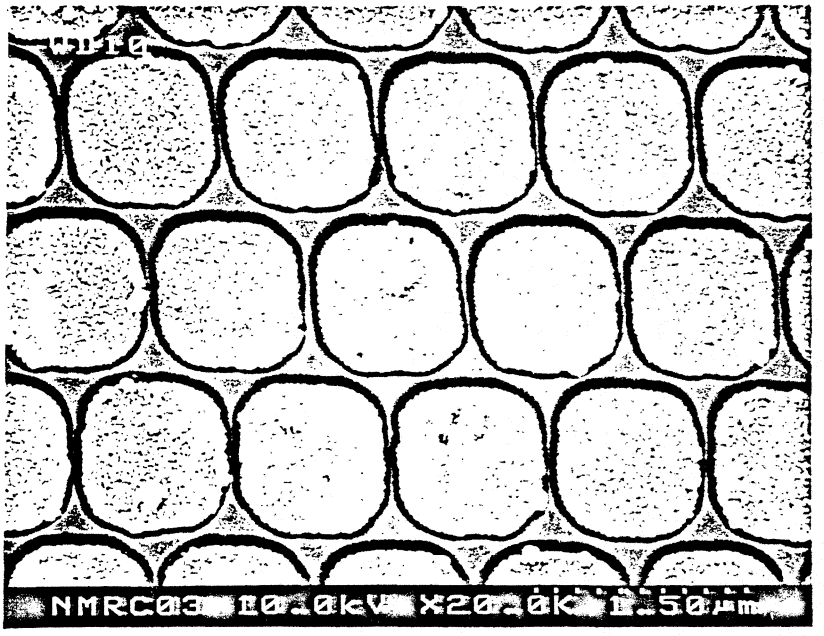

Figure 3. Densely packed 0.9μm square anodes with Pt/Au metallisation

Conclusions

An advanced process for the fabrication of new Schottky barrier diode chip geometries has been developed. The technique facilitates the production of chips with arbitrary cross-section and is especially suited to the fabrication of chips with dimensions less than the 80μm limit allowed by dicing. The devices are mechanically robust and exhibit no adverse effects on their electrical characteristics as a result of the fabrication procedure. Using this process, the structure of the diode chip can be matched to that of the circuit components, representing a significant advance for optimising the performance of submillimetre systems incorporating Schottky diode technology.

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