A Balanced Doubler Using a Planar Diode Array for 270 GHz

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ABSTRACT

A balanced doubler for 270 GHz has been built using a planar array of four varactor diodes. The maximum output power is 5.5 mW, with 45 mW input, corresponding to an efficiency of 12%. Much higher efficiencies should be possible given the measured device parameters, but circuit or device parasitic losses appear to be a limitation at present.

INTRODUCTION

In the frequency range above 100 GHz, frequency multipliers can achieve high conversion efficiency at low input power, but tend to saturate at a rather low output power. The saturation mechanism is believed to be due to the limited carrier velocity in the GaAs epitaxial layer [1], which leads to a maximum displacement current in the varactor. Since the current increases with frequency for a given voltage swing, this becomes a major limitation for submillimeter applications.

One of the most attractive solutions to this problem is to use series arrays of diodes, because they allow one to increase both the area and the number of diodes, while they may be treated as a single diode so far as circuit design is concerned. In an array having the same impedance level and total power handling as a single diode, the current density varies inversely with the number of diodes. In work reported previously [2], we were able to use this approach to build a doubler for 160–180 GHz using a four diode array which greatly exceeded the power capability of conventional whiskered diodes. The doubler described in this work, operating with an output frequency of 270 GHz, also uses four planar diodes fabricated on a single chip.

The diodes fabricated for this doubler have excellent parameters (as measured at low frequencies) and have been designed for optimized operation in the circuit. A doubler mount has been designed for their use, and the diodes successfully installed. The output power obtained is comparable to that expected from a pair of whiskered devices at the same frequency. However, the efficiency is much lower, apparently due to some presently unknown loss. While this demonstrates the potential for such arrays, work remains to understand the nature of the loss.

DIODE DESIGN AND CHARACTERIZATION

The doubler circuit used is close to a scaled version of the one reported previously [2]. This circuit is quite simple to fabricate, and the installation of planar diodes in the 170 GHz model was fairly easy. The primary design constraint for the diodes is that the chip must fit into this mount. Diodes for this work were fabricated using the surface channel process [3], and this constrains the geometry to be an array in a straight line. The diode layout is shown in Fig. 1, showing the connections to the doubler mount at three points. The large central pad serves as the ohmic contact for the two central diodes, as well as the output terminal. The ohmic contacts for the end diodes are the two small inner pads. The end pads are sized

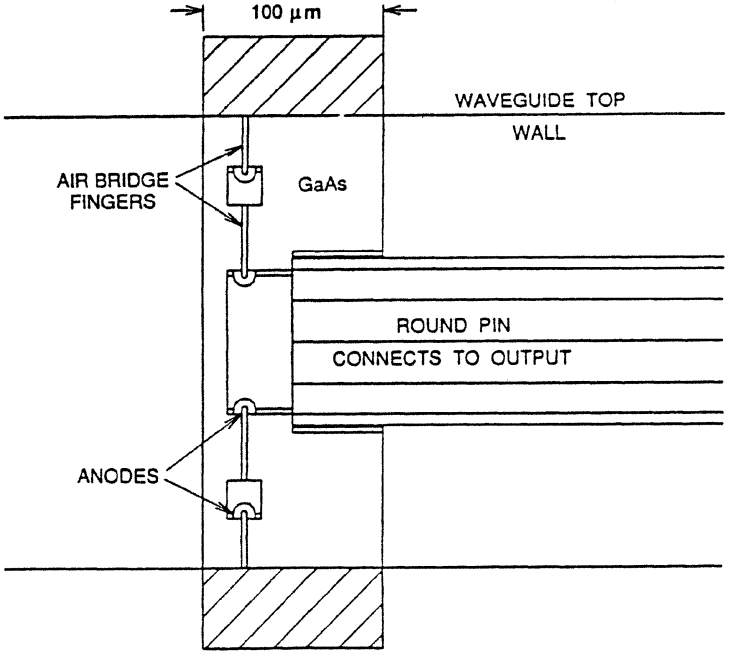

Fig. 1. Planar diode array, showing the method of installation into the circuit. The ends are soldered to the input waveguide walls, while the center pad solders to a pin connecting to the output waveguide. Chip is 370x100x25μm, waveguide is 330μm high.

to permit the chip to be soldered to the top and bottom walls of the waveguide. The diode layout was checked with the Hewlett Packard HFSS program to balance the power to the two diodes of each series pair, as well as to ensure reasonable power coupling to the chip. An effort was made to maximize the circuit inductance within the chip, since all varactors require substantial series inductance to tune out the average junction capacitance.

The series resistance of the parallel combination of the two pairs of diodes (equivalent to the resistance of a single diode) was measured in the doubler mount both at dc and using an HP 8720 network analyzer at 130 MHz [2]. The dc measurements gave a resistance of 6.4 Ω, while the rf measurements were about 1 Ω higher. The capacitance of each junction was measured at 1 MHz using a standard capacitance bridge. The junction capacitance was 16 fF with an additional pad to pad capacitance of 6 fF. The minimum value for the junction capacitance was 6 fF. The available pump power required a total breakdown voltage of only 15 V total for the two series diodes.

DOUBLER MOUNT AND TESTS

The doubler design is electrically equivalent to that in [2], but was scaled and slightly redesigned for use at 270 GHz. A cross section is shown in Fig. 2. All the waveguides were

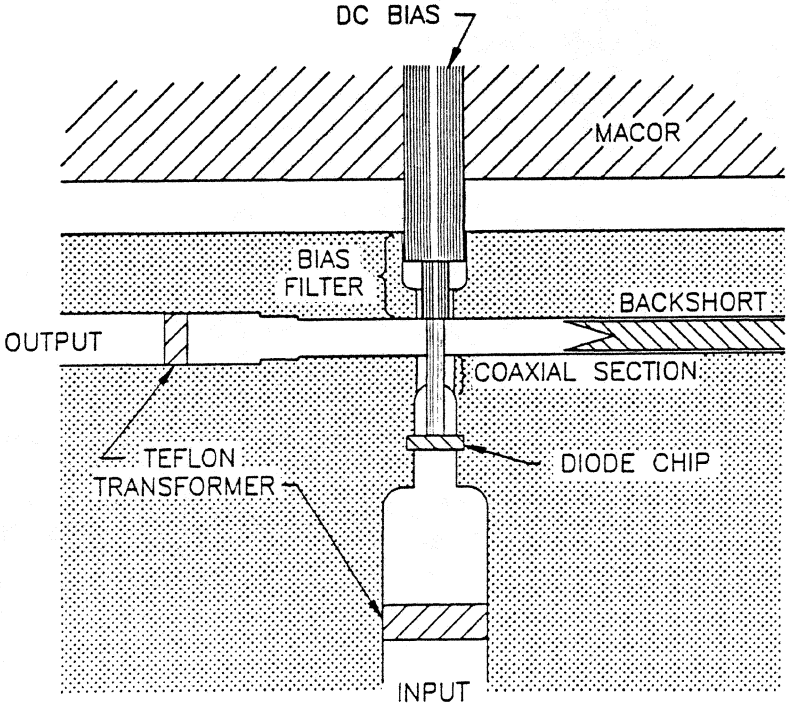

Fig. 2. Cross section through the balanced doubler mount.

milled symmetrically about the center line with the coaxial sections milled with a square outer section. The diode is soldered to the waveguide top and bottom walls as well as to the center pin in one operation, using low temperature indium solder. This operation was difficult with the small chip, but a technique was worked out in which the diode was placed on three thin solder preforms which ensured that the correct amount of solder was used. It is necessary to quickly cool the block after soldering since the solder tends to migrate along the surface of the device and bridge the anodes to the ohmic pads.

All tests were made with a 45 mW Gunn oscillator source tuning 125–145 GHz. The greatest output power was for 135 GHz input. At this frequency, no low loss isolators are available, so the interaction between the oscillator and the highly nonlinear load of the doubler can be severe. This is particularly a problem when neither the source nor the load is matched, as is the case here. To reduce the adverse interaction, a low loss adjustable phase shifter was included in the input circuit. A similar problem exists at the output, where the power sensor used (an Anritsu WR–8 sensor with taper to WR–3) also was poorly matched. The result is that it is difficult to determine the actual input and output powers, and whether the doubler is well matched. The Anritsu sensor was calibrated at both input and output frequencies with the same calorimeter built in WR–12 waveguide [4].

In these tests, the input and output match were optimized using teflon quarter–wave transformers positioned in the waveguide so that the output power was maximized. These transformers can correct a maximum VSWR of:

$$\epsilon(\text{teflon})[\lambda_g/\lambda(\text{air}) \;/\; \lambda_g/\lambda(\text{teflon})]^2 \cong 2.9 \text{ (typically)}.$$

For the input circuit, the strong interaction with the oscillator made it impossible to determine the match obtained, but it was assumed that the maximum power from the oscillator was coupled to the doubler, since the addition of a second transformer was of little benefit. The improvement in power with the addition of the output transformer was only about 25%, meaning that the output match was fairly good. The available power was measured at 45 mW though the phase shifter, by placing a teflon transformer before the power sensor, and varying the phase for maximum power.

The peak output power was 5.5 mW, under bias conditions of 7.8 V and 0.3 mA. The efficiency is 12%, while the theoretical efficiency of the diode (assuming $\gamma = 0.4$, $R_s = 7.4\ \Omega$, $C_j(0) = 16$fF for each junction) is 35% at a total input power of 40 mW. While this operation corresponds to the expected varactor mode, only slightly less power (~5 mW) was obtained under very different bias conditions of 2.1 V and 7.4 mA. This is quite surprising since this mode of operation is inherently much less efficient due to the large dissipation of

power (15.5 mW) in the bias circuit. This would be the case if the diode had poor capacitance modulation, but this is inconsistent with the low frequency characterization of the diodes. The chip is not expected to show significant saturation at the input power level of 11 mW per junction, but no measurements of output vs. input power have been made. Another possibility is that some unmeasured parasitic loss is present, either in the diode chip or in the doubler mount, and that this loss is relatively more important when the diode is biased in the high Q varactor mode. This type of loss appears to be present on the 160–180 GHz planar diode doubler, and is discussed in ref [5]. Since these diodes are made in a very similar way, a full understanding of the lower frequency doubler should clarify these results.

CONCLUSIONS

A balanced doubler using a planar array of four varactors has been successfully built for 270 GHz. The output power is 5.5 mW at 12% efficiency. This efficiency is considerably lower that is expected from the diodes and work is presently directed at understanding the reason for this discrepancy.

ACKNOWLEDGEMENTS

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