Planar Balanced Doubler Chip to 320 GHz

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I. INTRODUCTION

Schottky barrier varactor diodes are used as frequency multipliers in the local oscillator sources of heterodyne receivers at millimeter and submillimeter wavelengths. Whisker contacted GaAs Schottky barrier varactor diodes have been the most common frequency multiplier element, and have been used in heterodyne receivers extending well into the submillimeter wavelength range [1,2,3,4,5]. Although whisker contacted varactor diodes have proven very effective, much work has gone into developing varactor diodes which are more mechanically robust and have the potential to deliver larger amounts of power. This paper reviews the development of a planar varactor diode chip to be used in a balanced doubler to about 320 GHz.

The development of a multiplier chain to 1 THz using planar varactor diodes has continued. The proposed chain consists of two doublers (80 to 160 GHz and 160 to 320 GHz) and a tripler (320 to 960 GHz). The doubler chips incorporate multiple diodes for increased power handling ability, and are designed to be used in a balanced doubler circuit designed by Erickson [4]. The 320 GHz doubler chip is based upon the 160 GHz chip, which has been used in the balanced doubler circuit to generate record output power of 55 mW at 170 GHz [6,7,8].

The design goals for the 320 GHz doubler chip are reviewed in section II, and the DC characteristics for the prototype devices are described in section III. The results of

RF measurements are briefly described in section IV.

II. CHIP DESIGN GOALS

The 320 GHz balanced doubler chip is based upon the 160 GHz chip, however the design goals for the two devices are different. The primary goal in designing the first stage doubler was to generate as much output power as possible. The second stage doubler, however, must operate at twice the frequency, and is not required to handle as much input power. Therefore, the primary goal in designing the 320 GHz device is to achieve maximum diode efficiency while retaining moderate input power handling. An additional goal is to improve upon the power balance between the four junctions so maximum device efficiency is possible. The new device must also be designed so the chip fits in the 320 GHz doubler mount, requiring a chip length of only 500 μm. Sketches of the 160 GHz and 320 GHz devices are shown in Fig. 1 for comparison.

Since the goal is to develop an efficient doubler, the 320 GHz chips have considerably higher epitaxial layer doping densities and much thinner epitaxial layers compared to the 160 GHz diodes. The increased doping levels are required for reducing the device series resistance, which is especially important since the anode diameters are considerably smaller for the 320 GHz diodes. Although the higher doping density and thinner active layer result in a lower reverse breakdown voltage, this trade-off is acceptable since the input power requirement for the 320 GHz diodes is considerably lower than for the 160 GHz devices.

Similar to the 160 GHz doubler chip, the 320 GHz chip has two varactor diodes in series for each "leg" of the balanced doubler circuit. Since the doubler chip is soldered across the input waveguide, an initial constraint on the chip design is to fit the device into

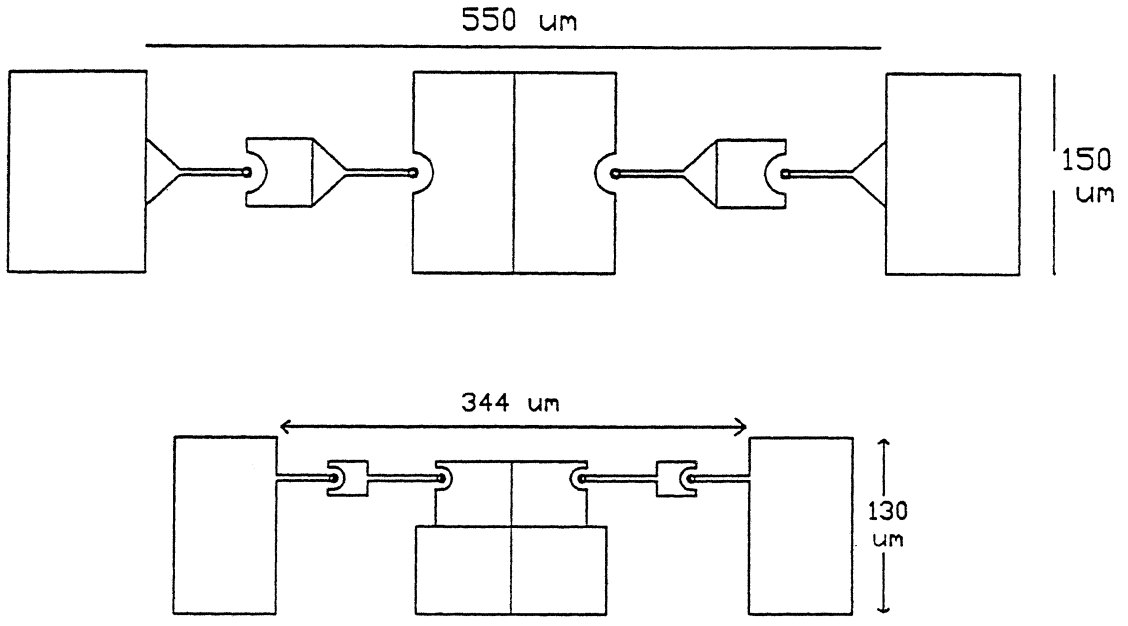

Fig. 1: Sketch of the 160 GHz (top) and 320 GHz (bottom) doubler chips.

the doubler mount. The Hewlett Packard High Frequency Structure Simulator (HFSS) has been used by J. Tuovinen (of the University of Massachusetts, Amherst) to help determine the chip dimensions for the prototype devices [9]. The 320 GHz chip is designed to span the input waveguide and is 500 μm in length by 130 μm in width. The ohmic contact pad size for the two inner diodes has been reduced to 25 μm x 25 μm and the center output pad and end contact pads have also been reduced in size compared to the 160 GHz chip. The smaller pads not only help lower the parasitic pad-to-pad capacitance, but they are necessary so that a total finger length of about 100 μm for each diode pair can be achieved for the reduced chip length. In order to reduce the ohmic pad size to 25 μm x 25 μm and obtain low series resistance, a contact resistivity of approximately $10^{-6}\Omega cm^2$ must be achieved for the 25 μm x 25 μm ohmic contact pads.

To achieve a good power balance between the four varactors on the doubler chip, each diode must have very similar characteristics. In addition to the junction capacitance, which is a function of the anode area, the pad-to-pad capacitance of each diode should also be approximately equal. Since the center output pad is considerably larger than the end contact pads, the finger length of the two center diodes (54 μm) is larger than that of the end diodes (42 μm) so the pad-to-pad capacitance seen by each diode is approximately the same. In addition, the center output pad is "flared" at the bottom so the bias pin can be soldered in place without having the solder come close to the center anodes.

The predicted chip parameters and DC characteristics for the planned 320 GHz diodes are listed in Table I. The 12 fF junction capacitance for each diode is designed to achieve a good match between the chip and circuit, and the series resistance is minimized while maintaining a breakdown voltage of approximately 8 V. The measured parameters for the 160 GHz SC10V2 doubler chips are also listed for comparison [6,7,8].

Table I: Predicted Parameters and DC Characteristics for 320 GHz Chip (single diode)

type	t_{chip} (μm)	t_{epi} (μm)	N_{epi} (cm^{-3})	diam (μm)	C_{j0} (fF)	R_s (Ω)	V_{br} (V)
planned 320 GHz	25	0.40	$1x10^{17}$	4	12	7	8
measured 160 GHz	25	0.64	$4.5x10^{16}$	9	37	6	15

III. PROTOTYPE 320 GHZ DOUBLER CHIPS

Four batches of prototype 320 GHz balanced doubler chips have been fabricated, and an SEM photograph of a completed chip is shown in Fig. 2. As for the 160 GHz chip, the large central pad serves as the ohmic contact for the two central diodes, as well as the output terminal and bias connection. The ohmic contacts for the end diodes are the two small inner pads. The fabrication steps used for the 320 GHz doubler chips are based upon the surface channel process [10,11,12], and the 160 GHz planar doubler chip fabrication [6,7,8].

DC Characteristics

The measured DC characteristics of the four prototype batches of 320 GHz chips are shown in Table II. The SC3T1 and SC3T2 diodes have been fabricated with

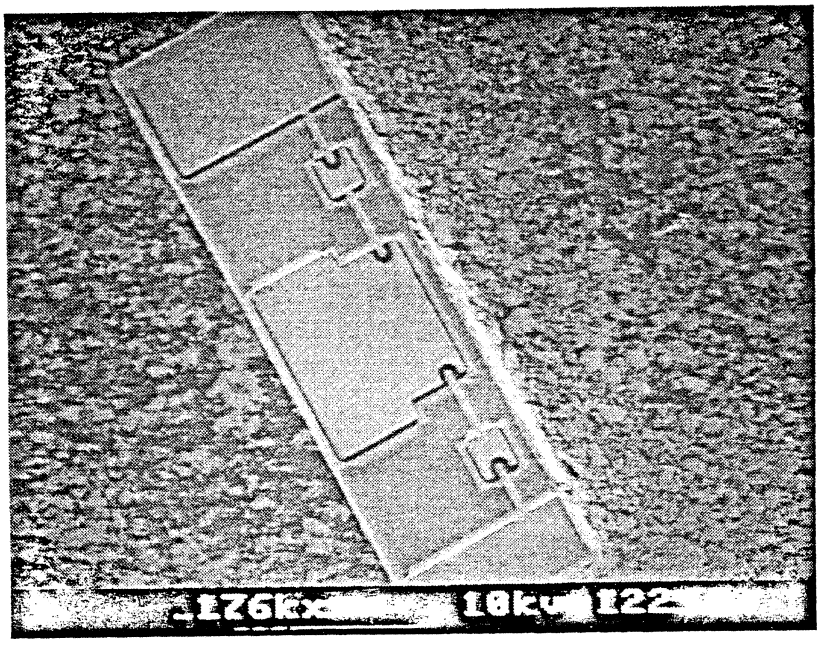

Fig. 2: SEM Photograph of the 320 GHz Balanced Doubler Chip.

evaporated ohmic contacts in an attempt to reduce the contact resistance, and have very similar DC characteristics. The zero bias capacitance, series resistance and breakdown voltage of these diodes are close to the predicted values given in Table I. However, the SC3T1 and SC3T2 diodes have very poor capacitance modulation (maximum capacitance/ minimum capacitance ratio) which severely limits the device RF performance. Diodes from these two batches have capacitance ratios $(\frac{C_{max}}{C_{min}})$ of approximately 1.2. A ratio of at least 2 is desired for frequency multiplication.

In the next batches of devices, steps have been taken to improve the capacitance modulation. The SC3T1 and SC3T2 diodes tend to punch-through before the maximum electric field for breakdown is reached, indicating a thicker active layer could yield improved performance. The SC3T3 devices have the same epitaxial doping density as the two previous batches, but the epitaxial thickness has been increased to 0.27 μm to allow for a greater applied reverse voltage and additional capacitance modulation. The

Table II: 320 GHz Balanced Doubler Chip Characteristics (single diode)

batch #	t_{chip} (μm)	t_{epi} (μm)	N_{epi} (cm^{-3})	diam (μm)	C_{j0} (fF)	R_s (Ω)	V_{br} (V)
SC3T1	25	0.25	$1.5x10^{17}$	3	14	8	7
SC3T2	25	0.25	$1.5x10^{17}$	3	15	9	7
SC3T3	25	0.27	$1.5x10^{17}$	4.5	28	8	8
SC3T4	25	0.40	$1.0x10^{17}$	3.5	15	6	9

SC3T4 diodes have a reduced epitaxial layer doping density of $1x10^{17}cm^{-3}$ in addition to an increased thickness of 0.40 μm. A lower active layer doping density should lead to a sharper capacitance variation. To eliminate possible sources of error and improve device yield, the evaporated ohmic contacts have been replaced with the proven SnNi/Ni/Au alloyed ohmic contact technology for the SC3T3 and SC3T4 diodes.

Capacitance measurements indicate the SC3T3 and SC3T4 diodes do have considerably improved capacitance modulation. The junction capacitance of the SC3T3 diodes, however, is quite large due to oversized anodes and they are not suitable for the 320 GHz doubler mount. The SC3T4 devices have a zero-bias junction capacitance of 15 fF, and a capacitance ratio of approximately 1.5. Often the pad-to-pad capacitance of planar diodes can be tuned out in the multiplier circuit. If the 4 fF pad-to-pad capacitance is subtracted from the SC3T4 diodes, the capacitance ratio improves to almost 2.

In addition to the pad-to-pad capacitance, the finger capacitance contributes to the total parasitics of the device. Most of the finger capacitance is caused by a portion of the contact finger overlying the oxide and the conductive GaAs near the anode. In an effort to reduce this capacitance, several SC3T4 chips have been etched an additional 12 minutes in the surface channel etch to undercut the contact finger length which covers the oxide and conductive GaAs. In Fig. 3 the capacitance-voltage characteristic of an SC3T4 single diode is shown before and after the additional surface channel etch. It is evident from the capacitance curve that the effect of the additional etching is a reduction in total capacitance by approximately 3 fF and an increase in the measured capacitance ratio from 1.5 to 1.7. If the pad-to-pad capacitance is now subtracted from the diode after the

additional etching, a capacitance ratio greater than 2 is obtained. The increased capacitance modulation of the SC3T4 diodes should lead to significantly improved RF performance.

IV. 320 GHz DOUBLER RF RESULTS

RF measurements for the SC3T2 and SC3T4 diodes have been performed by N. Erickson [13]. The planar doubler mount used for the 300 GHz tests is a scaled version

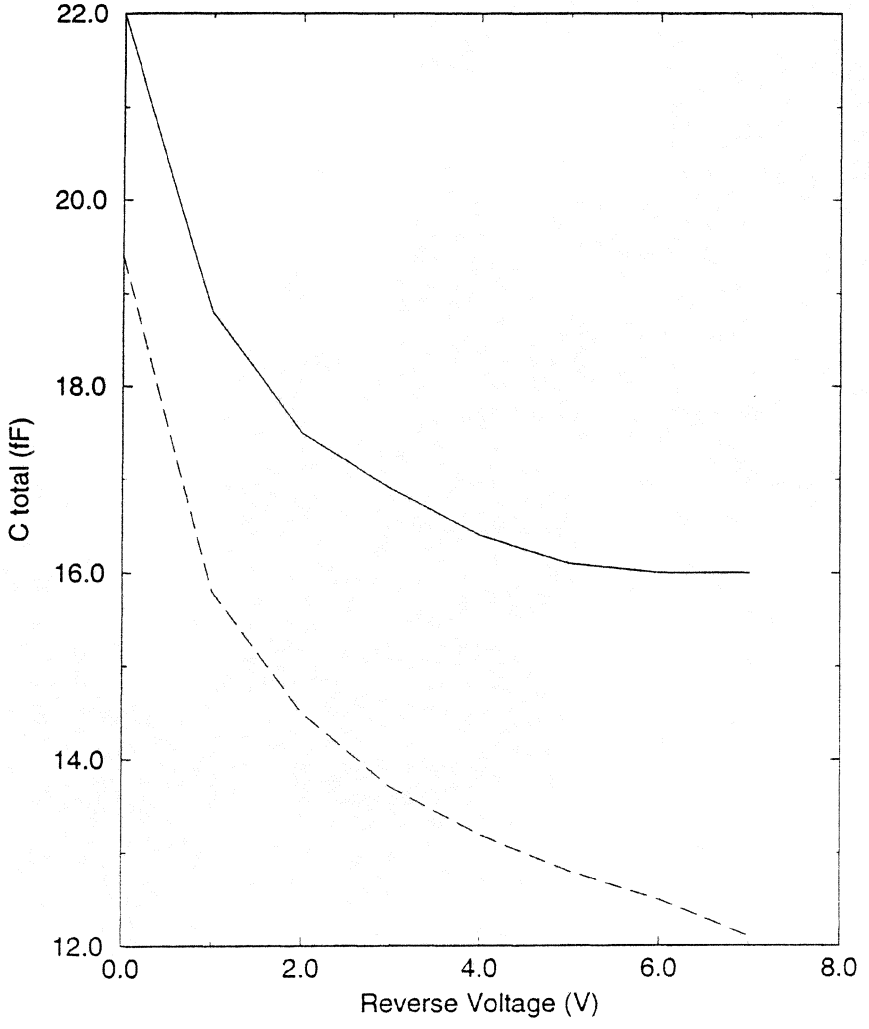

Fig. 3: C-V curve of SC3T4 diode before etching (solid) and after etching (dashed).

of the one used for the 160 GHz diodes [6,7,8]. The two doubler block cross-sections are essentially identical, and a sketch of the planar balanced doubler mount design is shown in Fig. 4. Matching for the 300 GHz tests was optimized using teflon quarter-wave transformers, which can be positioned in the input and output waveguides to achieve maximum output power. In addition, tuning is possible through the use of input and output backshorts. The substrates for the 320 GHz doubler chips have been thinned to approximately 25 μm to reduce the circuit loading caused by the bulk GaAs. The impedance match obtained for the planar chips is comparable to that for whiskered diodes in similar mounts.

Despite their small measured capacitance ratios, the SC3T2 diodes produced encouraging RF results. An output power of approximately 4 mW has been generated at

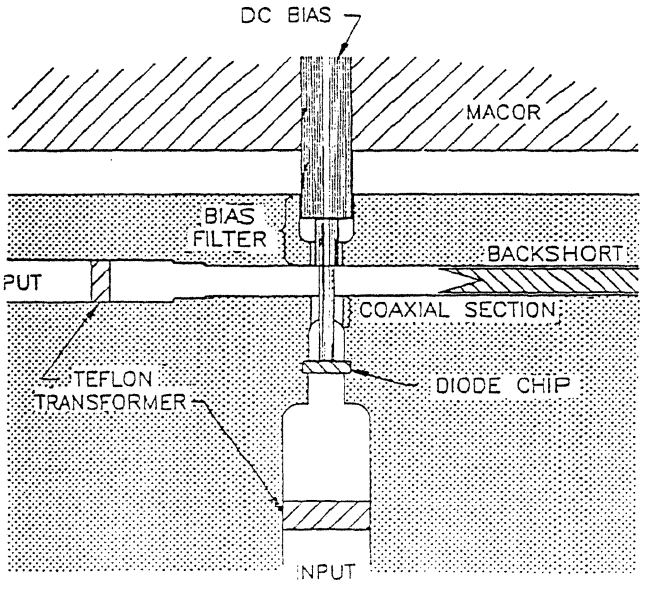

Fig. 4: Cross-section of the planar balanced doubler mount.

320 GHz with 30 mW input power supplied by a source consisting of a Gunn oscillator in conjunction with the 160 GHz planar balanced doubler. The SC3T2 diodes are certainly not optimized, as they produced the maximum output power of 4 mW at an applied bias between zero and -2 V, indicating much of the frequency multiplication occured in a resistive, or "varistor" mode. In the "varistor" mode of operation, the forward I-V characteristic of the diode is used, and this is much less efficient than when operating as a varactor. Despite producing maximum output power with little to no applied reverse bias, this result matches the power output by Erickson's 300 GHz balanced doubler which uses two whisker contacted diodes [4]. The cause for the resistive mode operation is most likely due to the low breakdown voltage and small capacitance modulation of the SC3T2 diodes.

As expected, the SC3T4 diodes delivered improved performance compared to the SC3T2 devices due to increased capacitance modulation and breakdown voltage. A maximum output power of approximately 6 mW has been obtained at 270 - 300 GHz with the input power supplied by a Gunn oscillator. This result was achieved with 50 mW input power, for an efficiency of 12 %. Although this result is very impressive, the doubler does not appear to be operating at its fullest potential. The same output power obtained while operating in a "varactor" mode, which should be the most efficient, was also generated while operating in a "varistor" mode. A "varistor" mode of operation is normally not as efficient as pure varactor multiplication. The RF results indicate some parasitic element may be preventing the doubler from operating at its peak efficiency and causing it to operate equally as a varactor and a varistor. Despite this less than optimal operation, however, the generated output power equals the best doubler result at about 300 GHz.

V. SUMMARY

Improvements in planar chip and mount design have made the planar Schottky varactor diodes competitive with whisker contacted diodes at frequencies up to 320 GHz. By integrating several diodes on a single chip, increased power generation has been achieved.

Several design changes were implemented in the 320 GHz series diode array, including reducing the ohmic and anode contact pad sizes, staggering the finger lengths and reducing the overall chip dimensions compared to the 160 GHz devices. In addition, portions of the fabrication process were modified in the development of the smaller chips.

The first application of a planar array of varactor diodes in the 300 GHz frequency range has been demonstrated. The planar Schottky device has displayed superior performance to a pair of whisker contacted diodes used in a similar mount at a nearby frequency, thus demonstrating the potential for series diode arrays at millimeter and submillimeter wavelengths.

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