VERIFICATION OF THE FINITE ELEMENT ANALYSIS AND STUDY OF LOSSES OF A PLANAR DIODE DOUBLER

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Abstract

Microwave modeling using finite element analysis (FEA) is valuable for its flexibility and the ease with which modifications can be made to a structure. The focus of this paper is the verification of the accuracy of the results predicted by the FEA of a planar diode doubler from 85 to 170 GHz. Careful measurements with a slotted line were carried out to determine the diode terminal impedance at the input frequency. In the measurements, a commercial network analyzer could not be used due to the large input power requirement of the doubler. Good agreement between the measured and simulated the diode terminal impedance was observed, although full agreement requires the addition of an empirical loss term. Several options were considered for the source of the loss of the doubler structure. The most probable cause of the loss is the dislocation layer on the back side of the planar diode chip, which was formed when the diode was thinned mechanically. Full confirmation of this source of loss will be performed in the future.

1 Introduction

The design of high efficiency multipliers requires good modeling capabilities. This is particularly true in the case of multipliers with an array of planar diodes. Modeling based on the finite element analysis (FEA) has been chosen over conventional scale modeling in the work described here. The advantages of the FEA approach are that it makes it easy to study dielectric thickness effects, optimum inductances in the diode package, power balance between

the diodes, and the origin of parasitic effects. It also permits multiple probe ports, deletion of parts of the structure and splitting the structure in pieces. In this finite element analysis, the HFSS (High Frequency Structure Simulator by Hewlett Packard) software package was used.

This paper describes the work that was carried out to verify the accuracy of the results predicted by numerical simulations of a planar diode doubler from 85 to 170 GHz. This doubler is shown in Figure 1 and the full description of the FEA is given in [1]. Experimental tests on the doubler are explained in [2] and the details of the array of planar diodes in [3]. Careful measurements were carried out to determine the diode terminal impedance at the input frequency. The main problem in measuring the input impedance of a frequency multiplier (from which the diode terminal impedance can be calculated), is that it depends strongly on bias voltage and absorbed input (pump) power. The available input power for testing this doubler with an array of four planar varactors on a single chip should be at least 100 mW. This means that a commercial vector network analyzer can not be used to measure input impedances at frequencies around 85 GHz. Instead a WR-10 slotted line was used to measure the complex reflection coefficient, which was in turn used with the de-embedding circuit model to obtain the measured diode terminal impedances. Input reflection may greatly reduce the absorbed power, invalidating the "high power" measurement. Therefore, the input match was first optimized with a tuner consisting of a $\lambda_g/4$ thick piece of teflon properly placed in the input waveguide. The use of this simple matching transformer is convenient because its effect on the circuit can be easily predicted in the de-embedding process to obtain the diode terminal impedances. The output match was improved utilizing the same technique, since mismatch in the output affects the input impedance.

2 Measurement set-up

To verify the reliability of the simulated results, measurements of the input impedance of the doubler were carried out. Using the known input waveguide geometry, the de-embedded diode terminal impedance was calculated. The measurements were carried out between 79.7 and 90.6 GHz.

Before making the actual impedance measurements, matching in both the input and output port of the doubler were improved by adjusting the positions of two $\lambda_g/4$ thick teflon pieces in the respective waveguides. In this matching process the output power was

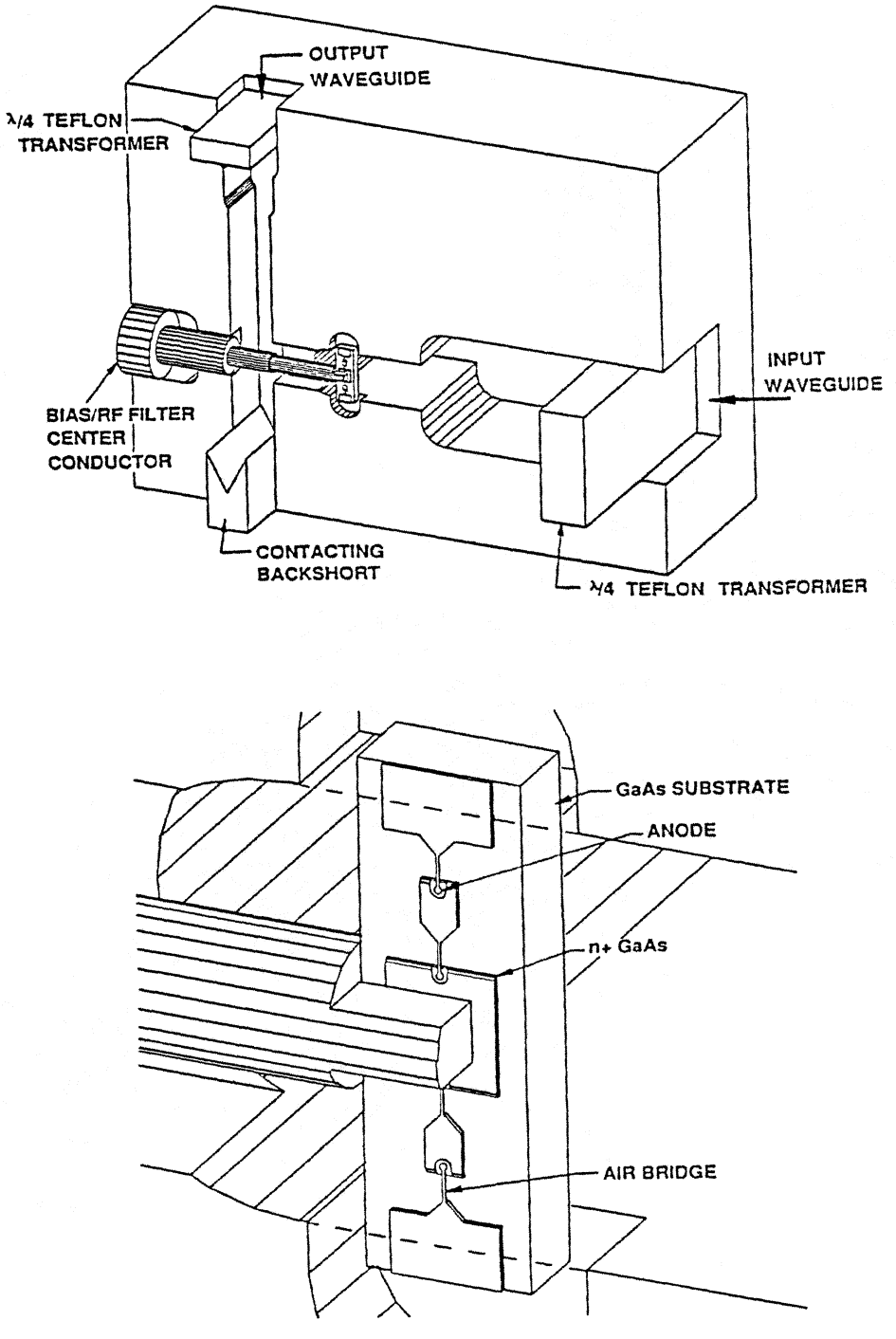

Figure 1: *The planar diode frequency doubler from 85 to 170 GHz used in the tests and in the finite element analysis. The end pads of the diode are soldered to a mating half of the block.*

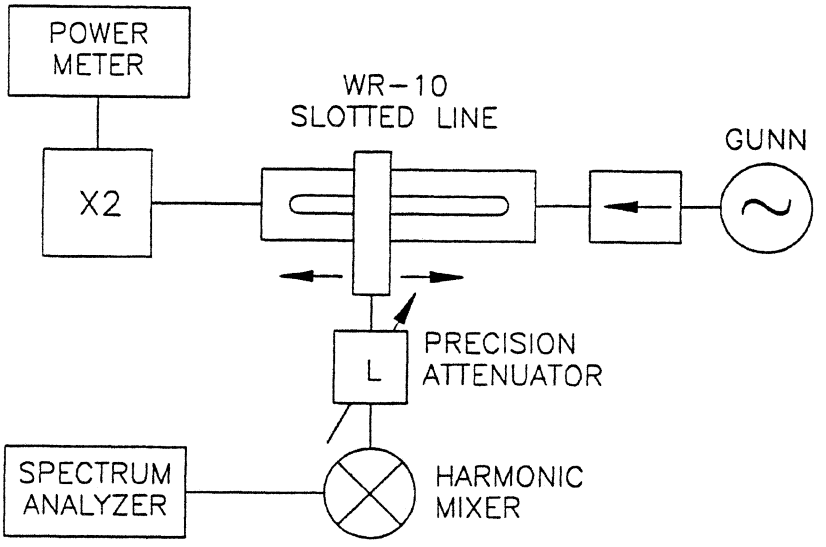

Figure 2: *Set-up for measuring the input impedance of the doubler.*

maximized and the reflected input power was minimized, with resulting VSWRs $< 2:1$ on both ports.

The input impedance measurement set-up is shown in Figure 2. At 79.7 GHz a fixed Gunn oscillator with an output power of 140 mW was used while at other frequencies a tunable Gunn oscillator with an output power of 100 – 120 mW was used. The maximum power with the latter Gunn was obtained around 82 GHz and the minimum at the high end of the measurement band. The Gunn oscillator was followed by an isolator, and a slotted line. The input waveguide of the doubler was connected to the other end of the slotted line and the output waveguide was connected to a power meter. The probe port of the slotted line was attached to a calibrated adjustable attenuator, which was followed by the harmonic mixer of a spectrum analyzer.

During the measurements, power coupled to the sliding probe was detected with the spectrum analyzer. The actual value of the power ratio was obtaining by adjusting the calibrated attenuator. This method of detection is more sensitive than a diode detector and also ensures that the oscillator is at the correct frequency.

The needed reference positions of the VSWR minima were obtained by placing a copper

plate between the flanges of the doubler and slotted line. Because of the limited isolation of the isolator in front of the Gunn oscillator, the Gunn had to be tuned (electrically or mechanically) slightly for the reference measurement. This is important for accurate measurements, because even a relatively small change in frequency causes a significant error in the location of the standing wave minimum and therefore in the phase of the reflection coefficient. This is because the probe of the slotted line is more than 15 wavelengths away from the short. During the measurements the frequency was kept fixed within few MHz.

With and without the short, three standing wave minimum locations were measured. The difference between the three minimum pairs were calculated and the average of the these differences was used to calculate the phase of the reflection coefficient. The magnitude of the coefficient was determined from the average of three power rations.

3 Comparison of the simulated and measured results

Comparison of the measured and simulated de-embedded diode terminal impedances is shown in Figure 3. The results in this figure are based on the assumption that the planar diode can be modeled as a two terminal device. The need of modeling the diode as a three terminal device was also considered. The required series element in three terminal device were so small that the assumptions of two terminal is well justified. During the measurements the diode bias was kept at 11 V. The input power varied from 100 to 140 mW. The GaAs substrate thickness of the diode was measured to be about 22 $\pm$ 2 μm. The theoretical curve was calculated using above input power, bias voltage, and substrate thickness. The second harmonic termination was chosen at the value for optimum efficiency. The effect of different sources of errors on the measurement is show in Table 1. The overall accuracy (3σ) of the measurements is about $\pm$4.0 and $\pm$4.1 Ω for the real and imaginary parts, respectively. The random errors were small; at a fixed frequency and doubler setting the real and imaginary parts were repeatable with in 1 and 2 Ω, respectively. Sources of systematic errors are the teflon matching transformer (position and tilt in the waveguide), frequency offset in the de-embedding, and output mismatch. Also, the assumption of no losses in the simulations causes systematic errors.

Figure 3 shows that the imaginary part of the impedance agrees very well with the simulations. The measured real part values are much more scattered and the difference between the measured and simulations can not be explained with the measurement errors.

Table 1: *Sources of error in the slotted line measurement of the diode terminal impedance.*

Source of error	Value of the error parameter at 3σ deviation	Value of error ($\pm$) $\mathrm{Re}(Z)/\Omega$	$\mathrm{Im}(Z)/\Omega$
VSWR	Accuracy of power ratio 1 dB	0.3	1.5
Phase of ρ	$\Delta\mathrm{ang}(\rho) = 30°$	2.0	1.25
Losses in WG mount	10 % loss assumed	0.25	0.25
Input power inaccuracy	P changed from 100 to 40 mW	1.5	2.25
Output mismatch	Trans. moved $\lambda_g/4$ from opt. pos.	2.25	2.25
Input trans. not ideal shape	Real shape simulated with HFSS	-	-
Input trans. tilted	Tilted 102 μm from one end	1.0	1.0
Input trans. position	Position changed 51 μm	1.5	1.25
Input trans. thickness	Thickness changed 51 μm	1.0	1.0
De-embedding frequency	Frequency changed 100 MHz	0.3	0.6
TOTAL ERROR (RSS) 3σ		$\pm$4.0	$\pm$4.1

The good agreement with the imaginary part of the measured and simulated values can be explained by the clear physical origin of the reactance. The reactance is mainly defined by the capacitance of the planar diode, which is due to the fringing fields in the planar structure and the junction capacitance. The origin of the real part of the terminal impedance is more complex. In addition to the series resistance of the junction the termination of the second and third harmonics affects the real part. In the simulation, an ideal open termination was assumed for the 3rd and higher harmonics.

The discrepancy between the measured and simulated real part of the diode terminal impedance implies the presence of a loss in the real doubler circuit that has been missed by lossless finite element simulations. A simple equivalent circuit of the planar diode is shown in Figure 4. This equivalent circuit includes a shunt resistance, which simulates the losses in the doubler structure. Comparison of the diode terminal impedance calculated using the equivalent circuit and the HFSS-MDS simulations is shown in Figure 5. This figure shows that a shunt resistance of 300 Ω could explain the higher measured real parts of the diode terminal impedance.

Four main sources of a possible loss in the doubler structure were foreseen: 1) waveguide losses, 2) limited conductivity of the n^+ region underneath the metal pads of the planar diode, 3) losses in the GaAs substrate, and 4) losses in the back surface of the planar diode chip (the rough ground surface formed during the thinning of the diode chip). Because of the first source of loss, a 10 %waveguide loss was included in the error analysis, which shows

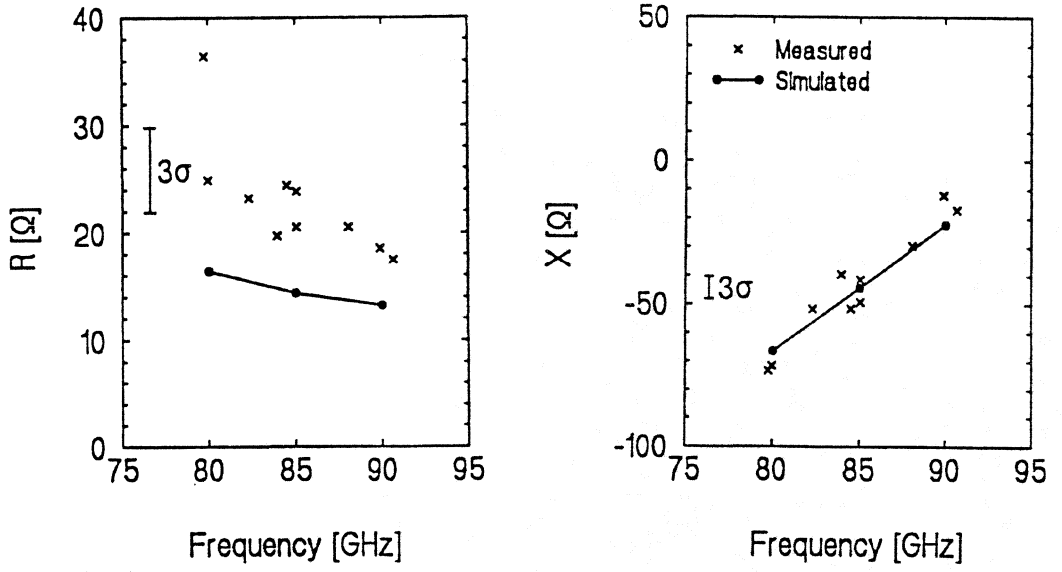

Figure 3: *Real and imaginary part of the measured and simulated de-embedded diode terminal impedances. The simulated curve is calculated for a 22 μm GaAs thickness and using real input power levels and bias voltages for the diode.*

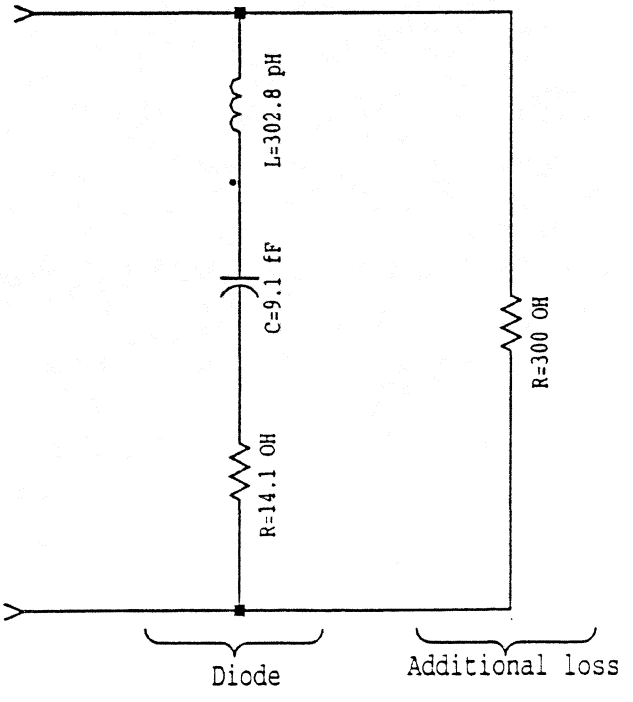

Figure 4: *The equivalent circuit of the planar diode at the input frequency. This circuit includes also the shunt resistor, which can explain the measured real parts of the diode terminal impedance.*

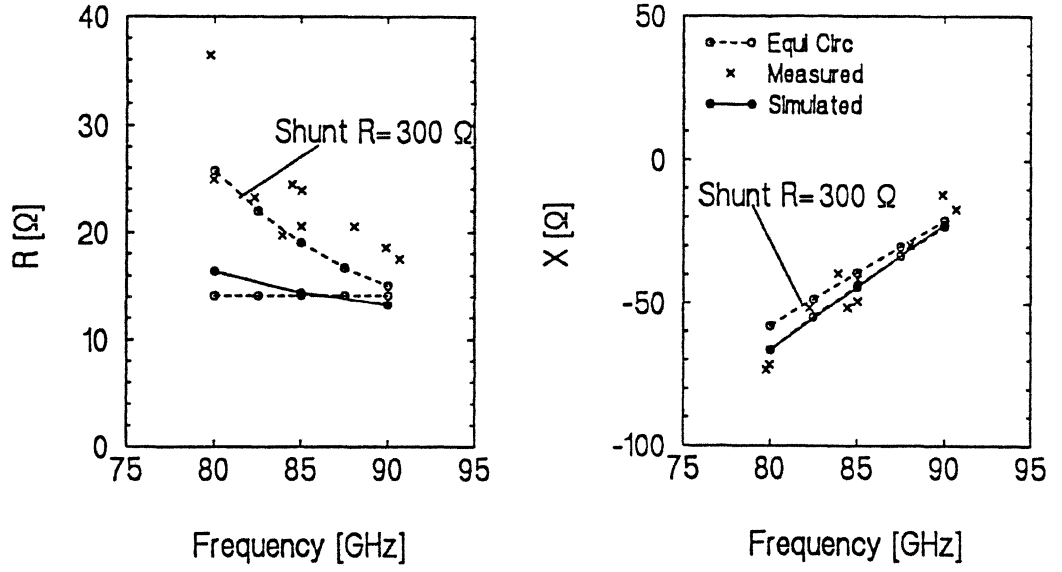

Figure 5: *Real and imaginary part of the measured and simulated de-embedded diode terminal impedances with the impedances calculated using the equivalent circuit with and without the 300 Ω shunt resistor.*

that the discrepancy between the measurements and simulations can not be explained by a reasonable waveguide loss. The effect of the limited n^+ region conductivity was studied by the FEA. In the analysis a conductivity of 1000 S/cm was used. No significant change was observed for the real part of the diode terminal impedance.

The results of the FEA of the loss in the GaAs are shown in Figure 6. This figure shows that a value of $\tan\delta = 0.3$ for the GaAs substrate does raise the simulated values quite close to the measured ones. However, because this unrealisticly large value of $\tan\delta$ is required and because the slope of the simulated curve of the real part does not seem to agree very well with the measured values, the loss in the GaAs substrate is not assumed to be the main explanation for the loss in the doubler circuit.

Since the above three sources of loss did not seem to be very likely explanations, we finally considered the dislocation layer on the back side of the chip. This layer is due to the mechanical thinning process of the diode and we assume that the surface states at the many grain boundaries cause this surface to behave like a poor conductor. The dislocation layer was simulated in the FEA by placing an infinitely thin resistive layer on the back side of the diode chip. Figure 7 shows results of these simulations. The resistance values for the layer, shown in the figure, are over the full length of the diode. Figure 7 shows that the layer has a strong effect on both the real and imaginary part of the terminal impedance. On

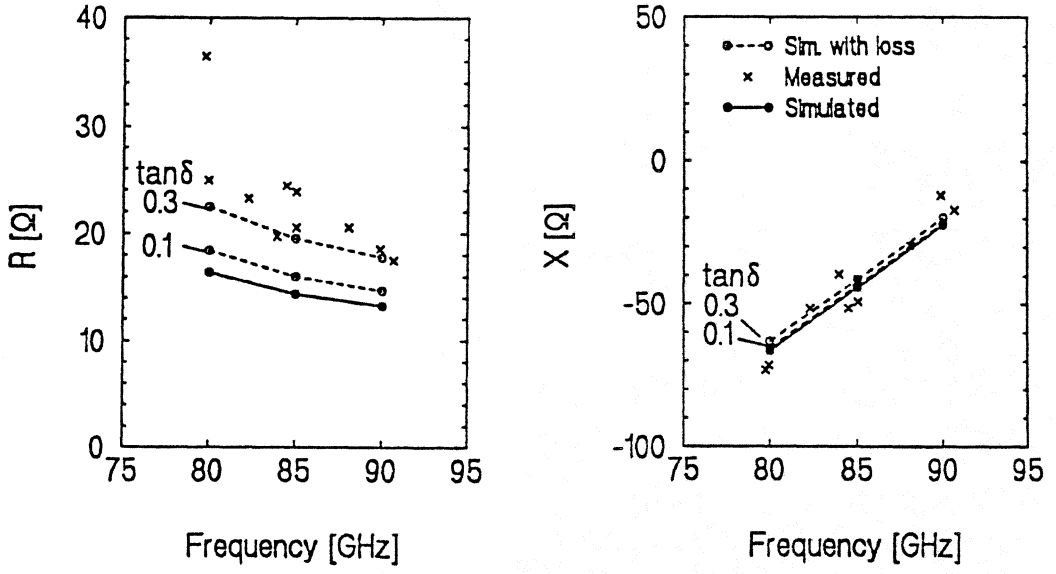

Figure 6: *Real and imaginary part of the measured and simulated de-embedded diode terminal impedances. The GaAs substrate loss is included to the simulated curves.*

the imaginary part, the layer has mainly reduced the capacitance by 23 Ω at all frequencies and resistance values. The simulated real part of the impedance is sensitive for the actual value of the resistance of the layer. Simulations with a resistive layer of 800 Ω predict very similar real part values with the measurements. This shows that the dislocation layer is a likely explanation for the high measured real parts of the diode terminal impedance. A thin and very lossy dielectric layer might better simulate the dislocation layer, because a constant shift in the imaginary part of the simulated results was caused by a lossy conductive layer.

Overall, the good agreement between the measured and simulated reactive parts has convinced us on the usefulness of finite element analysis. This is especially true after considering the great complexity of the doubler structure, simulations, and measurements.

4 Conclusions

The accuracy of previously described finite element analysis (FEA) of a planar diode multiplier [1] has been verified by careful measurements. The input impedance of the doubler, from which the diode terminal impedance was calculated, was measured between 80 and 90 GHz using a WR-10 slotted line. Before actual impedance measurements, the input match was optimized with a tuner consisting of a $\lambda_g/4$ thick piece of teflon placed in the waveguide. This was important to ensure high absorbed input power, i.e., the correct operating point

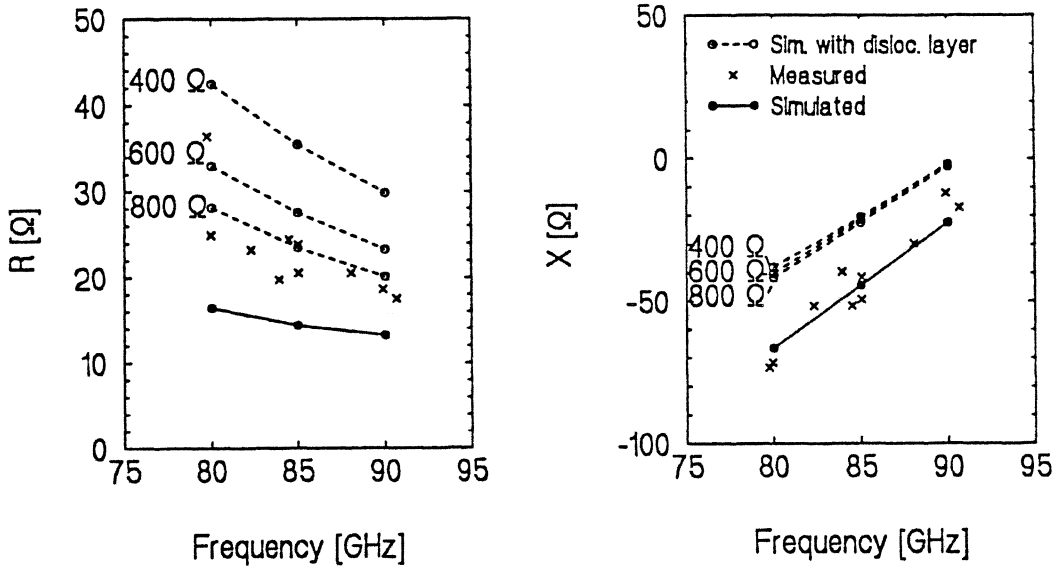

Figure 7: *Real and imaginary part of the measured and simulated de-embedded diode terminal impedances. Dislocation layer simulated by a resistive layer.*

for the doubler. The output match was optimized the same way. A good agreement was observed between the reactive part of the measured and simulated diode terminal impedances. The resistive part of the impedance did not show as good agreement as the reactive, which is due to the more complex nature of the origin of the real part, which may include losses in the diode itself. Different sources of this loss was considered. The best fit to the loss is a dislocation layer on the back side of the planar diode chip, which was formed during the mechanical thinning process of the diode.

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