# Low-Noise MOVPE-Grown Planar InGaAs Mixer Diodes

P. Marsh, D. Pavlidis, and K. Hong
Solid State Electronics Laboratory, Department of Electrical Engineering and Computer Science,
The University of Michigan, Ann Arbor, MI 48109-2122

## Abstract

InGaAs lattice-matched to InP is an excellent candidate for applications requiring high mobility and conductivity. Schottky junctions on InGaAs exhibit barriers ($\phi_b$) in the neighborhood of 0.25eV and high mobility contributes to the low n+ sheet resistances of 2.0-5Ω/□ for 1μm n+ InGaAs layers ($n_s = 1.5x10^{19}/cm^3$, $\mu_n = 1800cm^2$/volt•sec) grown with our in-house Metalorganic Vapor Phase Epitaxy (MOVPE) system. This material is therefore well suited for high-performance THz diodes since it provides low $\phi_b$, as necessary for low required LO power and has low specific contact resistance needed for reduced losses and high-frequency operation.

The design, material growth, fabrication, and characterization of InGaAs planar mixers is reported. These mixers demonstrated a state-of-the-art performance of 261K DSB noise temperature ($T_{mix}$) with a corresponding conversion loss ($L_{mix}$) of 5.4dB at LO, RF, and IF frequencies of 92GHz, 92GHz ± 1.4GHz, and 1.4GHz respectively. Planar mixer diodes were produced using a novel chemical dice process that performs all lithography and wafer thinning steps before airbridge fabrication, thus greatly reducing the possibility of damage to airbridge and anodes. The mixer diodes were quasi-optically tested while mounted on spiral antennae.

## II. Introduction

Planar mixer diodes have traditionally relied on GaAs material systems to achieve high performance at submillimeter and THz frequencies and have shown performance comparable to whisker-contacted Schottkys [1]. In recent years, improvements in growth technology have made it feasible to utilize the performance advantages offered by the InP-based material systems. The high mobility of InGaAs enables the reduction of access resistance ($R_s$). For example, a 1μm thick n+ ($n > 10^{19}/cm^3$) InGaAs layer showed a sheet resistance on the order of 2-5Ω/□. The low barrier heights ($\varphi_{be}$) of mixers using InGaAs Schottky junctions are especially useful in reducing LO power ($P_{LO}$) requirements, particularly under zero-bias conditions as required in simple antiparallel subharmonic mixer designs [2]. The InP-based system also allows for a highly-

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controlled HCl wet etch that virtually eliminates undercut in the $0\bar{1}1$ and $01\bar{1}$ directions, thus allowing for the repeatable chemical dicing obtained for the discrete mixers. Another advantage of the InP-based system is the availability of high-performance HEMT technology which can potentially be integrated with the diodes. Platinum plating is used here to produce anodes having good ideality, high $\varphi_{be}$ and low reverse leakage.

This paper covers the fabrication, characterization, and performance of planar InGaAs mixers. Section III covers mixer layer structure, fabrication and mounting. Section IV describes the test setup and extraction of mixer performance. Section V describes dc characteristics and compares measured against modeled RF performance.

# III. Layer Structure, Fabrication, and Mixer Mounting

Mixer diodes were grown at 570°C via in-house MOCVD using TMG, TMI, and $AsH_3$ precursors with Si (disilane) doping. Figure 1 shows the layer structure of the mixer diodes characterized here. The 1μm n+ layer is doped to approximately $2x10^{19}/cm^3$ and the 800Å active layer is doped to $2x10^{17}/cm^3$. The authors' previous InP-based mixer designs made use of an InP or InAlAs layer beneath the Schottky contact to raise $\phi_b$ and reduce reverse leakage [3]. However, mixers having active layers consisting completely of InGaAs gave much lower series resistance than InGaAs-InP or InGaAs-InAlAs structures but also had much higher leakage. The use of plated Pt Schottkys has since greatly reduced reverse leakage while preserving the benefits of an all-InGaAs structure.

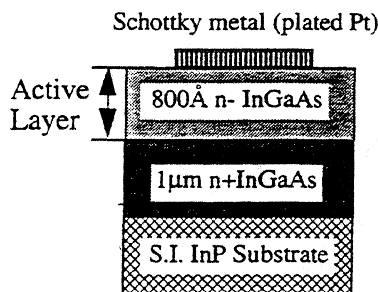


Figure 1. Layer structure of the mixer diodes. The n+ InGaAs layer provides low sheet and ohmic contact resistance. The n- layer is Si doped to $2x10^{17}/cm^3$. A plated Pt anode improves Schottky quality.

Discrete devices are fabricated using a process similar to that covered in [3]-[5]. First, ohmic and interconnect metal are deposited as shown in Figure 2A. Optionally, ohmic metal alone may be deposited in place of the interconnect - as was the case here. Next, the wafer frontside is attached to a cover glass using black wax. The wafer is then thinned to 50μm, using concentrated HCl (37%) in a process similar to that of [4], [5]. To continue processing, it is necessary to attach the thinned wafer to a silicon substrate (Figure 2B). Wafer attachment is accomplished using Norland NOR 121® glue, spun on the wafer backside and oven-cured. The cover glass and black wax are removed using concentrated HF and trichloroethylene (TCE) respectively. Next, pillar photoresist (P.R.) is spun on. Pillars and anode regions are opened. Then the anodes are Pt plated using

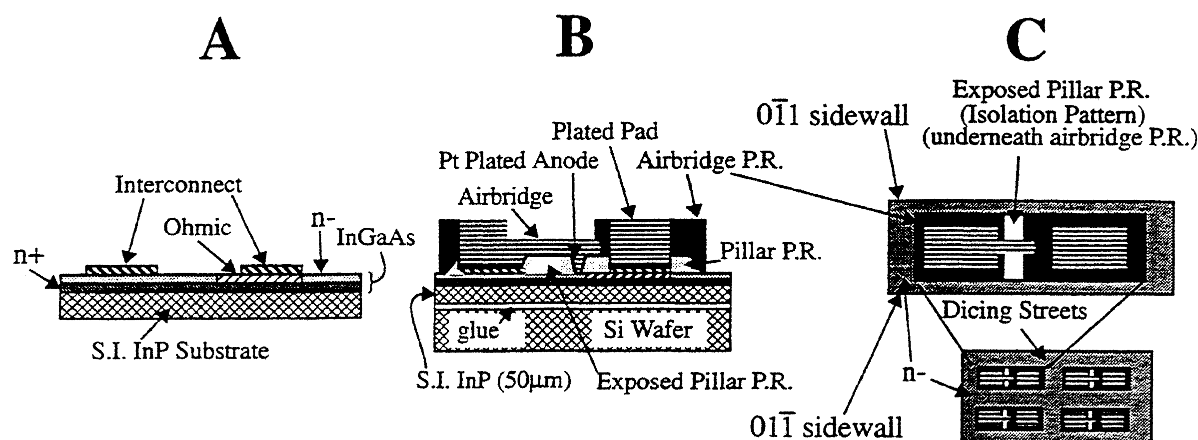


Figure 2. Discrete mixer fabrication process. The wafer is thinned after the ohmic and interconnect steps. Here, the interconnect and ohmic were both deposited as ohmic metal to save a step. Multiple exposures of both pillar and airbridge photoresist (P.R.) allow for definition of the dicing streets. The possibility of damage to the anode contacts is greatly reduced by performing all lithography before forming the airbridges. Contact pads are plated thicker than the airbridges to further increase mechanical ruggedness.

Enthone Platanex III® Pt plating solution. Dicing streets are then opened in the pillar P.R., followed by a contour bake. A final exposure of the pillar P.R. defines the isolation pattern (Figure 2B). Development of the isolation pattern is delayed until the end of the process to allow the isolation etch to then remove n+ between the diode pads. Ti/Au/Ti pillar metal is then deposited and 3μm airbridge P.R. is spun on. The interconnect mask is used to open the pad areas, allowing them to receive a thick Au plate. Subsequently, the airbridge areas are exposed but not immediately developed. After heavily plating the pad areas, the airbridge regions are developed and the dicing streets are exposed into the airbridge P.R. Airbridges are then formed via Au plating. Development of the dicing streets follows. A combination of wet etch and ion milling then removes the pillar metal from the dicing streets, exposing bare n- InGaAs. Dicing is then subsequently performed by first removing the InGaAs with $H_2O$:$H_2O_2$:$H_3PO_4$ (8:1:1) then using 37% HCl to etch the 50μm thick InP, down to the Si wafer. During this dicing process, the pillar P.R. and anode regions are well-protected by the airbridge P.R. and dicing is carried out through a mask of InGaAs covered by photoresist. The InGaAs mask virtually eliminates undercut in the $0\bar{1}1$ and $01\bar{1}$ directions and gives vertical $0\bar{1}1$/ $01\bar{1}$ sidewalls. Undercut occurring at the ends of the device is very predictable. Profiles resulting from the chemical dicing enhance the handling and mountability of the devices. The process continues with flood exposure and development of the airbridge resist. The remaining pillar metal is removed via wet etching and ion milling. At this point the InP wafer becomes a set of discrete diodes held on the Si wafer by the Norland® glue. Finally, a development step removes the previously exposed pillar P.R. beneath the airbridge to enable electrical separation of the diode pads via the isolation etch of the InGaAs. The isolation

etch yields operational, discrete mixer diodes. These diodes may be readily plucked from the Si wafer after soaking them in acetone for about 24 hours.

A spiral antenna topology [6] eases mixer characterization by virtue of broadbanded performance, predictable impedance, and ease of coupling both LO and RF signals with predictable losses. Spiral antennae for the discrete mixers are fabricated on mechanical-grade semiinsulating (S.I.) GaAs. The antennae are Au plated to improve contacting. Diodes are mounted in a flip-chip fashion as illustrated in Figure 3. Excellent electrical and mechanical bonding are provided by pressing the diode pads into indium pieces placed onto the antenna terminals. This room-temperature process avoids possible heat damage and/or high resistance that might occur from the use of conductive epoxies or solder.

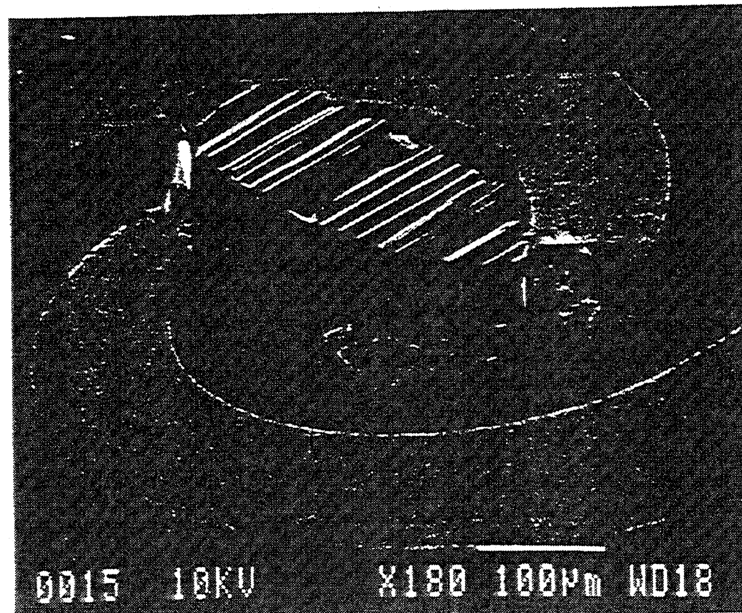


Figure 3. **SEM shot of a discrete mixer, having the diode flip-chip mounted onto the spiral antenna with indium.**

The antenna wafer is positioned with its backside contacting a silicon substrate lens such that the antenna lies at the lens' focal point. IF is taken off at the ends of the antenna terminals.

# IV. Test Setup and Extraction of Mixer Performance

Measurement results are reported here for two planar InGaAs mixers, namely: 7c6 and 7b3 having anode diameters of 1.9μm and 3.5μm respectively. Mixer performance is defined by the double sideband (DSB) RF port noise temperature, $T_{mix}$, and single sideband (SSB) RF to IF conversion loss, $L_{mix}$. $T_{mix}$ is defined as the temperature of a noiseless mixer's blackbody RF load such that it would produce the same noise power at its IF port as the actual mixer under test with an RF load at 0K. $T_{mix}$ and $L_{mix}$ are evaluated using the quasi-optical setup shown in Figure 4. The mixer's spiral antenna couples well to both horizontal and vertical polarizations which serves to simplify the simultaneous coupling of LO and blackbody RF radiation to the mixer diode. A polarization grid of closely-spaced wires reflects the vertically-polarized LO signal into the mixer Si lens while the horizontal component of the RF signal passes through the polarizer. The Si lens is aligned by pulsing the LO and detecting the pulsed signal at the IF port. The IF chain is calibrated to enable measurement of the uncorrected IF noise temperature $T_{im}$. $T_i$, the equivalent

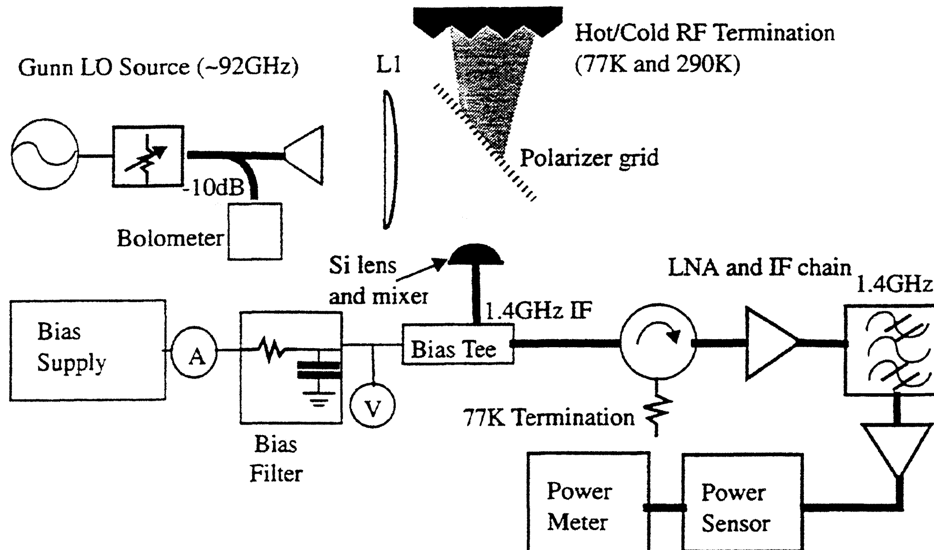


Figure 4. Quasi-optical test setup for evaluation of mixer performance. A low-noise IF chain is calibrated to measure the mixer's IF noise temperature ($T_i$). The mixer's performance is then extracted from known system losses and the variation of $T_i$ as a function of the RF load temperature ($T_r$).

matched IF noise temperature, is extracted via the relation: $T_i = \frac{T_{im} - T_c \cdot \Gamma_i^2}{1 - \Gamma_i^2}$ Where $T_c$ is the effective temperature of the circulator termination and $\Gamma_i$ is the IF reflection coefficient. Therefore:

$$G_m = \frac{\Delta T_{im}}{(1-\Gamma_i^2)(1-\Gamma_r^2) G_a G_p \Delta T_r}$$

and

$$T_{mix} = \frac{T_i}{G_m} - \underbrace{(1-G_a) T_o + (1-G_a)\Gamma_r^2 T_o G_a}_{\text{Si lens}} + \underbrace{(1-G_p)(1-\Gamma_r^2) T_o G_a}_{\text{Polarization Grid}} + \underbrace{(1-\Gamma_r^2) G_a G_p T_{rh}}_{\text{RF Load}}$$

Noise contributions

Where $G_m = 2/L_{mix}$, $T_o = 290K$ (room temperature), $G_a = 0.871$ = reciprocal of the Si lens loss due to backside radiation and dielectric loss, $\Gamma_r = 0.555$ = reflection coefficient of the Si lens, $G_p = 0.5$ which represents the RF coupling loss due to insertion of a linearly-polarized RF signal into a spiral antenna, $T_{rh} = 295K$ = hot RF load temperature, and $\Delta T_r$ = 295K-77K = difference between hot and cold RF load temperatures. Here, $T_{im}$ is measured with a room temperature RF load. LO power ($P_{LO}$) was determined by obtaining it from a use of a harmonic balance program [7] used with the measured diode I-V, current, and dc bias voltage under LO drive. The $P_{LO}$ extracted this way was found to be 3.5dB ± 1.5dB lower than that read by the bolometer, i.e. about 4-6dB lower than that accounted for from the quasi-optical setup losses. However, confidence is inspired by the consistency of the discrepancy between the bolometer readings and extracted $P_{LO}$ across nearly all bias, $P_{LO}$, and anode diameters measured; for both preliminary unreported results and the results reported here.

IF reflection, polarization losses, and Si lens losses and reflections were removed from the calculations of measured $T_{mix}$ and $L_{mix}$. No attempt was made to remove the effect of the mismatch between diode and antenna.

# V. Measured Performance

Figure 5 illustrates dc characteristics of the mixer diodes. At 0.22-0.28eV, $\phi_b$ is considerably below that of GaAs diodes (0.8-0.9eV), thus lowering $P_{LO}$. The ideality factor ($\eta$) is good at 1.2 and the highest cutoff frequency ($f_c = 1/(2\pi R_s C_{jo})$ is > 7THz. The zero-bias capacitances, $C_{jo}$, were estimated from depletion-layer thickness calculations based on the $2 \times 10^{17}/cm^3$ doping of the n- InGaAs layer. The series resistance, $R_s$; ideality, $\eta$; and Schottky barrier height, $\phi_b$; and reverse saturation current, $I_s$, were determined from the I-V curves.

| Diode Designation | Wafer Designation | Diameter (μm) | $C_{jo}$ (fF)(est.) | $R_s$ (Ω) | η | $\phi_b$ (eV) | $I_s$ (μA) | $f_c$ (THz) |
|---|---|---|---|---|---|---|---|---|
| 7c6 | U423 (discrete) | 1.9 | 7.4 | 5.5 | 1.2 | 0.27 | 0.25 | 3.9 |
| 7b3 | U423 (discrete) | 3.5 | 27.85 | 0.8 | 1.2 | 0.22 | 5.5 | 7.14 |

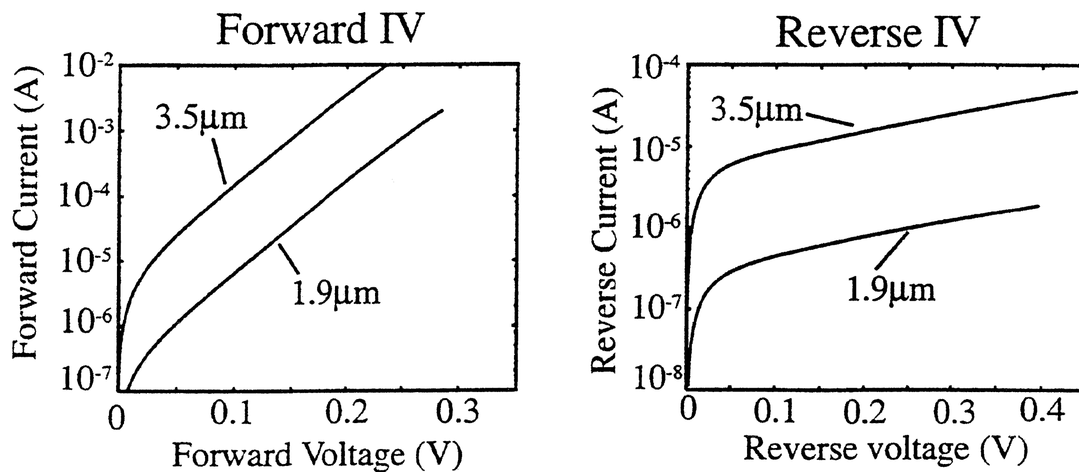


Figure 5. DC Characteristics of the measured mixer diodes. Diodes exhibit low $\phi_b$ with low η and low reverse leakage (for 1.9μm diodes).

Figure 6, illustrates measured performance of mixers 7c6 and 7B3 compared against the corresponding harmonic-balance simulated results based on the mixer simulator of [7]. DC bias was set to optimize noise temperature. The simulator was loaded with the diodes' dc values of $R_s$; $C_{jo}$; η; and reverse saturation current, $I_s$. This simulator obtains noise calculations exclusively from shot and $R_s$'s thermal noise. Since the theoretical and measured data agree well, especially for diode 7c6, it appears that the real diodes are relatively free of significant noise due to hot electron effects, trapping, or other sources. Insignificant levels of hot electron noise allow these diodes to obtain excellent performance ($T_{mix}$ < 500K) over a 1:5 range of $P_{LO}$. Other measurements showed a weakened dependency of noise performance and $P_{LO}$ for $P_{LO}$ > 440μW. Zero-bias performance for the 1.9μm diode (7c6) is excellent, $T_{mix}$<500K for $P_{LO}$ > 220μW.

The smaller anode device (7c6) performs better largely due to its RF and LO impedances being closer to the antenna impedance of 71Ω.

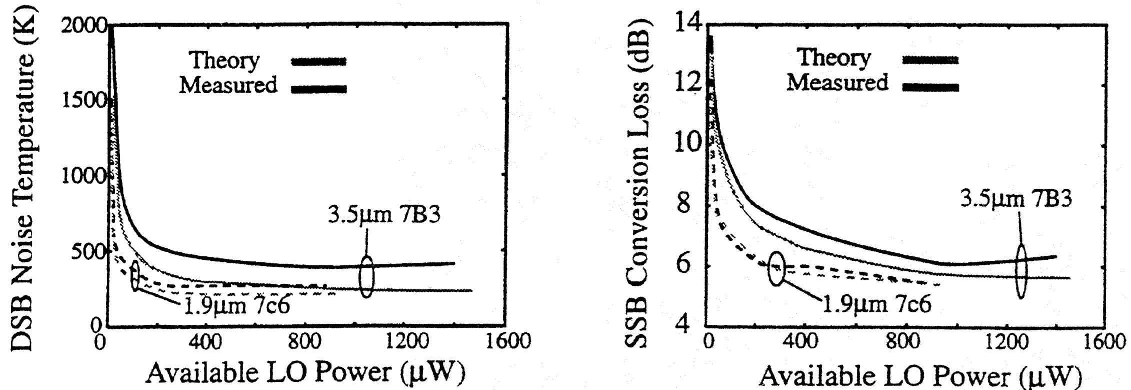


Figure 6. Measured vs. modeled performance for mixers. DC bias was set to minimize the mixers' noise temperature. Noise temperature approaches its minimum value for $P_{LO} > 180\mu W$. Good agreement of measured and modeled performance indicates a low level of hot electron and trap noise.

# VI. Conclusions

Planar InGaAs mixers having state-of-the-art noise performance have been fabricated and demonstrated at 92GHz. Pt plated Schottkys have been shown effective at achieving low (~0.25eV) $\phi_b$ while maintaining low reverse currents on the $n = 2x10^{17}/cm^3$ InGaAs. DSB noise temperature ($T_{mix}$) and SSB conversion loss ($L_{mix}$) were 261K and 5.4dB respectively @ $P_{LO}$ = 891μW for a mixer (7c6) having a 1.9μm anode diameter. This mixer gave $T_{mix}$ = 451K, and $L_{mix}$ = 8dB @ $P_{LO}$ = 44μW; $T_{mix}$ = 271K, and $L_{mix}$ = 6dB @ $P_{LO}$ = 223μW; and a zero-bias performance of $T_{mix}$ ~ 450K, and $L_{mix}$ = 8dB @ $P_{LO}$ = 225μW. These InGaAs mixers show very little hot electron or trap noise contribution to $T_{mix}$. Therefore, they have demonstrated very low noise performance over a 1:5 range of $P_{LO}$. Performance appears to depend on the matching of the mixers' RF impedance to that presented by the spiral antenna, i.e. 71Ω. This likely was the reason the 1.9 diode outperformed the 3.5μm diode. For $P_{LO}$ > 220μW and an anode diameter of 1.9μm, the mixer's performance is only a weak function of dc bias. These InGaAs mixer results compare favorably to that of state-of-art planar GaAs mixers [1] in waveguide fixtures.

These results indicate that InGaAs mixers hold promise in submillimeter and THz receiver applications. Their low $\phi_b$ and consequently low $P_{LO}$ requirements reduce the problem of supplying LO at high frequencies. The low hot electron noise is expected to have a large impact on submillimeter and THz noise performance. The etch and undercut controllability of InGaAs-masked InP points to possible micromachining of waveguides etc. in the InP substrates. Finally the availability of high-performance HEMTs and HBTs on InP-based systems could facilitate integration of RF and IF functions on the same InP wafer.

## Acknowledgments:

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