# Electrolytic Deposition Techniques For The Fabrication Of Submicron Anodes

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**Abstract**

Small-area anodes of whisker contacted Schottky diodes as well as planar Schottky diodes usually are deposited by electroplating techniques. With shrinking anode areas, the physical structure of the deposited metal becomes increasingly important. Therefore, it is essential to investigate the influence of the deposition parameters on the diode performance in order to be capable of fabricating submicron anodes with improved electrical performance.

A comparison of DC- and pulse-plating techniques is presented and the influence of parameters such as deposition temperature, current density, and metal film thickness on the diode I/V characteristics is experimentally investigated. It is shown that non-optimized deposition parameters lead to degraded diode performance, especially with small anode diameters. Therefore, the influence of the diode diameter is also taken into account for the optimization of the electrolytic deposition. A number of experiments demonstrate that variations of the plating process especially affect the ideality factor and the series resistance of the diodes.

## 1. Introduction

Contacts to semiconductors have been a topic of interest for more than five decades [1]. Especially for applications at high frequencies, the nonlinear space charge properties of metal-semiconductor contacts are utilized in MeSFET's, HEMT's and Schottky mixer and varactor diodes for a large variety of applications [2]. It is a matter of fact that the quality of the metal-semiconductor interface determines the electrical performance and the reliability of the devices. When device operation at submillimeter wavelengths is envisaged, the required area of the metal-semiconductor contacts are so small that only optimized metal deposition techniques enable the reliable fabrication. GaAs Schottky mixer diodes for THz operation have anode diameters between 0.8 μm and 0.25 μm, which means contact areas between 0.5 $\mu m^2$ and 0.05 $\mu m^2$ [3]. Due to a number of advantages, electrolytic deposition techniques are used for the fabrication of the anodes.

The requirements for THz Schottky diodes with such small anodes from the electrical point of view are near-ideal I/V characteristics and low-noise performance. Another item of great importance is of course the reliability of the contacts and the yield during fabrication. Especially for planar diodes where only one anode per device is available, in contrast to whiskered devices with thousands of anodes per chip, this item is of major importance. It has already been shown earlier that small deviations from a near-ideal I/V characteristic caused by non-optimized Schottky metal deposition lead to a reduced device reliability [4].

This paper presents results on Schottky contacts fabricated by DC- and pulse plating techniques. The influence of the most important deposition parameters on the device characteristics is investigated and an optimized process for the fabrication of submicron Pt anodes is described.

## 2. Experimental

The fundamentals of electrodeposition of metals on semiconductors are well understood for some decades and the metal growth generally is considered as a simple cathodic reduction [5,6].

$$Oxd_{(l)} + ne^- \rightarrow Red_{(l)}$$

which reads in the case of Pt as follows:

$$Pt^{4+} + 4e^- \rightarrow Pt$$

It is the large number of electrochemical and chemical reactions and side reactions in connection with the possible deposition parameters which makes this field extremely difficult

for the theoretical investigation of realistic structures [7]. Therefore, this study concentrates on experimental results. In the literature three approaches for the electrodeposition of metals on semiconductors are described:

- Current at a controlled potential (potentiostatic technique) [7,8]
- Electrode potential under constant current (galvanostatic technique) [4]
- Pulse-plating techniques [9,10]

Because of their importance for the fabrication of whiskered and planar Schottky diodes, this work concentrates on galvanostatic and pulse plating techniques.

We have used a number of different wafers for the investigations with doping concentrations between $2 \cdot 10^{16}$ $cm^{-3}$ and $1 \cdot 10^{18}$ $cm^{-3}$ and an epi-layer thickness between 300 nm and 50 nm, respectively, such as commonly utilized for the fabrication of mixer and varactor diodes. The anode diameters have been varied between 7 µm and 0.5 µm. All anodes were fabricated according to our standard diode process [11]. This means that the GaAs surface is electrochemically etched prior to the platinum deposition. This etch technique results in a smooth and oxide-free interface [12] because etching and Pt deposition are performed in-situ in the Pt electrolyte. The Pt solution[1] is based on sulfuric and phosphoric acid with a pH-value of 0.2 and 2 g Pt/l. The recommended current density for the galvanostatic deposition is 0.4 $mA/mm^2$. The pulse generator for the pulse plating generates voltage pulses with an amplitude between 0-20 V, pulse width 0.2 -10 µs, and pulse rate 1-4 ms.

The fabricated Pt/GaAs diodes have been electrically characterized by I/V- and C/V-measurements. Usually, the Schottky anodes consist of a Pt/Au contact. The Pt layer forms the Schottky contact to the GaAs and determines the diode performance whereas the Au layer only provides a good contact to the whisker wire or to the airbridge. Therefore, all diodes fabricated in the course of this work only have a Pt layer. This allows additionally the investigation of the deposited Pt layers with the SEM.

## 3. Results and Discussion

### 3.1 DC-plating

For a given Pt solution, the DC-plating deposition parameters are the electrolyte temperature $T_{Pt}$ and the current density during the deposition $J_{DC}$. Fig. 1 shows the influence of $T_{Pt}$ on the forward I/V characteristics of Schottky diodes (anode diameter 6.7 µm, epi-layer doping $1 \cdot$

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$10^{17}$ $cm^{-3}$). At very small diode currents ($I_D$ < 1 nA) occurs a deviation from the ideal diode behavior. This deviation (excess current) is more pronounced at $T_{Pt}$ = 40 °C and reduces with increasing $T_{Pt}$. This could be explained that with increasing electrolyte temperature also the thermal energy of the metal ions increases. This causes a more homogeneous distribution of the $Pt^{4+}$-ions on the GaAs surface. A further increase of $T_{Pt}$ has lead to a very inhomogeneous deposition. The reason is that the anodic pulse etching which is performed prior to the Pt deposition at high $T_{Pt}$ preferably takes place at surface crystal defects . So at some areas at the free GaAs surface the epi-layer is removed with a high etch rate which subsequently leads to a preferred Pt deposition on these areas. Therefore, the combined pulse etching and DC-plating process is limited to a $T_{Pt}$ of 60 °C. The diodes fabricated at 60 °C also exhibit a slightly better n-value (1.13) and smaller series resistance (20 Ω) compared to the deposition at lower $T_{Pt}$ (n=1.17, $R_S$=23 Ω). Therefore, all subsequent experiments have been carried out at $T_{Pt}$ = 60 °C.

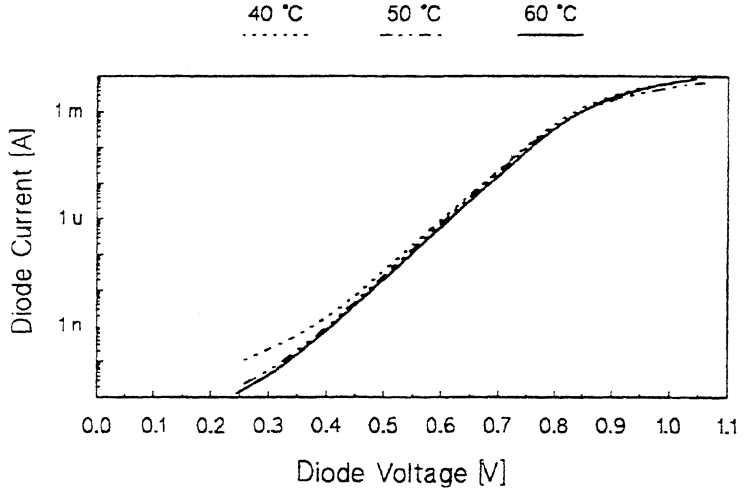



Fig.1: DC-plating: Influence of the deposition temperature on the diode I/V characteristics

The influence of the deposition current density on the diode characteristics is discussed in fig. 2 (anode diameter 6.7 µm, epi-layer doping 1· $10^{17}$ $cm^{-3}$). Generally, the current density $J_{DC}$ is the deposition parameter which has the strongest effect on the metallurgical quality of the deposited metal film. If $J_{DC}$ is too high, hydrogen ions contribute considerably to the ion current and are incorporated into the deposited film which must be avoided because it leads to Pt films with reduced adhesion and higher brittleness. On the other hand, if $J_{DC}$ is too small the number of Pt growth centers on the GaAs surface decreases which leads to a reduced homogeneity. The best results in our study have been obtained with deposition current densities $J_{DC}$ between 2 and 3 $mA/mm^2$ . The deposition at 2.4 $mA/ mm^2$ leads to a reduction of n to 1.09 compared to 1.11 for a current density of 1.2 $mA/ mm^2$. More pronounced is the reduction of the series resistance which is in the order of 3-4 Ω. Since the higher current density also leads to a higher Pt growth rate, the deposition time $t_{DC}$ was chosen such that the thickness of the Pt was identical for all samples ($J_{DC}$ · $t_{DC}$ = const.).

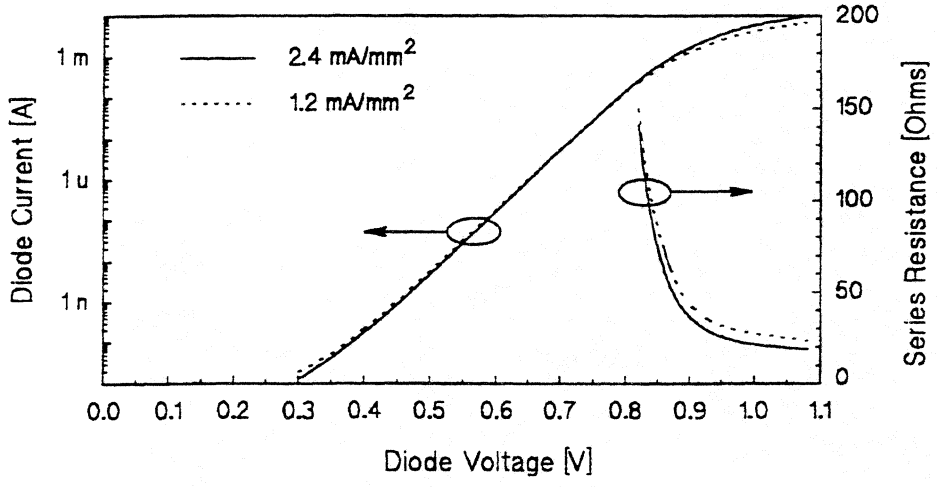



Fig. 2: DC-plating: Influence of the deposition current density on the diode I/V characteristics

The experiments have shown that DC-Plating should be carried out at $T_{Pt}$ = 60 °C and $J_{DC}$ = 2-3 mA/mm$^2$ . Additionally, it has been revealed that all DC-plated anodes exhibit a small excess current at small bias which is the more pronounced the smaller the anode diameter is. However, the fabrication of homogeneous Pt anodes with diameters smaller than 1.5 µm requires due to the small contact area a larger density of Pt growth centers (nuclei). This can be achieved by an increase of $J_{DC}$ but as demonstrated, $J_{DC}$ is limited to a certain range in order to grow Pt films with sufficiently good quality. Therefore, pulse plating techniques should be applied for the fabrication of submicron anodes [10].

### 3.2 Pulse plating

Up to now, there exists only very few insight in which way the pulse parameters influence the deposited films and the diode performance. The following paragraph therefore shows in how far the pulse parameters (pulse width $\Delta t_P$, pulse amplitude $V_P$, number of pulses $N_P$) affect the diode performance.

Fig. 3 (anode diameter 6.7 µm, epi-layer doping 2 · $10^{16}$ cm$^{-3}$, exponentially increasing towards the substrate) shows the current dependent diode ideality factor n as a function of the pulse amplitude. Best results have been achieved with $V_P$=17 V. These diodes exhibit an ideal behavior with a minimum n of 1.08 down to currents of less than 40 pA. This demonstrates already the difference to dc-plated diodes which even with optimized deposition parameters (see above) have a small excess current (=> slightly increased ideality factor) at pA-currents.

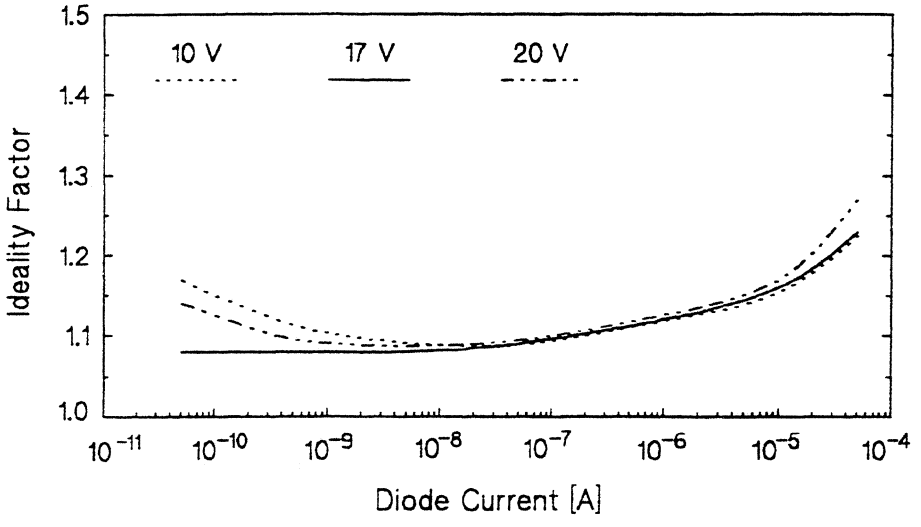



Fig. 3: Pulse plating: Influence of the pulse amplitude on the diode ideality factor

The next parameter which has to be investigated is the pulse width. The utilized pulse generator delivers pulse widths from 200 ns to 10 µs. For the anodic pulse etching prior to the Pt deposition the pulse width has to be as short as possible in order to achieve a resolution of 1 nm /pulse. This is required for the controlled etching of thin epi-layers. The experiments have revealed that for the subsequent cathodic deposition a pulse width of about 1 µs seems to be optimum. Fig. 4 (anode diameter 6.7 µm, epi-layer doping $2 \cdot 10^{16}$ $cm^{-3}$, exponentially increasing towards the substrate) shows the ideality factor and series resistance as a function of the diode current for a pulse width of 1 µs and 10 µs. It can be seen that the minimum ideality factor is the same for both curves (n=1.07). A slight deviation occurs in the current range above 10 µA where the series resistance begins influence the I/V curve. This behavior is also expressed in the curves for the series resistance. The diode fabricated by application of 1 µs-pulses exhibits a series resistance which is approx. 2 Ω smaller than that of the 10 µs-pulses diode. This could be explained by the assumption that for pulse widths > 10 µs saturation effects at the electrolyte/GaAs surface start to play a role. Of course, also pulse widths shorter than 1 µs can be utilized but since the generation of such pulses is more difficult there is no need to do so.

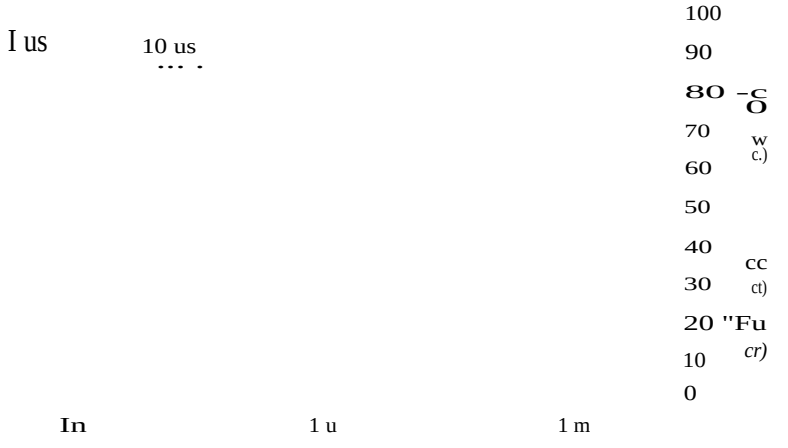
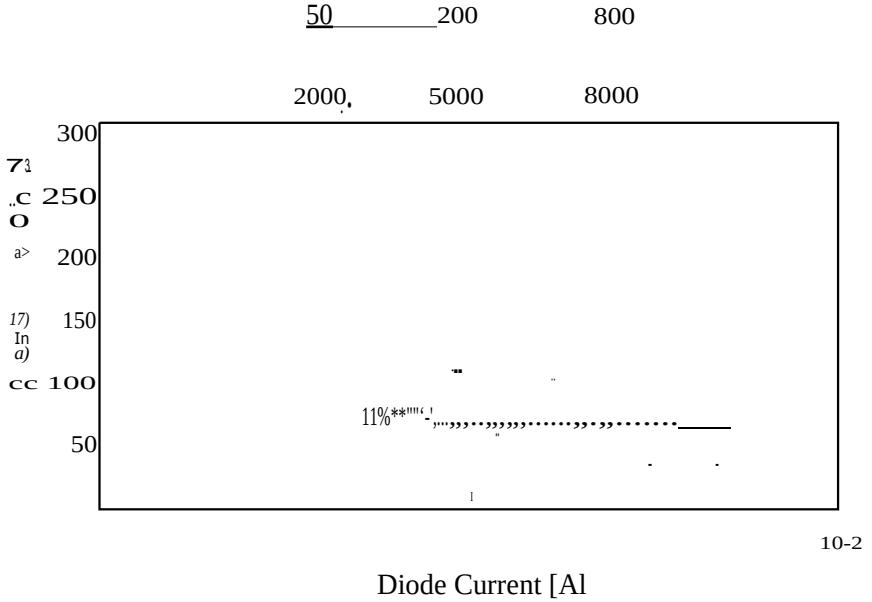



Fig. 4: Pulse plating: Influence of the pulse width on the diode ideality factor and series resistance

The influence of the Pt thickness is illustrated in fig. 5 (anode diameter 6.7 gm, epi-layer doping $2 \cdot 10^{16}$ $cm^{-3}$, exponentially increasing towards the substrate). One diode chip with -varactor diodes has been fabricated for this test. In a first step 50 pulses of Pt plating have been applied_ Subsequently, the IN characteristics was measured. Then the diode chip was again immersed into the Pt solution and another 70 pulses were applied. Thus, plating pulses were applied and IN curves measured until stable curves were obtained. It clearly can be stated that already after a small number of pulses the Schottky barrier is stable and is not affected by a further growth of the Pt layer. This is obvious due to the constant ideality factor of 1.08 which could be measured for all curves. However, a significant change occurs in the series resistance which decreases with the increasing number of pulses, shown in fig. 6 (120 C ^ for 50 pulses, 20 C2, for 8000 pulses). For Np > 2000 the series resistance decreases very slowly and for Np > 5000 it remains constant at a minimum value. This means that at least 5000 plating pulses should be applied which corresponds to a Pt thickness of approximately 50 nm.

Diode Voltage [V]

Fig. 5: Pulse plating: IN characteristics as a function ofthe number of pulses




Diode Current [Al

Fig. 6: Pulse plating: Series resistance as a function of number of pulses

It is commonly accepted that with decreasing mode diameter the minirnum ideality factor increases but no investigations on this have been made. The higher n values of small area contacts is due to the increasing influence of edge effects [13] but also due to the increasing influence of the anode homogeneity [14,15]. This behavior also can be seen in fig. 7 where the ideality factor versus the current density with the anode diameter as parameter is depicted. Diodes with diameters varying between 6.7 pm and 0.7 pm have been fabricated simultaneously on the same chip. The 6.7p.m-diodes behave almost ideal with a n of 1.06 and no excess currents at small bias. With shrinking diameter the minimum n increases and additionally the behavior at small currents becomes more non-ideal. Since the diodes have been fabricated with the optimized pulse plating process which delivers very good results even for 0.5Rm-diodes (see fig. 8), this tin of 0.08 between 6.7pm and 0.7pm-anodes can be a contribution due to the increasing influence of edge effects. The fact that at high current densities the n values of the large diodes increase faster is due to the influence of the series resistance at mA-currents. This demonstrates that even with an optimized fabrication process diodes with diameters smaller than approximately 1.5 pm exhibit a higher ideality factor which cannot be reduced.

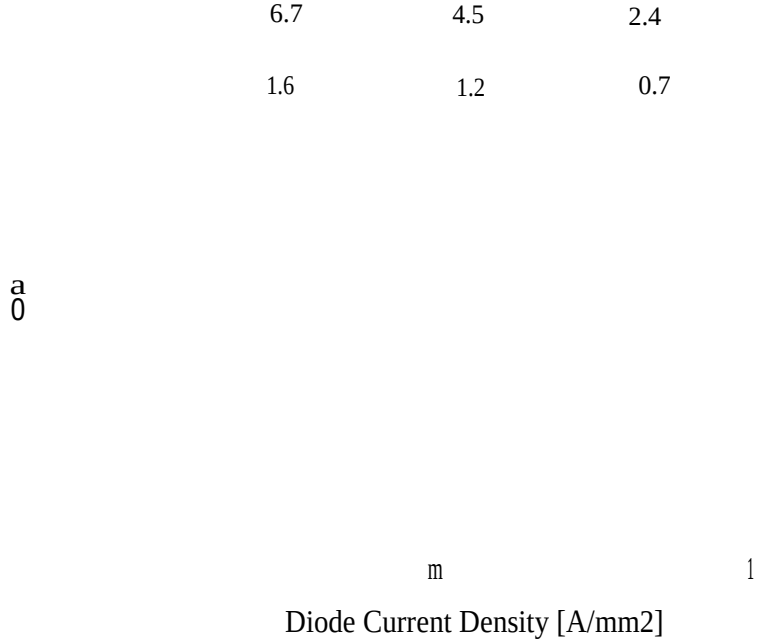



Fig.7: Pulse plating: Area dependence of the ideality factor

Fig. 8 finally shows a SEM photograph of a 0.5µm Schottky diode fabricated according to the optimized pulse plating process with the following parameters: $V_P$=17 V, $\Delta t_P$=1 µs, $N_P$=8000, $T_{Pt}$=60 °C. This diode chip has an $In_{0.02}Ga_{0.48}As$ epi-layer with a doping concentration of 1·$10^{18}$ $cm^{-3}$. The measured diode parameters are as follows: $C_{j0}$=0.9 fF, n=1.28, $R_S$=20 Ω, $V_{br}$= -2.9 V.

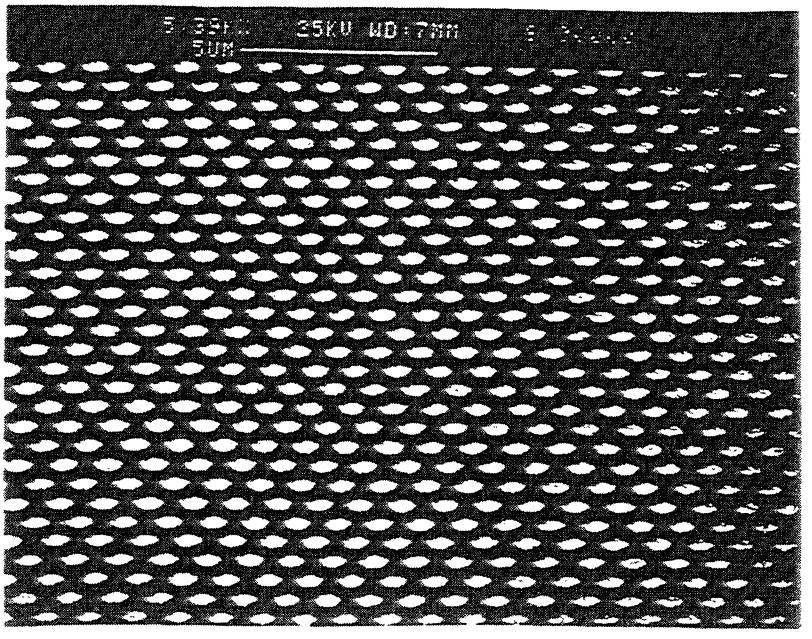



Fig. 8: SEM-photograph of a 0.5µm Schottky diode

## 4. Conclusions

The reliable fabrication of whiskered and planar submicron Schottky diodes with near-ideal electrical performance is still a technological challenge. Therefore, the Pt deposition process has to be investigated. This paper shows the influence of plating parameters on the I/V characteristics of diodes with varying diameters. It is demonstrated that submicron anodes should be fabricated with a pulse plating process.

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