Micromachined Millimeter-wave SIS-mixers

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A heterodyne mixer with a micromachined horn antenna and a superconductorisolator-superconductor tunnel junction as mixing element is tested in the 75-115 GHz frequency range. Experimental results show that the SIS mixers can be operated on thin Si_3N_4 membranes in a vacuum environment, and that the micromachined horn antenna can withstand repeated thermal cycling. A lowest DSB receiver noise temperature of 70 K is measured at 102 GHz with a 3-dB bandwidth of 15 GHz. Analysis of the noise measurements shows that the receiver noise is mainly limited by the reflection loss due to the capacitance of the tunnel junctions and therefore can be further improved by the use of integrated tuning elements.

1 Introduction

Micromachined integrated horn antennas consist of a dipole antenna suspended on a thin $(\sim 1 \ \mu m)$ Si₃N₄ dielectric membrane inside a pyramidal cavity etched in silicon [1]. In the construction of this type of antenna, standard whole-wafer Si photolithography and well established anisotropic etching processes are used. We investigate the combination of micromachining with Nb-based fabrication technology and cryogenic operations, for the development of superconducting heterodyne receivers for millimeter and sub-millimeter wavelengths.

Several reasons make a micromachined horn-antenna attractive in comparison with conventional waveguide and open-structure antennas. (a) The feasibility of micromachined horn antennas for imaging array applications, (b) the relative ease (and low cost) of fabrication of very accurate (sub-)millimeter-wave cavities, (c) the use at frequencies above 1 THz, where machined waveguides become inconveniently small and difficult to fabricate and open structure antennas will suffer from substrate losses, (d) the possibilities of integrating a mixing element with (super- or semi-conducting) electronics, for example SQUID IF-amplifiers or Flux-Flow oscillators.

The development of heterodyne receivers with room-temperature semiconductor GaAs Schottky diode detectors for use at millimeter and sub-millimeter wavelengths [2] has shown the feasibility of micromachined integrated horn receivers. A similar design is used in this work in the construction of micromachined millimeter-wave heterodyne mixers using super-conducting tunnel junctions (SIS-junctions) as mixing elements. Heterodyne receivers based on SIS-junctions are the most sensitive receivers for frequencies from 36 GHz up to 840 GHz, both in waveguide [3] and quasi-optical designs [4], with noise performance limited by fundamental quantum-noise limits. The current state-of-the-art waveguide and quasi-optical receivers for the 90-115 frequency range have DSB noise temperatures of 20 K and 35 K, respectively [5, 6, 7, 8, 9].

This paper reports on the first measurements of a micromachined SIS mixer for the 75-115 GHz frequency range. Section 2 describes the receiver design. The fabrication process of the SIS-junctions and the micromachined horns is described in Section 3. Results of cryogenic testing, a Fourier Transform Spectrometer measurement and actual receiver noise measurements of a 75-115 GHz mixer are given in Section 4.

2 Receiver Design

The geometry and main dimensions of the horn-aperture and the dipole antenna are shown in Figs. 1 and 2, where the dimensions are expressed in units of wavelength of the design frequency. The 70° opening angle of a horn cavity, inherent to the [111] crystal planes of Si, is far too large for direct application in single-element or array receivers. To improve the wide beam pattern due to the large flare angle, an electroformed horn section with a 9° flare angle is placed in front of the micromachined section. Measurements on this quasi-integrated horn show a 97% Gaussian beam-coupling, a 34° 10-dB beam-width and a - 27 dB side lobe level [10]. The actual dimensions of the micromachined horn-antenna used in this work (based on the work in [2] and [11]) are shown in Table 1. The dipole length and distance from the apex of the pyramidal horn are chosen to give a 35 Ω antenna impedance at a center frequency of 90 GHz. The co-planar stripline used to bias the SIS-junction and to couple the IF-signals (Fig. 2) has a RF blocking capacitor of ~ 0.4 pF placed at $1/4 \lambda$ away from the antenna center. This capacitor is formed by a Nb₂O₅ dielectric layer and the overlap area of a 17 μ m wide crossbar on top of the 20 μ m wide coplanar striplines.

The stack of 5 Si-wafers forming the micromachined horn section is glued with cyanobond



Figure 1: Geometry of the micromachined horn structure. Dimensions are given in units of wavelength at the designed frequency.

to the backplate of the mixermount. The backplate also holds a bias-tee, made of chip capacitors and coil inductors. The machined horn section is placed in front of the backplate, mounted in an xyz-stage which allows the alignment with the micromachined section. The electrical connection from the junction-chip to the bias circuit is made by pressing two stiff wires into two indium contacts on the chip.

The mixerblock and cold stage of the IF-amplification chain are mounted in an Infrared Laboratories HD3-8 dewar. The cold-plate of the dewar also holds a 1000-turn superconducting magnet for suppression of Josephson-currents. The signal and LO-power are combined by a 97% transmission beam splitter and enter the cryostat via a 25- μ m thick polypropylene vacuum window of 3 cm diameter. On the 77 K radiation shield a 750- μ m thick quartz plate covered with black polyethylene serves as a cooled low-pass filter. A F=28 mm TPX-lens is placed at focal length in front of the horn.

The IF-chain consists of the bias-tee circuit in the mixerblock, a Pamtech LTE 1268K isolator, and a Berkshire Technologies L-1.5-30HI IF-amplifier (40 dB). A further amplification of 60 dB is provided by room-temperature amplifiers outside the dewar. The IF-power is measured in

Table 1: Dimensions (in mm) of the quasi-integrated horn antenna. See Fig. 1 for definitions of lengths.

f (GHz)	Α	S	L	Μ	L _M	A _M
95	4.3	4.3	1.2	1.6	22.1	11



Figure 2: (a) Details of a micromachined mixer before bonding the wafers together. (b) Details of the device wafer, showing the dipole antenna and the DC-bias/IF-output connections

a 35 MHz bandwidth with an HP-436A power sensor at a center frequency of 1.5 GHz (set by a tunable bandpass filter).

3 Fabrication

Previous work in our group has shown that high-quality $Nb/Al_2O_3/Nb$ SIS junctions can be fabricated on thin SiN membranes [12]. The process steps currently used differ slightly from the one described in [12] and are outlined below. The different stages of the fabrication process are shown in Fig. 3.

3.1 Junction Fabrication

The fabrication starts with the chemical vapour deposition (at the Center for Integrated Systems at Stanford University) of 1- μ m thick low-stress SiN membranes on both sides of a 0.38 mm-thick and (100)-oriented silicon wafer. The 4-inch diameter silicon wafer is double-side polished and has a high resistivity > 2000 Ω cm. The high resistivity is currently required for room temperature testing of the IF-circuitry, but will in future be replaced by low resistivity Si since free carriers will be frozen out at LHe temperatures. The junction fabrication is performed at MIT Lincoln Laboratory using a selective niobium anodization process (SNAP). Several





trilayers for junction fabrication have also been supplied by Ron Miller at AT&T Bell Labs. The details of the fabrication process are similar to the process described by Bhushan and Macedo [13]. The junction fabrication starts with the deposition of a trilayer by dc-magnetron sputtering at a base pressure $< 5 \times 10^{-4}$ mTorr. The 200-nm Nb base electrode is deposited at a power of 1500 watts and an argon pressure of 10 mTorr. After the substrate is allowed to cool down, a 5-nm Al layer is deposited at a power of 150 watts and a pressure of 2 mTorr and this layer is subsequently oxidized at an oxygen pressure of 10 mTorr. Finally a 35-nm counter electrode is deposited at the same conditions as the base electrode.

The trilayers are patterned by plasma etching the Nb layers with CF_4 and a wet etch of the Al layer. Care should be taken that the pattern is properly aligned with the crystallographic

axes of the silicon wafer, since otherwise the aperture hole (which is aligned later with the trilayer pattern) will end up rotated with respect to the crystallographic aces and will have a rough surface. The junctions are defined by the standard anodization process and a 300-nm Nb counter electrode is deposited and patterned to connect the junctions. After the infrared-alignment (described below) the same pattern is used again for the E-beam evaporation of 400-nm thick Au bonding pads. Currently the mask contains 9 device definitions for the 85-105 GHz and 170-210 GHz frequency range. The junction sizes are designed to be $1.6 \times 1.6 \mu m^2$.

The patterned trilayer now serves as an alignment mark for an infrared alignment, in which the antenna apertures have to be defined on the *opposite* side of the wafer. To protect the trilayer during this patterning, the device wafer is placed face-down on a Si backing wafer and bonded to it with FSC-M. Although the backing wafer somewhat blurs the image in the infrared alignment, an accuracy of $\pm 5 \,\mu$ m can be achieved. After patterning, the silicon nitride is etched (with an approximate etch rate of 100 nm/min) in a mixture of freon-23 with 4 % oxygen at a power level of 100 W.

The chip is now mounted in a Teflon KOH etching mount shown in Fig. 4 which isolates the front and backside of the wafer by sandwiching the wafer between two O-rings [14, 15]. Extreme care should be taken to avoid any contact between the KOH and the frontside of the wafer, otherwise the Nb devices will be completely destroyed. The space on the device side of the wafer is slightly overpressurized with nitrogen gas, to prevent KOH leakeage through pinholes in the Si₃N₄ membranes. The freestanding membrane is formed by etching the silicon in a solution which contains 20% KOH by weight at 80 °C for 4-5 hours and another hour of etching at 60 °C. The last step is used to create smoother sidewalls of the aperture.

The final fabrication step is the deposition (with E-beam evaporation) of a 400-nm Ti/Au layer on the sidewalls of the aperture through a ceramic shadowmask. The shadowmask (which was patterned by cutting with an excimer laser) is used to avoid the deposition of gold on the membrane.

3.2 Horn Apertures

The micromachining of the horn apertures is similar to the etching process described above. In the patterning of these apertures a mask with circular hole definitions is used. Because of the highly anisotropic etching rate these holes will end up as squares holes with an area as large as the smallest rectangle that encloses the circular holes (Fig. 4). The advantage of this method is that the alignment to the crystallographic axes of the wafer is not important. After the etching, the SiN layers on the wafers are stripped in $160 \,{}^{0}C \,H_{3}PO_{4}$ and a 400-nm Ti/Au layer is deposited on the sidewalls.



Figure 4: (a) Mount used in the KOH etching of the apertures in the device wafer. (b) SEM picture of the circular aperture in the Si_3N_4 membrane and the pyramidal cavity formed by the anisotropic etch.

3.3 Mounting

The separate parts of the horn aperture are aligned under a microscope and bonded together with UV- and heat-curing Norland optical Glue and Krazy Glue Cyanobond. The accuracy of this alignment is within 20 μ m. The parts forming the horn section can be permanently bonded with the optical glue, but for repeated use of this horn section, the device wafer is glued with a cyanobond glue that dissolves easily in acetone.

4 Results

4.1 Cooling and mechanical ruggedness

A possible drawback in the use of thin freestanding membranes with superconducting devices could be that due to the high thermal resistance of the Si_3N_4 membrane, the cooling of the superconducting devices is not sufficient.

Measurements shown in Fig. 5 demonstrate that the superconducting junctions can be adequately cooled. In Fig. 5, three measurements of the same device are shown, where the device



Figure 5: DC I-V characteristics of device HEN52 measured immersed in liquid helium (solid line) and in the vacuum dewar at a mixermount temperature of 4.6 K and 2.74 K (dashed and dotted line).

was either immersed in liquid Helium (solid line), or mounted in the vacuum dewar with a mixer mount temperature of 4.6 K (dashed line) or 2.74 K (dotted line). The measurements show that the gap voltage of the two junction array decreases from 5.45 mV in the liquid Helium dewar (T=4.2 K) to 5.19 mV when the device is mounted in the vacuum dewar. This 0.13 mV decrease in gap voltage (per junction) corresponds to a temperature increase of 1 K. It will be shown next that this increase in temperature deteriorates the mixer performance somewhat, but even at the elevated temperature a good mixing performance is still achievable.

By pumping the He bath of the vacuum dewar the mixer mount temperature is reduced to 2.74 K. As can be seen in Fig. 5 this increases the gap voltage to a value similar to the measurement in the liquid helium dewar. Since the gap voltage of a superconducting tunnel junction is nearly independent of temperature for temperatures below half the critical temperature (9.2 K for Nb), this measurement shows that by pumping the He bath an optimum operating temperature can be reached.

The steep and even somewhat backbending current rise near the gap of the devices mounted in the vacuum dewar, which is not observed in the measurement in the liquid He dewar, indicates that the power dissipated by the DC tunnel current at the gap voltage increases the junction temperature (thereby decreasing the gap voltage). Although this bias current dependent temperature is inconvenient for a comparison of measured data with mixer theory, we do not expect that it influences the mixer performance in a very strong way, since for mixer operation the bias current of a device will be approximately one third of the total current increase at the gap voltage ($\approx 50 \ \mu$ A for this junction) and the temperature increase will be only marginal.

The observed temperature increase of the devices when mounted in the vacuum dewar is



Figure 6: Pumped and unpumped I-V charactersistics of device HEN52 at a LO frequency of 102 GHz and the measured IF-output power with a 295 and 77 K input load.

expected to be less for higher frequency designs, since the membrane size decreases with the wavelength.

Glueing the device wafer with the Si_3N_4 membrane to the wafers that form the apex of the horn cavity forms a sealed air-filled cavity and the pressure difference between this closed cavity and the dewar vacuum will cause bending of the membrane. Several devices have been mounted and used in the vacuum dewar and all the membranes withstand the pressure differences. Also, the thermal cycling between room temperature and 4.2 K does not degradade the device characteristics.

4.2 Noise measurements

The results for a heterodyne measurement on an array of two junctions, which gave the best noise temperature measured thus far, is shown in Fig. 6. The array has a normal state resistance of $R_N = 37 \Omega$ and each junction has an area of 2.6 μm^2 (the critical current density is $J_c = 4.9 \text{ kA/cm}^2$). Fig. 6 shows the DC I-V curve measured with and without the 102 GHz local oscillator radiation applied (at a mixer mount temperature of 2.74 K) and the IF-output power with a 77 K and 295 K blackbody input signal.

The maximum Y-factor (measured at the first photonstep below the gap voltage) is 3.94 dB, which results in a 70 K DSB receiver noise temperature (without any correction). For a mixer mount temperature of 4.7 K the DSB noise temperature is 80 K, showing that although there is a clear decrease in gap voltage (see Fig. 5) the noise temperature increases only 10 K. The measured noise temperature as a function of frequency is shown in Fig. 7. The 3 dB bandwidth



Figure 7: Noise temperature as a function of frequency. The 3 dB bandwidth is 15 GHz.

of the mixer is ≈ 15 GHz.

Our first results are within a factor of 3.5 and 2 in comparison with the best waveguide and quasi-optical SIS mixers for this frequency range, respectively. As will be shown next the present level of the noise temperature is mainly caused by the large reflection of signal power due to the capacitance of the tunnel junction. The waveguide and quasi-optical mixers have overcome this problem by use of (external or integrated) tuning elements, or by use of sub-micron area tunnel junctions.

For a possible further optimization of the micromachined receiver, the various noise and gain contributions of the receiver are analyzed. The total measured receiver noise temperature, expressed in terms of noise and gain of the rf, Mixer and IF components, is given by:

$$T_{\rm REC} = T_{\rm RF} + \frac{T_{\rm MIX}}{G_{\rm RF}} + \frac{T_{\rm IF}}{G_{\rm RF}G_{\rm MIX}} \tag{1}$$

The noise contribution $T_{\rm IF}$ and the gain of the IF-chain are found by using the shot noise of the unpumped I-V curve as a calibrated noise input for the IF-chain. The values thus found are $T_{\rm IF} = 3.6$ K and $G_{IF} = 100.3$ dB. Once the IF gain is known, the product $G_{\rm RF}G_{\rm MIX}G_{\rm IF}$ is found from the difference in output power δP_{out} caused by the 295 K and 77 K input signals, since $\delta P_{out} = \delta P_{in}G_{\rm RF}G_{\rm MIX}G_{\rm IF}$ (where $\delta P_{in} = kB(295 - 77)$, k = Boltzmann's constant, B=IFfilter bandwidth). At the biasvoltage with the optimum noise performance, $G_{\rm RF}G_{\rm MIX} = -5.1$ dB, which results in a noise contribution of 11.6 K from the $T_{IF}/G_{\rm RF}G_{\rm MIX}$ term in Eq. 1. The noise contribution of the RF input is caused by the loss of the beamsplitter (97 % transmission), the dewar window (97 % transmission) and the quartz heat filter (≈ 100 % transmission at 100 GHz) and amounts up to 16 K. Losses in the lens and the machined and micromachined horn sections do not contribute to the RF noise temperature, since those losses are at 4.2 K.

The unknown parameters in Eq. 1 are the separate mixer and RF loss G_{RF} , G_{MIX} and the mixer noise temperature T_{MIX} . We estimate the resistive loss of the micromachined horn section to be 1-2 dB, based on the scale model measurements described in [16]. Main cause of this loss is the partly uncovered sidewall of two wafers of the pyramidal horn section. A part of the sidewall is not covered with gold, to avoid shorting of the coplanar IF-output/DC-bias lines. With a total RF input loss of 1.3-2.3 dB, the mixer gain is -3.8- -2.8 dB and the mixer noise temperature is 28 ± 12 K.

The mixer gain and noise are also calculated with the quantum mixer theory. For an accurate calculation a precise knowledge of the embedding admittances at the LO, USB (upper side band) and LSB (lower side band) is necessary and from an analysis of the pumped I-V curve these embedding impedances can be found. As was already pointed out, the current dependent temperature near the gap voltage makes it difficult to obtain a very accurate value for the embedding admittances. Furthermore we observed that the shape of the pumped I-V curves does not changes very much if the frequency is changed. Very flat or even negative slopes on the first photonstep below the gap were not observed, indicating that the embedding admittance is mainly determined by the junction capacitance and also that the embedding will change slowly as a function of frequency. Analysis of the pumped curve shown in Fig. 6 yielded a calculated LO embedding admittance of $Y_{emb} = 0.75 + j2.5$ (scaled to the normal state admittance $Y_N = (37 \ \Omega)^{-1}$). This capacitive embedding results in a -5 dB coupling coefficient to the 35 Ω antenna impedance. If we ignore the influence of any reactive antenna admittance, the embedding admittance from the parallel connection of the antenna admittance, the parasitic capacitance due to the overlap of the electrodes (\sim 30 fF) and the junction capacitance (55 $fF/\mu m^2$, with a junction area of 2.6 μm^2) we find a scaled embedding admittance of 1 + 2j at 100 GHz, in reasonable agreement with the value found from the analysis of the pumped curve.

The mixer noise and gain are calculated with the value for Y_{emb} found from the analysis of the pumped curve. Assuming the same embedding admittance at the LO, USB and LSB frequencies the calculated mixer gain and noise are $G_{MIX} = +1.5$ dB and $T_{MIX} = 16$ K. The calculations therefore overestimate the gain and underestimate the mixer noise, which we attribute to the error margins in the determination of the embedding impedancies.

4.3 FTS measurements

The frequency response of the micromachined horn antenna is measured with a Fourier Transform Spectrometer. In these measurements the SIS junction array is biased at a voltage just below the gap voltage and used as a video detector, with a frequency dependent responsivity $R = \Delta I / \Delta P \approx e/\hbar \omega$.



Figure 8: Frequency dependent coupling measured with a Fourier Transform spectrometer (solid line) and the calculated coupling (dotted line).

Fig. 8 shows the result of the frequency dependent coupling measured with the FTS, together with a calculated coupling, to be discussed later. The maximum coupling is measured just above 100 GHz, in agreement with the noise temperature measurement.

The dotted line shown in Fig. 8 shows a calculated frequency dependent coupling (scaled to the maximum measured coupling) of which the general behaviour is in good agreement with the measured frequency response. In the calculations we used the dipole antenna impedance measured in a scale model and added in parallel the capacitance from the two junction SIS array. The original impedances and the impedance after adding the junction capacitance are shown in Fig. 9, together with the embedding impedance found from the analysis of the pumped curve. The displayed curve of the calculated coupling in Fig. 8 is shifted +5 GHz in frequency to make the measured and calculated peak couplings coincide. Since the scale model differs somewhat from our actual design, slight differences between the measured and calculated coupling are to be expected. The maximum coupling calculated from this model is =-4.9 dB, which is nearly the same as the coupling calculated with the calculated embedding impedance although the actual admittances differ significantely.

5 Conclusion

In summary we have shown for the first time the operation of a micromachined SIS mixer for the 75-115 GHz range. The feasibility of micromachined SIS-mixers is demonstrated: the complete micromachined mixer is robust and can be thermally cycled in a cryogenic vacuum environment, the tunnel junctions can be sufficiently cooled, and noise measurements are performed. The measured minimum noise temperature of 70 K DSB is very encouraging and is expected to





Figure 9: Smith chart showing the impedance at the dipole antenna terminals measured from a scale model, and the impedance after adding a parallel capacitance of the tunnel junction array. Also shown is the embedding impedance calculated from the pumped I-V curve.

be further improved by future designs in which the junction capacitance is tuned out by an integrated tuning element.

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