Submicron Schottky-Collector AlAs/InGaAs Resonant Tunnel Diodes

S.C. Martin, R.E. Muller, K. Nummila*, and R.P. Smith
Center for Space Microelectronics Technology
Jet Propulsion Laboratory/California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109

M. Reddy, M.J. Mondry, and M.J.W. Rodwell,
Department of Electrical and Computer Engineering,
University of California, Santa Barbara, CA 93106.

D.H. Chow and J.N. Schulman
Hughes Research Laboratories
Malibu, CA 90265.

Introduction

Resonant tunnel diodes (RTDs) are currently the widest bandwidth semiconductor devices useful for high frequency oscillators and picosecond pulse generators [1], [2]. 712 GHz oscillators [2] and 1.7 ps pulse generators [3], fabricated with 1.0 THz bandwidth InAs/AlSb RTDs, are some examples of high speed RTD applications. Here, we report the fabrication and the dc and microwave characteristics of AlAs/$In_{0.53}Ga_{0.47}As$ Schottky-collector resonant tunnel diodes (SRTDs) with deep submicron Schottky collectors and an estimated intrinsic maximum frequency of oscillation f_{max} of 2.2 THz . The process is planar, so monolithic integration of single devices with matching circuitry for waveguide-based LO's or of many SRTDs into quasi-optical oscillator arrays is possible.

Schottky-Collector RTDs

RTD bandwidths are currently limited by parasitic resistance from the ohmic contacts. In Schottky-collector RTDs, the ohmic-contacted collector of a conventional RTD is replaced with a direct Schottky contact to the space-charge layer (Fig. 1), eliminating the top contact series resistance[4]. The remaining series resistance components are minimized by scaling the Schottky-collector to deep submicron dimensions. This reduced series resistance leads to an increased maximum frequency of oscillation, $f$max . 0.1 μm AlAs/GaAs SRTD's have been previously reported with an estimated f_{max} =900 GHz [5].
AlAs/$In_{0.53}Ga_{0.47}As$ SRTDs should yield further increases in f_{max} owing to the superior material properties of this system [6].

RTD electrical characteristics when biased in the negative-differential-resistance (NDR) region [1] are represented by the parasitic series resistance, R_s, the space charge layer capacitance, C, the negative resistance, R_n, and a quantum well inductance, L_{qw} (see inset of Fig. 2). $L_{qw} = -\tau_{qw}R_n$ (negative in the NDR region), where τ_{qw} is the electron lifetime in the quantum well. f_{max} is the frequency at which the network's admittance, Y(ω) has a zero real component. Inclusive of the quantum well lifetime τ_{qw} and assuming that

$$\tau_{qw} >> C(R_nR_s)^{-1/2},$$

the expression for calculating f_{max} is

$$f_{max} = 1/(2\pi)(\tau_{qw})^{-1/2}(R_nC)^{-1/4}(R_sC)^{-1/4} \quad (1).$$

* Current address: Nokia Research Center, PO Box 45, FIN-00211 Helsinki, Finland

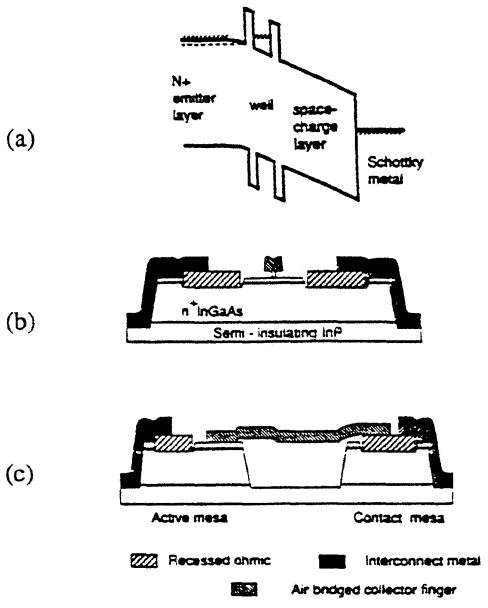

Fig. 1: (a) Band diagram, (b) and (c) perpendicular cross sections of a submicron AlAs/$In_{0.53}Ga_{0.47}As$ SRTD.

Improvements in f_{max} are obtained by decreasing R_sC, R_nC and τ_{qw}. Thin barriers result in both small τ_{qw} and a high current density which reduces R_nC . Reduction in τ_{qw} and R_nC through the use of very thin barriers is ultimately limited by degradation in the current peak-to-valley ratio (PVR) and by high device power dissipation. R_s can be reduced by employing a Schottky collector of submicron width; the resulting increase in f_{max} is shown in Fig. 2. Compared to 0.1 μm AlAs/GaAs SRTDs

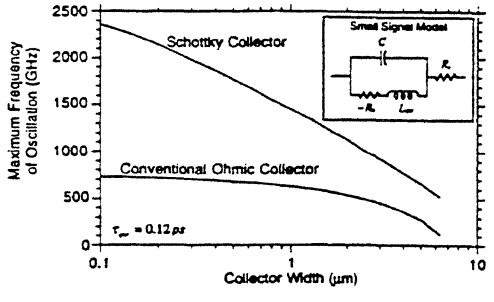

Fig. 2: Comparison of a conventional RTD to a Schottky-Collector RTD using measured values of R_n and C from the 5 ML AlAs/$In_{0.53}Ga_{0.47}As$ SRTD, inclusive of the effects of τ_{qw}. The inset shows the small signal equivalent circuit model of an RTD biased in the negative differential resistance region.

[4], AlAs/$In_{0.53}Ga_{0.47}As$ SRTDs have slightly smaller τ_{qw} and substantially smaller R_s and R_nC and therefore should attain higher f_{max}.

Fabrication

Molecular beam epitaxial growth of the RTD layer structure started with a 1.0 μm, $10^{19}/cm^3$, Si doped, $In_{0.53}Ga_{0.47}As$ buried N+ contact layer on the [100] InP substrate at a temperature of 540° C. This was followed by a 50nm, $10^{18}/cm^3$, Si doped, $In_{0.53}Ga_{0.47}As$ emitter and a 10nm, undoped, $In_{0.53}Ga_{0.47}As$ spacer layer. The last 10 nm of the emitter and the entire spacer layer were grown at a substrate temperature of 320° C to minimize out diffusion of Si dopants into the double barrier structure. 1.4 nm or 1.7 nm (5 or 6 monolayers), undoped AlAs form the barriers on either side of a 4.7 nm, undoped, $In_{0.53}Ga_{0.47}As$ quantum well. Growth interruptions were used before and after the low temperature growth to stabilize the substrate temperature. The rest of the structure, grown at 510° C, consisted of a 25 nm, undoped, $In_{0.53}Ga_{0.47}As$ space-charge layer and 10 nm, $5x10^{18}/cm^3$, Be-doped, $In_{0.53}Ga_{0.47}As$ p-type cap layer.

Due to the approximately 0.1 eV - 0.3 eV potential barrier at the air-semiconductor interface there is significant free charge in the space charge region of the uncontacted regions surrounding the Schottky collector. Parasitic surface leakage currents will arise if this sheet charge is significant. Assuming a 0.2 eV potential barrier at the air-semiconductor interface, the calculated electron free charge density is $10^{11}/cm^2$ without the p-type cap and is reduced to $10^9/cm^2$ with the cap. The cap layer, an extension of the space charge region, is fully depleted. Within the SRTD, the fully depleted cap increases the forward voltage by an estimated 0.4 V. This increased forward voltage can be eliminated by a self-aligned recess etch through the p-type cap before deposition of the Schottky metal. Experiments with a recess etch were abandoned due to difficulties in controlling the etch uniformity in very small area devices - while working devices were fabricated, the uniformity required for the parameter extraction described in the following section could not be accomplished. The total space charge layer thickness is 35 nm which minimizes space-charge transit time.

Acknowledgements
The work at U.C.S.B. was supported by ONR under contract # N00014-93-1-0378, NSF/PYI, and a JPL President's Fund. The work at JPL was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration, Office of Advanced Concepts and Technology, and by the Innovative Science and Technology Office of BMDO through an agreement with NASA.

References

1. E.R. Brown, J.R. Soderstrom, C.D. Parker, L.J. Mahoney, K.M. Molvar, and T.C. McGill, Appl. Phys. Lett., 58, 2291 (1991).

2. E.R. Brown, T.C.L.G. Sollner, C.D. Parker, W.D. Goodhue, and C.L. Chen, Appl. Phys. Lett., 55, 1777 (1989).

3. E. Ozbay, D.M. Bloom, D.H.Chow. and J.N. Schulman, IEEE Electron Dev. Lett. 14, 400 (1993).

4. Y. Konishi, S.T. Allen, M. Reddy, M.J.W. Rodwell, R.P. Smith and J. Liu, Solid-State Electronics, 36, 1673 (1993).

5. R.P. Smith, S.T. Allen, M. Reddy, S.C. Martin, J. Liu, R.E. Muller, and M.J.W. Rodwell, IEEE Electron Dev. Lett., 15, 295 (1994).

6. D.H. Chow, J.N. Schulman, E. Ozbay, and D.M. Bloom, Appl. Phys. Lett., 6, 1685 (1992).

7. R.E. Muller, S.C. Martin, R.P. Smith, S.T. Allen, M. Reddy and M.J.W. Rodwell, The 38th International Symposium on Electron, Ion and Photon Beams, New Orleans, Lousiana, June 1994; J. Vac. Sci. Technol. B (to be published).