Novel Planar Varactor Diodes

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Abstract

This paper reports on our development of novel planar varactor diodes. This includes devices integrating four Schottky diodes for use in balanced doubler blocks. Improvements in epilayer designs and reducing parasitics have greatly improved the RF results, yielding record efficiencies and output powers at 160 GHz, and record output powers at 320 GHz.

Introduction

Schottky barrier varactor diodes are used as frequency multiplier elements for local oscillator sources in millimeter and submillimeter wavelength receivers. Increasing interest in space-based applications has motivated the development of new solid state LO systems using planar diode technology. These systems are more rugged and more easily space qualifiable than their whisker-contacted counterparts. In addition, planar diode technology enables the integration of several diodes into a single device. We report on improvements in output power and efficiency of millimeter wave frequency multipliers, doubling to 160 and 320 GHz.

Previous Results

The 160 GHz and 320 GHz doubler blocks (Fig. 1) described here were originally designed to use SC10V2 and SC3T2 diodes, respectively. These diodes were fabricated by B. Rizzi, and the parameters of these devices are listed in Table 1. The devices consist of four Schottky diodes integrated in two series pairs, one pair on either side of the center pad (see Fig.

2). This balanced doubling configuration allows the input power at the fundamental to be applied across all four diodes, and the center pad is soldered to the center conductor of a coaxial line through which the output power at the first harmonic is extracted. Their best RF results, described in [1], were 25% peak efficiency and 55mW peak output at 160 GHz output frequency, and 13% efficiency, 4mW output at 270 GHz.

Improved 160 GHz balanced doubler

It was found that the voltage breakdown of the SC10V2 (160 GHz) devices was high enough to allow these devices to be safely pumped with 250 mW of input power, however this is far more power than is available from the intended source, a Gunn oscillator at 80 GHz. In order to improve the efficiency, a new version of the device was designed, the SC6T6 (Fig. 2), whose parameters are listed in Table 1. The N^- epilayer was designed to be thinner with higher doping, while the diameter of the anodes was scaled to keep the zero-bias junction capacitance the same as the previous (SC10V2) batch. Thinner epilayers with higher doping should tend to reduce transit-time or velocity saturation effects and, as expected, were found to greatly reduce the series resistance, from 6 down to 1.5 - 2 ohms.

The fabrication of the SC6T6 devices was similar to previous devices described elsewhere [2], except that the ohmic contacts were formed by Ni/Ge/Au evaporation rather than electroplating. It was found that this technique yielded lower ohmic contact resistivity and reduced the parasitic series resistance associated with the small-area ohmic pads (when measured at DC).

Improved 320 GHz balanced doubler

New devices were similarly designed for use in the 320 GHz doubler block. This new batch, SB3T1 (Fig. 3), was also designed with thinner, higher doped epilayers than the previous devices (SC3T4). The parameters for both of these devices are listed in Table 1. An early version of this device was fabricated using the standard planar varactor process and were tested at 270 GHz, but their RF performance was disappointing, yielding less than 3mW at any frequency.

It was believed that this disappointing performance was due to several factors, including

excessive parasitic shunt capacitance, poor capacitance modulation ratio, excess thickness of the substrates, and the presence of damaged GaAs on the back sides of the chips as a result of the mechanical lapping procedure. Fig. 4 shows the C-V characteristics of this early batch, and it is clear that due to the high parasitic capacitance, the capacitance modulation ratio is poor. In order to reduce the parasitic capacitance, particularly close to the anode, a new fabrication process was developed for forming the interconnect metal contacting the anode. As seen in figure 5, in the old batch, the metal of the contact finger lies directly on oxide which is over N-type epitaxial material, thus forming a shunt capacitor right beside the anode, effectively reducing its capacitance modulation ratio. Figure 6 shows the results of the new fabrication process to reduce this capacitance. On these devices (SB3T1), the interconnect metal no longer lies on oxide, but uses an air bridge technique to maintain a 1μm air gap between the metal and the semiconductor, and the only metal which touches the surface is the area of the Schottky contact itself. This effectively replaces a 0.5μm layer of oxide of dielectric constant 6 with a 1μm layer of dielectric constant 1, yielding roughly a factor of 12 reduction in the overlay capacitance.

The air bridge interconnect was formed by first applying a 1μm photoresist layer, in which vias for the anode and the pad areas are patterned. Then a short baking procedure was used to induce a slight slope to the vertical walls of the resist layer, and a second photoresist layer was applied on top of the first. This layer was patterned to form the shape of the pads and interconnect fingers by lift-off. Very thick metallization was then deposited by evaporation of the following metals: Ti (200nm), Al (1.2μm), Ti (200nm), Au (300nm), and the unwanted material was removed by lift-off of the second photoresist layer. After the isolation etching, the device was lapped to about 40 μm thickness, and then a wet chemical etch was used on the backs of the chips to thin them to under 25 μm. In this way, any damaged GaAs material left from the mechanical lapping process was removed.

The SB3T1 batch had one other significant difference from previous devices, in that it had no ohmic contacts. The large areas which typically are ohmic contacts were replaced with titanium Schottky contacts deposited directly on the N^+ buffer. Because of the extremely high doping of the GaAs beneath the contacts, they had a reverse breakdown voltage of ~0.2V. Also, due to the large area of these contacts relative to the anode area, they had a capacitance on the order of several pF, corresponding to an impedance of less than 1(-j) ohm at 160 GHz. It is believed that while the DC bias currents must pass through these contacts as a tunneling/

avalanche - generated particle current, RF currents (at $\geq$ 160 GHz) are shunted through this large capacitance as a displacement current, so that the I-V characteristics of this large-area contact do not contribute to the overall I-V or C-V characteristics of the device at RF.

RF testing

The varactor arrays were designed for use in two balanced doubler circuits as described previously. One circuit was designed for a center frequency of 170 GHz [3], while the other was designed for 300 GHz [4]. The diodes reported in this work provide greatly improved performance over that achieved previously. The lower frequency doubler was tested with Gunn oscillators providing a power of 130-145 mW from 79 to 85 GHz, with most of the effort concentrated at 79.5 GHz input. The higher frequency doubler was tested with a Gunn oscillator producing 40-50 mW in the 130-145 GHz range and also with the low frequency doubler as a source at 158 GHz. All power measurements were verified with a waveguide calorimeter designed for this work [5]. This calorimeter was calibrated by directly heating the internal load with D.C. power applied to a resistor and readings were then corrected for input losses. This calibration was verified by checking it against a second calorimeter of different design [6], and the agreement was found to be excellent, typically within 2%. The WR10 input waveguide to the calorimeter was converted to the required bands with standard tapers.
The doublers generally were not well matched to the diodes and required input and output tuners for best results. These tuners are small pieces of teflon filling the waveguides with electrical lengths of $\lambda/4$ which are pushed along the waveguide until a maxima in power is found. In some cases use of these tuners resulted in a doubling of the output power over the untuned case. In all cases the final power and efficiency achieved may be considered essentially free from the effects of impedance mismatch, except that the tuners themselves may cause somewhat higher loss than would be experienced in an optimized circuit. Input and output losses of the doublers are very small because of the circuit simplicity, so that the results closely approximate the efficiency of the diode itself.

159 GHz Results

Several diodes from the batch SC6T6 were tested with 79.5 GHz input and all gave

comparable results. The best diode produced 58 mW output with an input power of 145 mW, with an efficiency of 40%. This is the highest efficiency and power achieved in any doubler at a comparable frequency. Other diodes produced at least 50 mW, and some of the variation may be due to the tuning. Measurements were made of the output power vs. input power to check for the effects of saturation, and results are shown in Fig. 7. These tests were made in a doubler with tuning optimized at maximum input power, and then fixed. Only the D.C. bias was varied in these power tests. Up to nearly the highest input power available, the efficiency continues to increase, with perhaps a flattening at the last data point. While the method of optimization tends to favor the higher powers, adjusting the D.C. bias ensures that the impedance match degrades fairly slowly at lower power. Optimum bias at maximum power is 10-11 V, with <0.1 mA of current flow, consistent with the observed efficient varactor operation. This bias is about as high as is safe for the operation of diodes with 22 V breakdown, and the optimum bias increases with increasing input power, so the present operation is at near maximum power. Reliability was tested to verify safe operation by running the best doubler for 100 hrs. at full power. No significant deterioration in output power was observed over this period.

318 GHz results

Diodes for the higher frequency doubler showed the best impedance match at 159 GHz input, so tests were concentrated at this frequency. These tests required the first doubler to drive the second without any isolation, so tuning the second stage was difficult, particularly for input match. It proved easiest to include a phase shifter between the two doublers, and to set the phase for optimum power output, so that any residual mismatch between the two doublers was partially canceled. Slightly higher power could be attained without the phase shifter only with difficulty. In any case the tests required a connecting waveguide with a loss of 0.3 dB. The doubler used as a source in these tests produced a maximum power of 48 mW (45 mW after the connecting guide).

The highest power output at 318 GHz was 6.0 mW, for an efficiency of 13%. This is the highest efficiency achieved with planar diodes at this frequency. The efficiency is lower than that for whiskered diodes [7], but the power output is higher, because the planar array can survive much higher input power. The operation was consistent with the varactor mode with a

bias of 6.5 V and 0.2 mA. Several diodes from the same batch were tested in the same mount, and all others gave significantly poorer output, 4.5 mW or less. The efficiency vs. power behavior is of interest but is much more difficult to determine without input isolation. To simplify the measurement, we assumed that the interaction between the two doublers was relatively insensitive to power level, and simply attenuated the input power to the first stage doubler, producing a known first stage output power from a curve such as Fig. 7. These tests showed that the efficiency of the second stage was slowly rising (1.1 dB{out}/dB{in}) at 48 mW input.

CV Measurements

Diodes from the SB3T1 batch were tested for capacitance vs. voltage using a HP8510 network analyzer, over a frequency range of 2-18 GHz. Contact to the diodes was made with wafer probes (Picoprobes [7]), in the form of a transmission measurement through the diode junction (magS21). The diode chip formed the center conductor of a short CPW line, with ground planes made of small gold ribbons. Measurements of parasitic pad to pad capacitance were made on diodes with broken air bridges. The advantage of high frequency measurements is that they are somewhat more accurate than the usual 1 MHz measurements, and that they remain accurate in the presence of leakage currents, such as are experienced near reverse breakdown. It is also possible to measure at very low signal levels. These measurements used a test signal voltage of 10mV. Results of these tests on a diode of the same size that gave the best doubler results (as well as a larger diode from the same wafer) are shown in Fig. 8. This data shows a peculiar effect in that the capacitance drops about 0.5 fF at the onset of reverse breakdown. This was seen on all diodes measured, and can not be an artifact due to leakage conduction, because it would cause the opposite effect, and would have a different frequency dependence. These measurements are otherwise similar to the expected abrupt junction behavior if we assume a close-in parasitic capacitance of 2 fF.

Conclusions

New devices for millimeter wave frequency multipliers were developed and RF tested, including a device for doubling to 160 GHz and a scaled version of this device for doubling to

320 GHz. By using higher doped, thinner epilayers, the performance of the 160 GHz balanced doubler was greatly improved, from 25% efficiency to 40% efficiency and 58 mW output power. This is the highest efficiency and power achieved in any doubler at a comparable frequency.

A new fabrication procedure was developed for the 320 GHz balanced doubler which greatly reduced the parasitic shunt capacitance of the interconnect metal near the anode. These and other improvements yielded improved performance, 13% efficiency and 6mW output at 320 GHz. This is the highest efficiency achieved with planar diodes at this frequency.

Acknowledgments

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[6] N.R. Erickson, "High Efficiency Submillimeter Frequency Multipliers," 1990 IEEE MTT-S Int'l Microwave Symposium, pg. 1301.

[7] Picoprobes, GGB Industries, Naples, Fla.

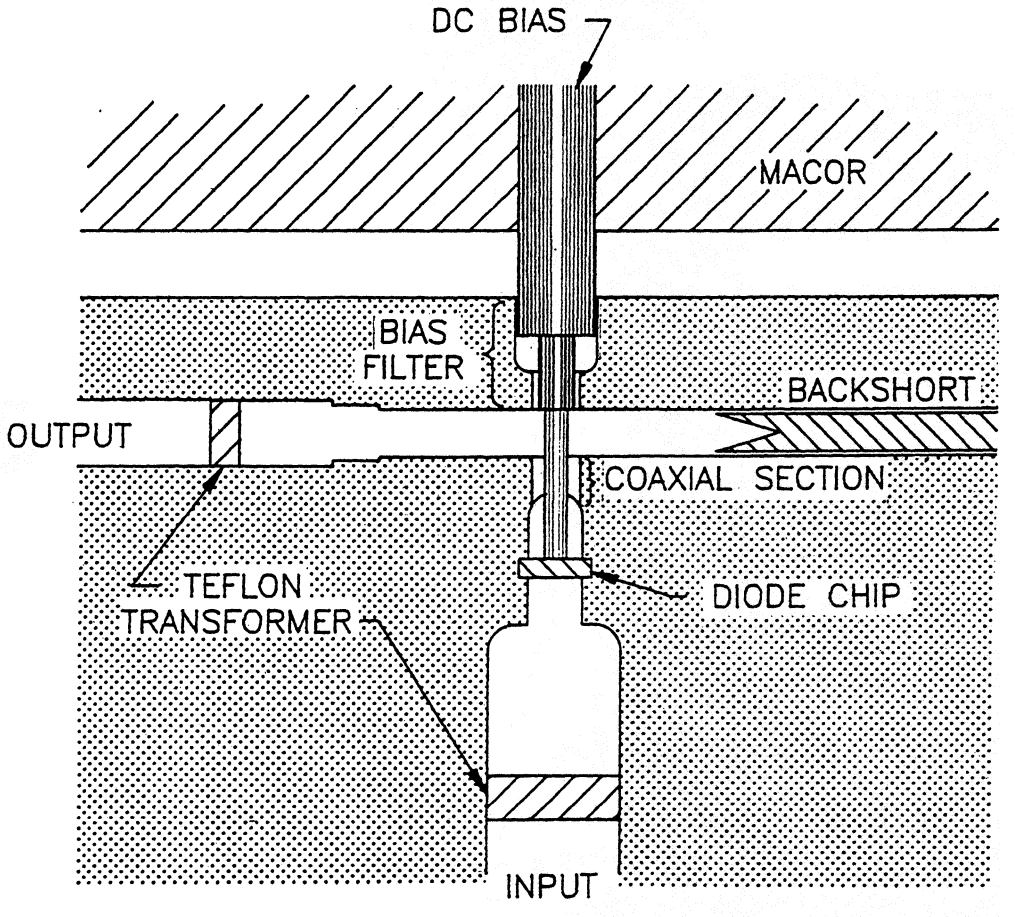

Figure 1: Diagram of the balanced doubler block

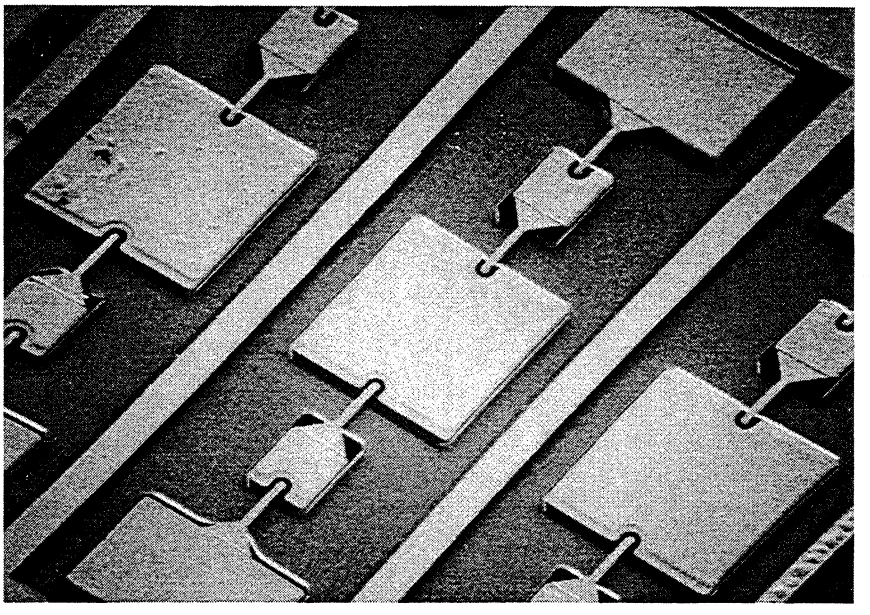

Figure 2: SEM photograph of SC6T6 devices

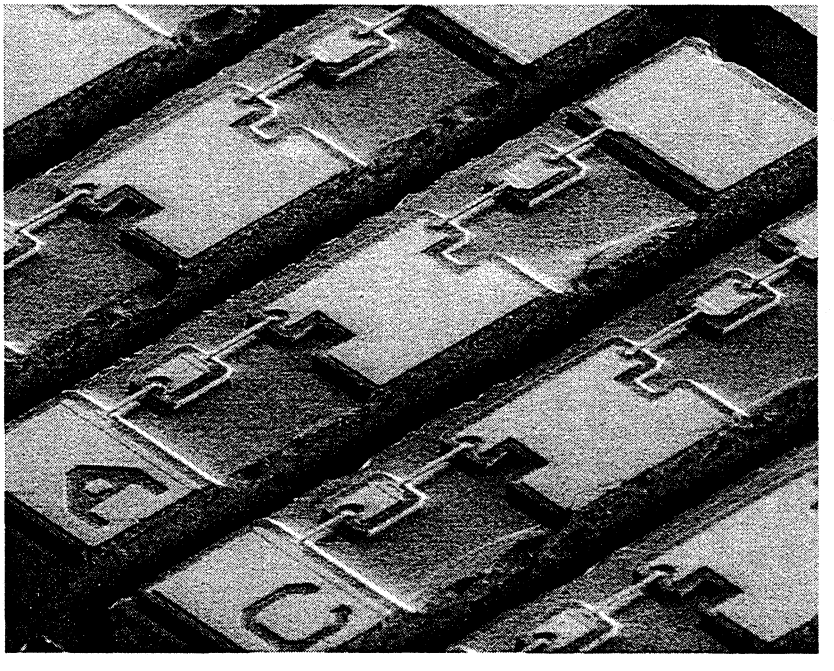

Figure 3: SEM photograph of SB3T1 devices

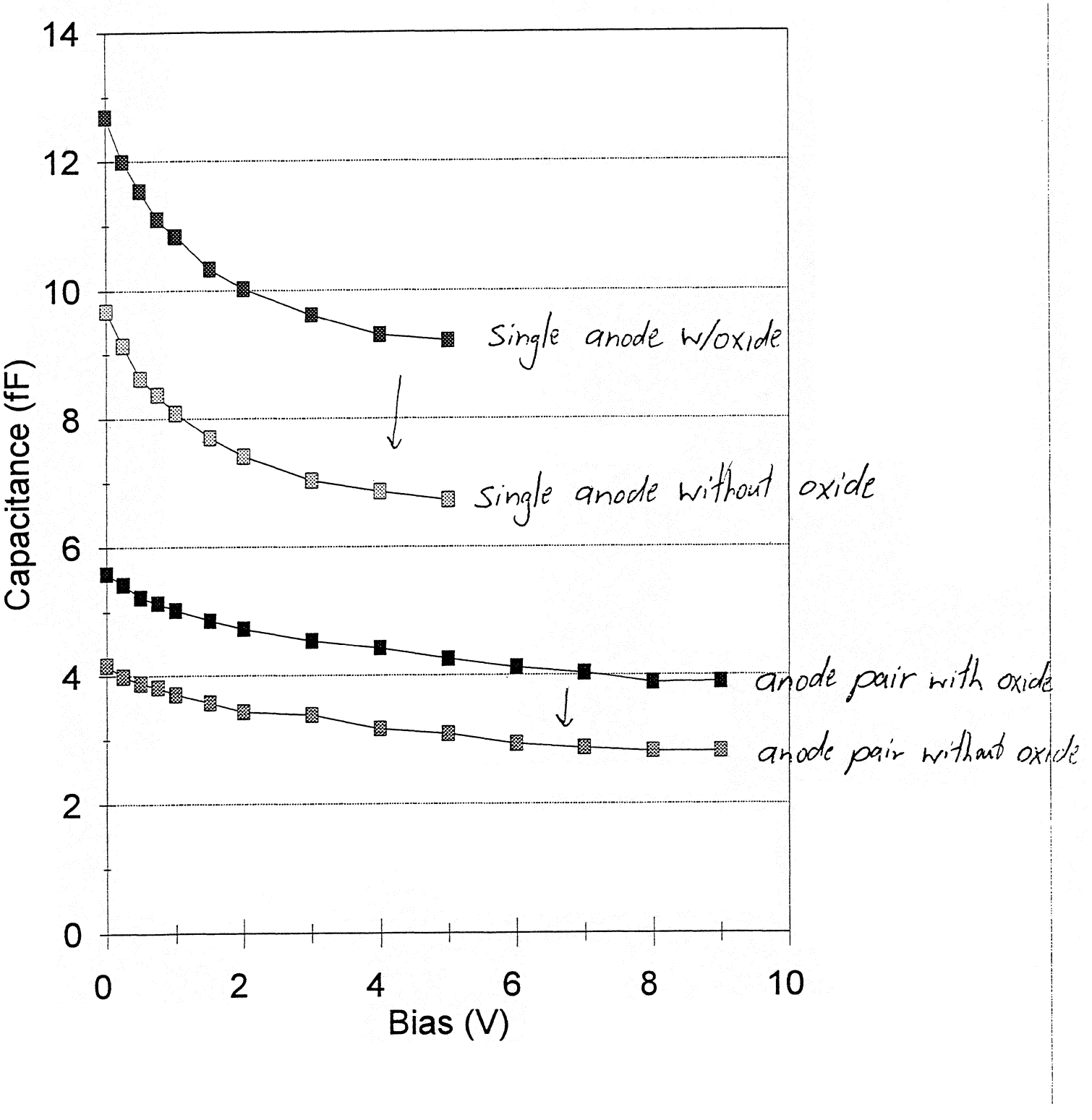

Figure 4 : CV characteristics of earlier, poor-performing batch. Note that there is little capacitance variation, although the modulation ratio was improved slightly by wet etching the oxide from the chips.

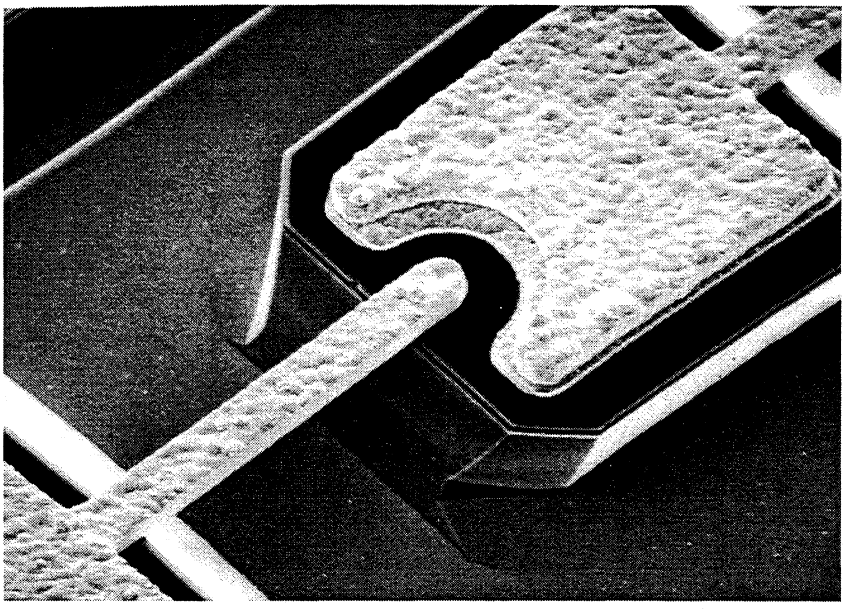

Figure 5: SEM photograph of older, poor-performing chip. Note large overlay area under finger metallization.

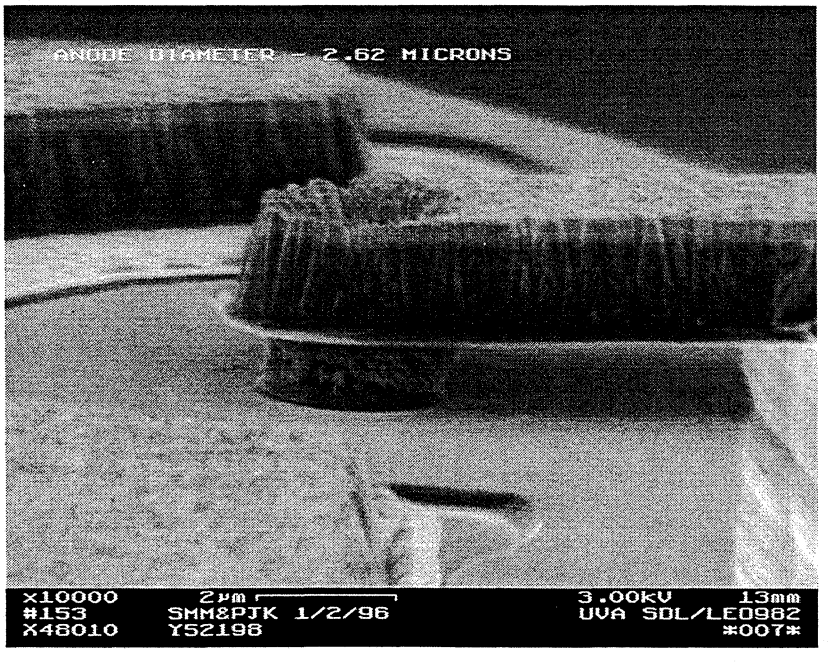

Figure 6: SEM photograph of new, air bridge interconnect metal. The only metal in contact with the semiconductor is the area of the anode itself.

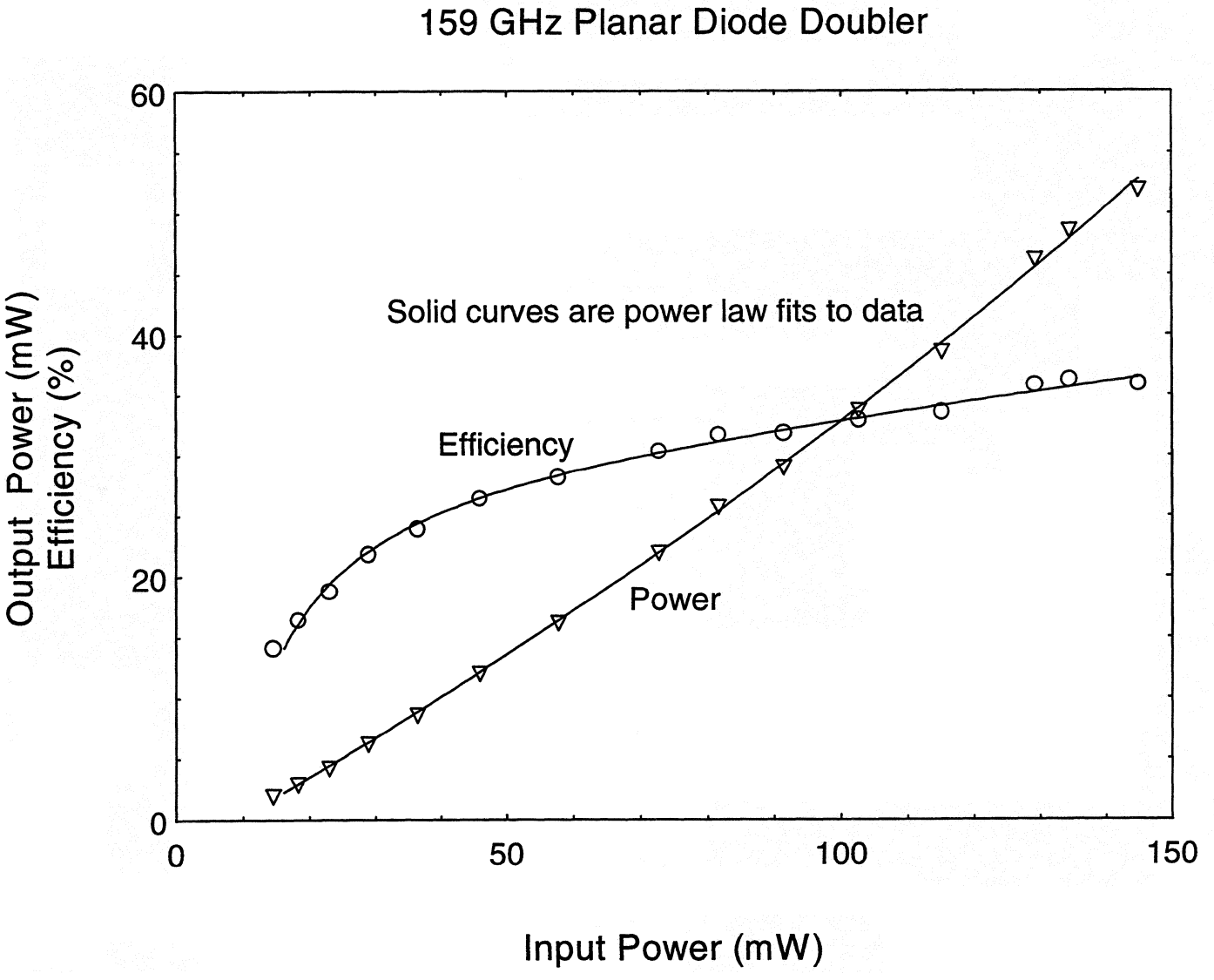

Figure 7 : Output power and efficiency vs. input power of SC6T6 diodes at 159 GHz.

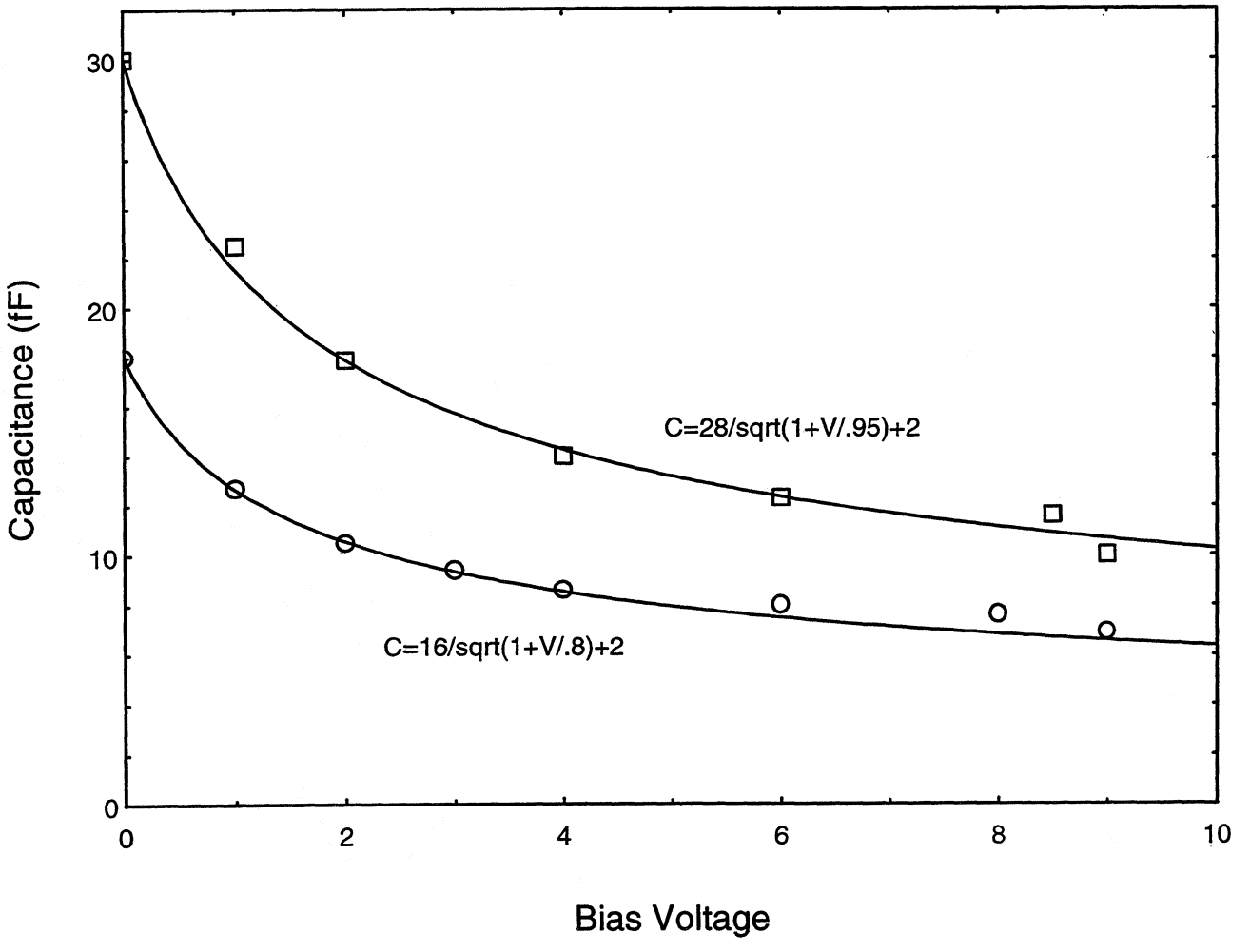

Figure 8 : CV measurements of two different anode sizes from the SB3T1 batch. The lower capacitance curve is a device with the same anode size as those which gave the best RF results.

Table 1: Device Parameters

Table 1

					Single Anode		
Batch#	t_{chip} (μm)	t_{epi} (Å)	N_{epi} (cm^{-3})	diam.(μm)	C_{jo} (fF)	R_s (Ω)	V_{br} (V)
SC10V2	25	6400	4.5×10^{16}	9	38	6	15
SC6T6	20	4500	1.2×10^{17}	6	40	1.5	11
SC3T4	25	4000	1.0×10^{17}	3.5	15	6	9
SB3T1	20	2500	2.5×10^{17}	2.6	18	??	8
SC3T7	40	4500	1.4×10^{17}	4	18	??	11