# ADVANCES IN SUBMILLIMETER WAVE SEMICONDUCTOR-BASED DEVICE DESIGNS AND PROCESSES AT JPL

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Abstract

Planar submillimeter wave circuits are slowly replacing whisker-contacted devices at frequencies above 100 GHz, but in many cases the size constraints dictated by the short wavelengths found at high frequencies have not been adequately addressed. In the last year we have been responding to the challenges of implementing submillimeter wave circuits in GaAs by using processing technologies somewhat new to this field as well as developing unique processing capabilities. This approach has allowed for greater flexibility in circuit design and the ability to fabricate circuits for frequencies up to 2.5 THz. Changes in our device processing include: (1) using either direct-write electron-beam or 5x projection lithography for all pattern definition, (2) doing mesa etching by RIE (reactive ion etching), and (3) incorporating an advanced planarization/air-bridge fabrication technique for submicron structures. Together, these process changes have enabled us to control process dimensions to sub-micron, or even deep sub-micron, levels. The circuits fabricated using these techniques include a number of waveguide and quasi-optical multipliers to be used at frequencies from 160 GHz to 640 GHz, and a quasi-optical mixer for 2.5 THz. While all of these circuits are made to be completely "planar" in the sense that there are no connections that lead away from the plane of the circuit, the relatively large amount of topography presents additional challenges when compared with the fabrication of HEMT-based MMICs used at lower frequencies.

**Introduction:**

Schottky-barrier diode circuits for submillimeter wave applications have improved significantly in the past several years, but in many ways the devices and circuits have not taken advantage of recently developed techniques used for microwave MMICs (Monolithic Microwave Integrated Circuits). In particular, practices developed for the design and fabrication of monolithic circuits should make it possible to economically produce better-performing devices with integrated matching and bias structures that can greatly simplify circuit assemblies, improving both the performance and ruggedness of the circuits.

Taking this approach, we fabricated a number of submillimeter wave circuits within the last year. These circuits include:

- A 320 to 640 GHz quasi-optic frequency doubler,
- A 160 to 320 GHz and a 320 to 640 GHz MMIC doubler, along with a 160 to 640 MMIC quadrupler,
- New designs of the 80 to 160 and 160 to 320 GHz planar varactor arrays previously fabricated and reported by the University of Virginia [1], and
- A 2.5 THz integrated mixer.

Performance of these circuits will only be mentioned briefly, as the purpose of this paper is to discuss particular processing techniques. These techniques have the potential to improve submillimeter wave circuit performance and to extend the use of planar circuits to even higher frequencies.

**Device Improvement:**

The approach used to improve device and circuit performance concentrated on developing fabrication techniques for circuits with up to 4 microns of topography that enable: (1) definition of small structures into the submicron regime, (2) tight dimensional control of circuit elements, and (3) tight layer-to-layer alignment tolerances. The resulting processes make possible a wider latitude of circuit designs, permitting the inclusion of more circuit elements and multiple devices, a reduction in device parasitics, and the possibility of higher frequency circuits designs.

In contrast with the wet etches and contact lithography typically used for submillimeter wave circuit fabrication, industry has moved to using dry etches and projection and electron-beam lithography for MMIC fabrication. Adoption, by industry, of these newer techniques was made partly for the economics of high throughput and high yield, but also for enabling the fabrication of structures with smaller dimensions and

tighter tolerances between layers - in other words, to make the "extrinsic" device as similar as possible to the "intrinsic" device.

A Schottky diode's frequency response is typically limited by the series resistance, $R_s$, and the junction capacitance. $R_s$ can be reduced in a number of ways. Assuming the usual device structure shown in Figure 1, much of the series resistance is determined by the area of the anode and the thickness and doping level of the topmost epitaxial layer, all of which are dictated by the application. However, the parasitic components of $R_s$ can be reduced [2] by increasing the length-to-width ratio of the anode, reducing the ohmic contact-to-anode spacing, and by increasing the thickness of the buried n+ layer (Table 1). The last of these techniques encounters diminishing returns due to the effect of skin-depth that occurs in high frequency circuits.

The overall device structure is necessarily larger than the intrinsic device, which gives rise to extrinsic capacitances, losses, and phase lags. By reducing various device dimensions, these extrinsic parameters can be reduced. Through the use of the newer lithography tools and by replacing wet etches with dry etches, we have greatly reduced mesa sizes in order to reduce these extrinsic parameters. These improvements will be pointed out in the specific circuit descriptions below.

Finally, for circuits operating at terahertz frequencies, device sizes and features need to be very small and dimensions well controlled. As part of the fabrication of anodes for fixed-tuned monolithic circuits, we developed a newer version of our T-anode e-beam lithography process [3] that introduces a temporary planarization layer after mesa etching. The new process enables us to take full advantage of the tighter mesa geometries that result from the use of stepper lithography and reactive-ion etching (RIE) of mesas while permitting us to make a 0.05 $\mu m^2$ device with a length-to-width ratio of 5 in order to reduce $R_s$ as much as possible.

## Circuit Fabrication:

Each of the circuits described in this article had a unique process flow. However, we will describe only the 320-to-640 GHz quasi-optic doubler in detail and then discuss differences in the fabrication processes used for the other circuits.

*320-to-640 GHz quasi-optic doubler:*

The process flow for the 320-to-640 GHz circuit is shown in Figure 2. SEM views of the circuit and the diode quad-bridge are shown in Figure 3. All layers in this process were defined by our I-line 5x projection aligner. The smallest dimensions were approximately 1 micron, and tolerances between layers before they would interfere were less than a micron in many cases. Since this circuit was our first to be processed on the projection

aligner, we were doing process development simultaneously with device fabrication. Details on the circuit design approach are listed in [4].

Fabrication starts with the definition of the ohmic contacts, which are recessed a few thousand angstroms to the buried n+ layer. For this step, a wet etch (consisting of a 1:1:38 solution of hydrogen peroxide:phosphoric acid:water) is preferable, as dry etches tend to damage the etched surface, leading to poorer contact characteristics. The etch is shallow enough that the silicon nitride etch mask is only undercut by a small fraction of a micron during this etch. A conventional Ni/Ge/Au/Ni/Ag/Au ohmic metalization is deposited by electron beam evaporation. The ohmic contacts are annealed in a rapid thermal annealer after the mesas have been defined and the silicon nitride mask has been removed.

Next, the mesas were patterned, then etched in an RIE system using a chlorine/boron-trichloride/argon mixture. Because the design of the circuit demanded that the diode quad-bridge be as compact as possible, the nominal mesa-to-mesa spacing is approximately 3 microns, but variations were included on the mask that ranged from 1 micron to 5 microns. All of the mesa separations showed reasonable dc characteristics, although lower breakdown voltages were observed in some cases for the one micron spacings. It isn't known whether the one micron inter-mesa distance is too small to suppress breakdown current with some substrates and processes or whether the photoresist did not fully clear out of the 1 micron gap and thus the subsequent etch did not fully isolate the mesa structures for those devices that exhibited low breakdown voltages.

The anodes and the bulk of the circuitry were metalized in the same processing step. The lithography for this step proved to be the most challenging part of the circuit fabrication. The basic approach used for the step is much like that used for many Schottky metalizations - a photoresist layer optimized for good metal lift-off is defined on top of a rounded, cross-linked, bridge-base photoresist layer. Problems included: (1) the 1 μm x 4 μm anodes are defined partly by the bridge base layer and partly by the metalization mask itself. Thus, the area of the anode is not only dependent on a single lithographic step, but also on an overlay accuracy. (2) The height differential between the tops of the mesas and the semi-insulating substrate is greater than the depth of field of the projection aligner. This problem required us to choose between double exposing the wafers using two separate masks or running two completely separate process steps. (3) The spiral matching circuits included two micron lines and spaces in patterns that would be considered to be very difficult to lift off even with much larger geometries. (4) The ground plane around the outside of the quad-bridge is located only one micron away from the mesas, where the photoresist is much thicker, necessitating a relatively high exposure time. Despite these issues, we obtained a reasonable yield.

The circuit was then passivated using a 1200 angstrom thick silicon nitride dielectric layer, deposited in a Plasmatherm PECVD reactor. Contact vias were opened in the nitride using a $CF_4/O_2$ etch. . After additional patterning, a final air-bridge metal was deposited to supply the top plate of the bias line capacitors and tie them to the neighboring ground planes. This metalization also forms the air-bridge structure seen in Figure 3(b), which is intended to suppress slot-line modes that may otherwise propagate along the coplanar waveguide. Finally, the wafers were lapped to a thickness of approximately 125 μm before being scribed into individual die.

The rf measurement results will be reported at a later date, but preliminary results show up to 1.4 mW output power from a quad bridge made of 1 μm x 4 μm diodes. The minimum loss was about 16 dB with 0.53 mW associated output power.

*MMIC multipliers:*
Details on the microstrip MMIC multipliers appear in [5]. The process was essentially similar but significantly simpler than the process for fabricating the quasi-optic doublers due to the lack of small structures off- mesa on the semi-insulating GaAs layer. In addition, overlay dimensions other than ohmic-to-Schottky were significantly larger.

However, wafer thinning is much more critical to microstrip performance, and the high frequencies of these circuits necessitate the thinnest wafers possible in order to suppress the propagation of undesired radiation through the substrate. Once the MMICs were through front-side processing, a sequence of lapping and polishing steps was used to thin the wafers. The difficulty of maintaining a reasonable yield for these relatively large circuits while thinning samples to tens of microns, required that we trade off some performance with final chip thickness. For this design, we chose a target thickness of 50 μm. We were able to deliver at least some circuits with thicknesses within a few microns of this target. Figure 4 shows an SEM of a typical device.

DC characteristics of these diodes were excellent. For example, a 1.2 x 7 micron diode that was predicted to have a minimum possible series resistance of 5 Ω (without considering the limited ohmic contact area) and a breakdown voltage of 7 V, was measured to have an $R_s$ of 5.9 Ω and a breakdown voltage of 5.9 V.

*Array multipliers:*
The highest multiplier power outputs measured to date at about 160 GHz and 320 GHz were obtained using varactor diode arrays mounted in waveguides [1]. Unfortunately, current requirements demand significantly higher power outputs. It is believed that higher power could be obtained by simply increasing the number and anode area of the diodes in proportion such that the approximate active impedance of the devices stays the same - in this case, we increased the number of devices in each leg from two to three and increased the anode area by 1.5. For the new design the mesa areas of the devices are

much smaller in order to reduce parasitic, distributed capacitances. The devices are shifted towards the ground contacts, and the spacings between them are adjusted in order to reduce phasing problems. The nominal doping of the circuits is the same as previously reported [1] - approximately $1.2x10^{17}/cm^3$ for the topmost layer for 160 GHz circuits, and approximately approximately $2.5x10^{17}/cm^3$ for the topmost layer for 320 GHz circuits. The buried n+ layer is significantly thinner than previously reported - 1 micron for the rf results reported below, and 2 microns for the latest devices.

SEM photographs of the overall circuits and a device are shown in Figure 5. The fabrication process was exactly as described for the MMIC multipliers except that the last metalization layer included a nickel barrier layer to permit soldering, and that a selective $Cl/BCl_3/SF_6$ etch was used for the mesa etch for the most recent lot. DC parameters from the latest run, taken before thinning, are shown in Table 2. The best rf data from the first run of devices indicated a record power output of 76 mW at 160 GHz with an efficiency of 22% for devices with anode sizes of 3 μm x 7 μm x 2 fingers despite much higher-than-anticipated capacitances and the thin n+ layer.

*2.5 THz mixers:*

Mixer devices monolithically integrated with slot antennas, IF filters, and IF coplanar waveguide lines were fabricated on GaAs [6] with a topmost layer doped to $1x10^{18}/cm^3$ and a 1 micron buried n+ layer. The extremely small sizes and overlay tolerances along with the short turnaround time led us to use our JEOL electron beam lithography system for several of the layers instead of the optical projection aligner.

Other than using the different lithography tools, most of the process was much as described above with the exception of the anode process. We had previously reported a new e-beam anode process that could be used with wet-etched mesas defined after the anode layer [3]. For the current layouts, the mesa sizes and separations were so small that they had to be defined by dry etching prior to anode formation.

In order to fabricate air-bridged T-anodes [3] on top of the already-defined mesas, it was necessary to temporarily fill in the gap between the mesas. This was done by spinning PMMA to a thickness of 4 microns, and then iteratively flood exposing the sample with deep-UV and developing the PMMA until the tops of the mesas were just clear of the PMMA. The usual tri-layer PMMA/copolymer/PMMA resist structure can then be processed on top of the planar PMMA layer as previously reported.

In addition, it is possible to make connections off-mesa by grading the e-beam exposure of the thick, planarizing PMMA layer. We were unable to optimize this process in the short time that we had available, but working devices were obtained by exposing and developing the T-anodes and off-mesa interconnect metal in one lithography step.

Finished devices (Fig. 6) had anode areas of 0.1 x 0.5 $\mu m^2$ and 0.1 x 1 $\mu m^2$. The lowest measured $R_s$ value was about 30 Ω. Modeling leads us to believe that much of this resistance may be due to the very small ohmic pads necessitated by the compact coplanar environment of the devices.

**Conclusions:**

We have reported on a number of monolithic integrated circuits fabricated within the last year for submillimeter wave applications. It is clear that overall device sizes and geometries must be more compact and more accurate than for lower frequency circuits. By using better forms of lithography and other processes that allow us to reduce device sizes and overlay tolerances, and by optimizing the device geometries in order to take advantage of these device improvements, we have shown that monolithic circuits can be made with reproducible and predictable devices with state-of-the-art performance.

**Acknowledgements:**

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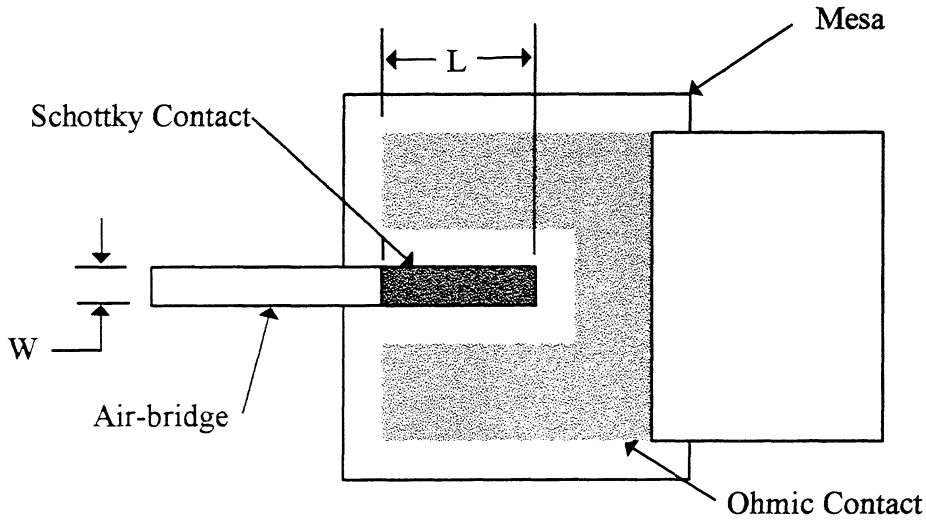



Figure 1. Basic geometry for the mesa area of a Schottky diode.

| Buried layer thickness | $R_S$ |
|---|---|
| 0.5 μm | 4.3 Ω |
| 1.0 μm | 3.2 Ω |
| 2.0 μm | 2.6 Ω |
| 4.0 μm | 2.3 Ω |

1.a.

| Length | Width | $R_S$ |
|---|---|---|
| 2.0 μm | 4.0 μm | 3.1 Ω |
| 4.0 μm | 2.0 μm | 2.6 Ω |
| 8.0 μm | 1.0 μm | 2.3 Ω |
| 16.0 μm | 0.5 μm | 2.0 Ω |

1.b.

Tables 1.a. and b. Calculated [2] series resistance of a Schottky diode as a function of (a) buried layer thickness and (b) length and width with eight $\mu m^2$ anode areas. For both tables, the top layer doping is $2.6 \times 10^{17}$ /$cm^3$ with a thickness of 210 nm, the buried layer is doped to a level of $5 \times 10^{18}$ /$cm^3$ , there is a 1.5 μm anode-to-ohmic contact spacing, and the contact resistivity is $10^{-7}$ $cm^2$. For table 1.a., L=4 μm and W=2 μm. For table 1.b., the buried layer thickness is 2 μm.

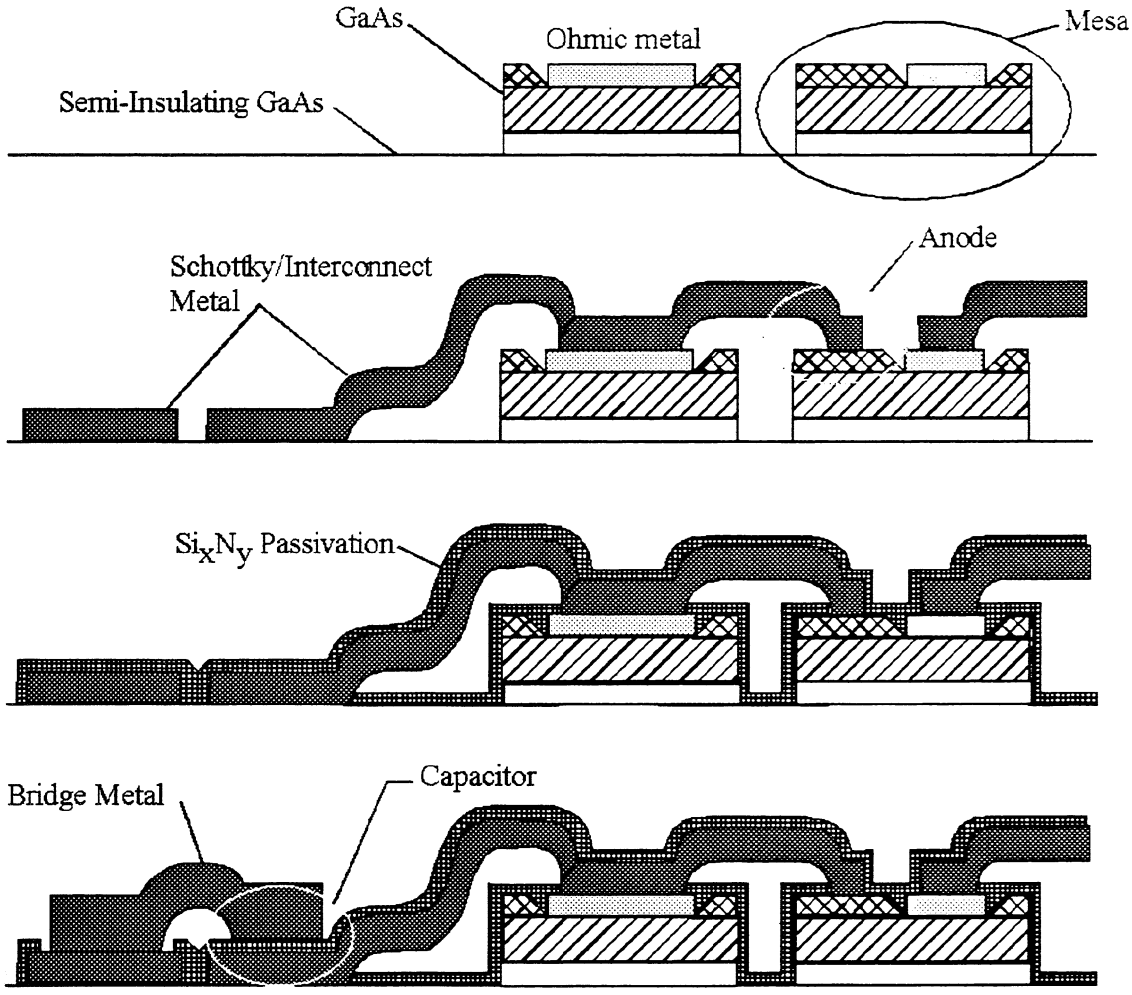
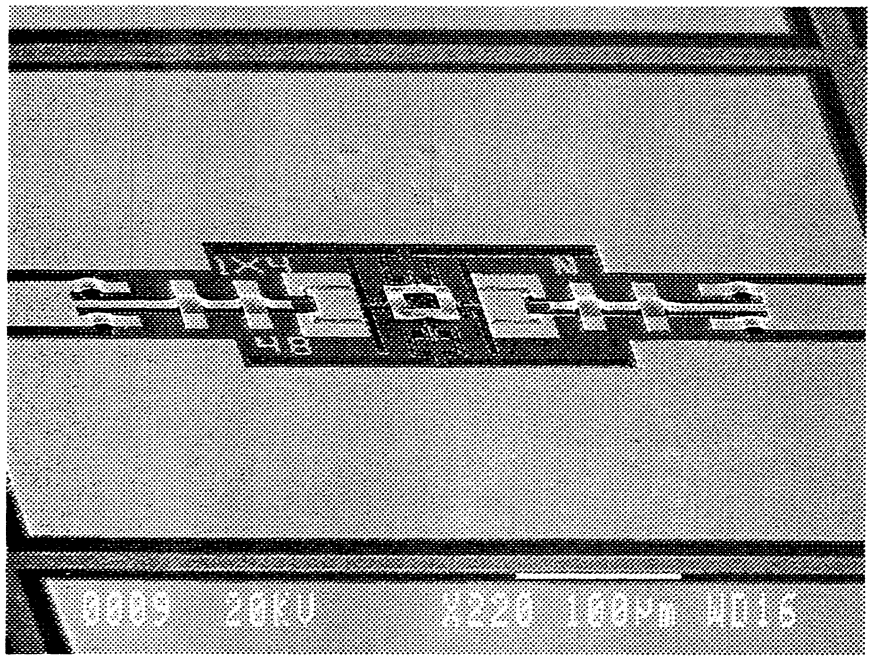
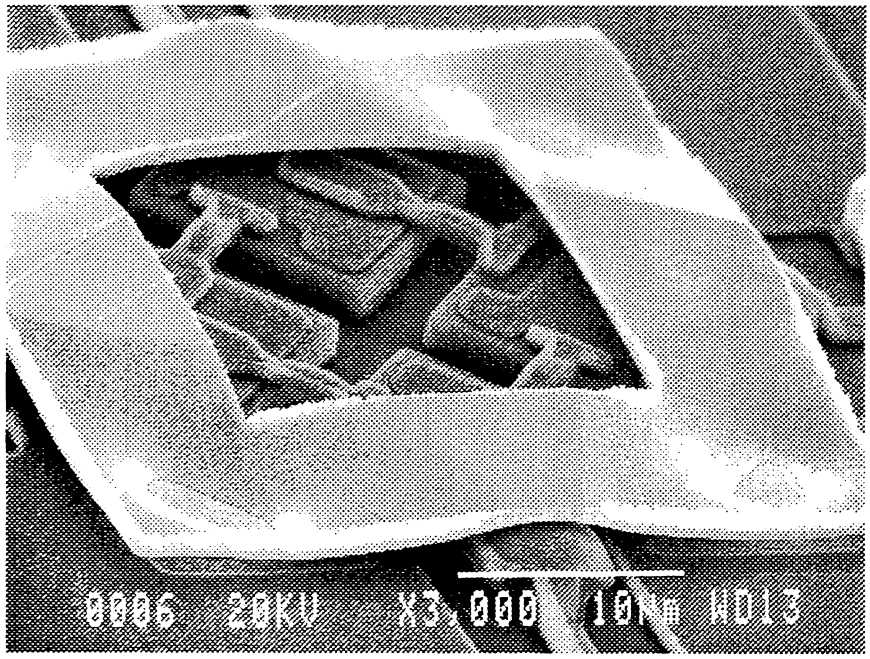



Figure 2: Process flow for quasi-optic, 640 GHz doublers.



(a)



(b)

Figure 3: SEM photographs of the quasi-optic doublers. In (a), the diode bridge can be seen between the faint horizontal input slot antennas and the vertical output slot antennas. The bias lines extend to the right and left sides of the picture. Fig. 3.b. shows a close up of the four diodes. The large air-bridge structure across the top of the bridge is meant to suppress slot modes by tying together the ground planes.

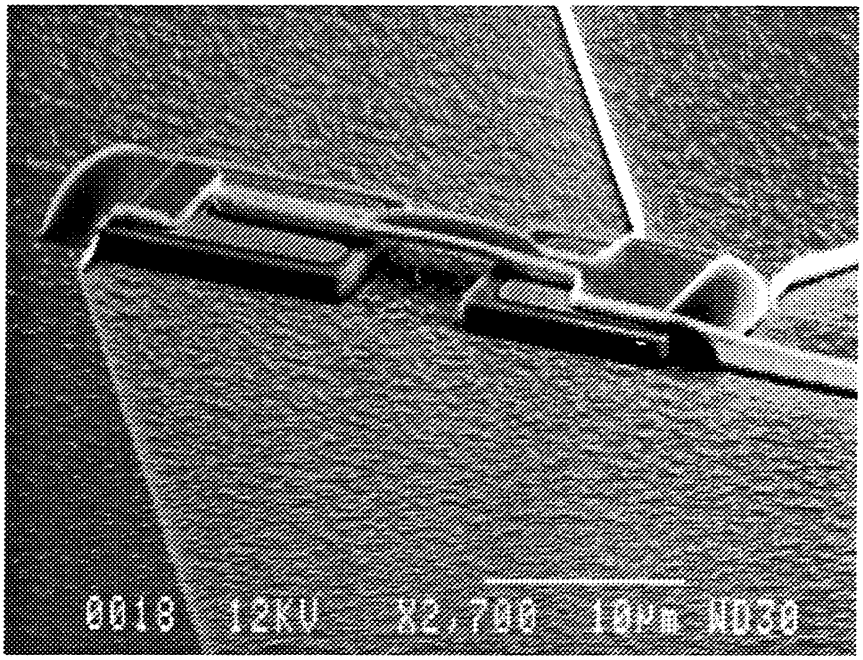



Figure 4. SEM photograph of a diode from one of the microstrip multipliers. The anode is on the left-hand mesa. Radia stubs extend to the upper right and lower left corners of the photograph.

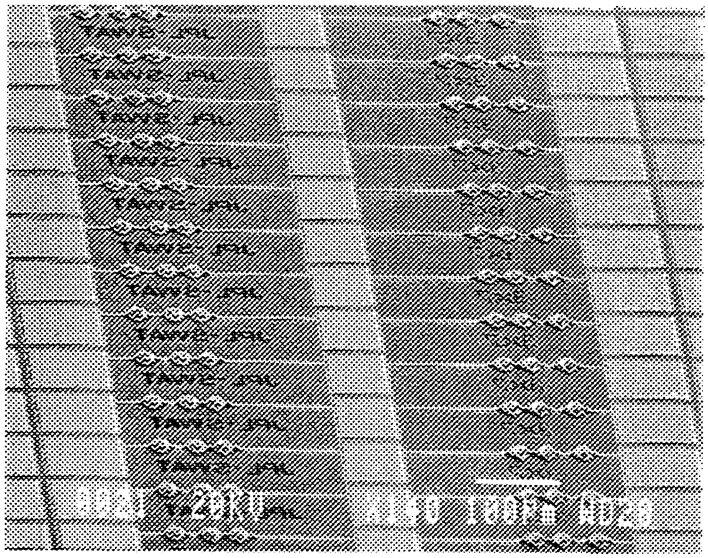
Wafer 0.031XT: $N_d \sim 1.2 \times 10^{17}/cm^3$

| Size (μm x μm) | Is (fA) | Ideality factor | Rs (Ω) |
|---|---|---|---|
| 3 x 7 x 2 | 37 fA | 1.13 | 2.96 |
| 3 x 7 x 2 | 44 | 1.14 | 2.82 |
| 1.5 x 14 x 2 | 54 | 1.15 | 2.56 |
| 1.5 x 14 x 2 | 70 | 1.15 | 2.53 |
| 1.7 x 4 x 2 | 27 | 1.18 | 4.32 |
| 3 x 8.4 x 2 | 51 | 1.13 | 3.1 |
| 3 x 8.4 x 2 | 53 | 1.13 | 3.0 |

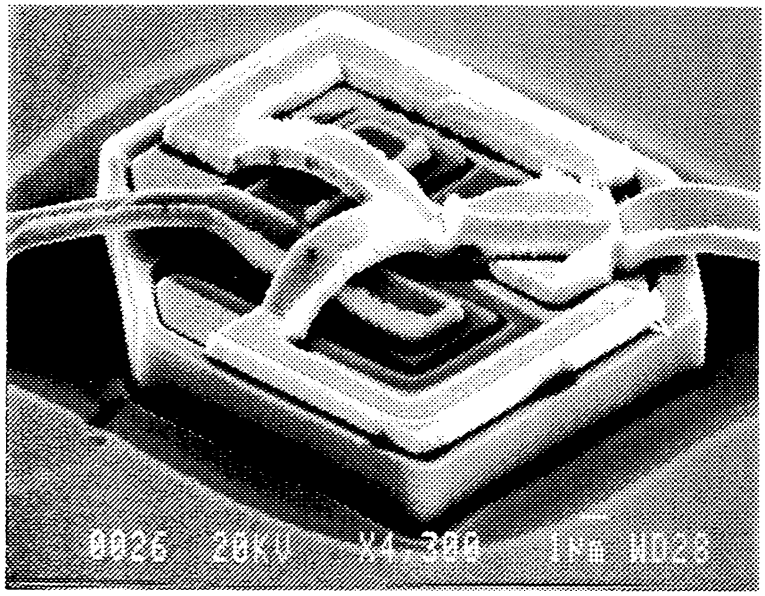
0.019 SU $N_d \sim 2 \times 10^{17}/cm^3$

| Size (μm x μm x n) | Is (fA) | Ideality factor | Rs (Ω) |
|---|---|---|---|
| 1.7 x 4 x 2 | 42 | 1.16 | 3.67 |
| 1.5 x 3 x 2 | 32 | 1.17 | 4.42 |
| 1.5 x 14 x 2 | 75 | 1.14 | 2.57 |

Table 2. DC parameters of devices from recent wafers with varactor diodes as shown in figure 5. The sizes are expressed in microns x microns x number of parallel anodes per device. The series resistances include a probe resistance of approximately 0.7 Ω.

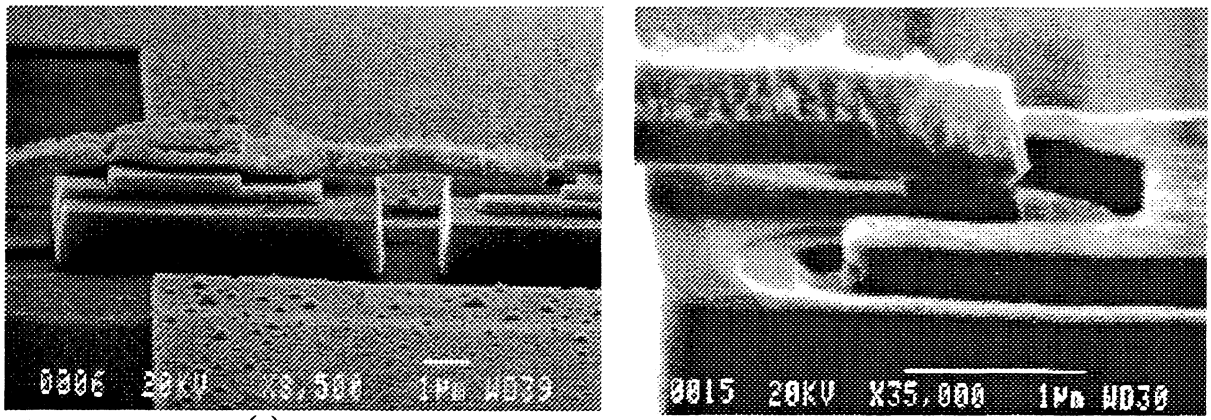


(a)



(b)

Figure 5: SEM photographs of (a) 6-element arrays and (b) a single diode. In (b), the bridge to the anodes comes from the left side of the photograph. The active device area is formed by two 3 x 7 $\mu m^2$ rectangular anodes.




(a) (b)

Figure 6: Close-up views of 0.1 x 0.5 $\mu m^2$ diodes in coplanar waveguide/slot antenna structures for 2.5 THz detection. The active mesa area is approximately 4.5 x 5 $\mu m^2$.