RECENT PROGRESS ON THE SUPERCONDUCTING IMAGING RECEIVER AT 500 GHz

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New integrated receiver chips with a superconducting FFO on a Si substrate are designed in order to match silicon optics. A solution for the problem of spatial mismatch between the silicon-immersed double-dipole antenna and the SiO_2-based microstrip tuning circuit is found and tested experimentally. A number of single mixer pixels for the imaging array receiver are fabricated and tested. Preliminary results of a balanced SIS mixer are given. The integrated lens antenna was tested with a reference SIS mixer showing sidelobes at approximately - 17.5 dB and a DSB receiver noise temperature T_{RX} 130 K. A T_{RX} = 200 - 300 K and 110 - 150 K is obtained at 480-520 GHz for the single and balanced mixers respectively using the internal LO. A prototype of the FFO shield was tested with the magnet of 1000 Gauss. A computer system "IRTECON" is developed based on LabWindows for precise computer control of the chip device and the receiver complete characterization.

Introduction

A low-noise imaging array receiver (IAR) for the radio astronomy or monitoring of the atmosphere pollution is of general interest since it may save observation time and most of related technical and financial resources. IAR may contain pixels based on the Superconducting Integrated Receiver (SIR) chip which consists of a low-noise planar antenna SIS mixer and a flux-flow oscillator (FFO) as a local oscillator [1, 2]. This concept of chip-size, light-weight and low-power consuming SIR is very attractive for most imaging applications because dense packaging of such chips is possible. The independent control of each pixel seems to be an advantageous feature either for optimization of LO power or for multi-frequency operation of the array receiver.

We present here results of the experimental study of recently developed SIR device intended for a nine-pixel IAR [2] with silicon optics. The goal of the study is to demonstrate that each pair of pixels can work at about 500 GHz independently and equally good. The detailed study of the phase-lock (or frequency-lock) loops [3] for the integrated LO is the last option that has to be accomplished for the practicable receiver.

A few problems were found in going from quartz to the silicon substrate. The design principles developed for SIR on a silicon substrate/lens are discussed below. The main optical cryostat with a large (array) input window is being assembled. Test data reported here were obtained with a special single-pixel assembly cryostat.

I. Design of New Silicon Device

The simplified electrical diagram of the new SIR on silicon and a photograph of the chip are shown in Fig. 1 and Fig. 2 respectively.

a) Antireflection coated optics

Each pixel of IAR has its own elliptical silicon lens (R_1 = 5 mm, R_2 = 5.228 mm). This lens has to be the only optical element providing a beam f/10 at 450 - 550 GHz [4, 5]. The silicon lenses with antireflection (AR) coating from Stycast epoxy have been fabricated by diamond turning. Two epoxy compounds art. 2850 FT and art. 1264 were tested for the AR-coating using FTS technique. We have found for a number of different tests that AR-coating made from epoxy 2850 FT has 5.2 instead of 4 reported in [6]. Extra absorption was also suspected because of unspecified carbon filler in this epoxy. The AR-coating of 87 m fits the requirements [7] for epoxy 1264 (2.9). However, the data reported here were measured only for the lenses with the 75 m AR-coating from 2850 FT epoxy.

b) Antenna mixer

We continue with the concept of a quasi-optical double-dipole antenna SIS mixer [1, 2, 4]. This kind of integrated lens antenna must have a back reflector installed at the quarter-wave distance to achieve the

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beam of good symmetry. The back reflector is a silicon chip (800 m 800 m, thickness 44 m) which is one-side covered with a film of Nb/Au. To install the back reflector onto the SIR chip, a tiny drop of the vacuum oil was used. A double-dipole antenna with the back reflector could be treated as a four-dipole array immersed into a homogeneous silicon medium ($_r$ = 11.7). Center of the antenna array has to be placed in the focus of the elliptical lens. Because of homogeneity of the medium surrounding the antennas, one may hope that the relatively simple analytical formulas developed for a thick wire dipole antenna are accurate enough to estimate the main properties of the real device. The beam inside the silicon media was estimated analytically taking into account the mutual interference of all four antennas. The calculated main lobe was found to be consistent with the results obtained via the method of moments. Since the microstrip feeders connecting the antennas may somewhat change the impedance of the dipoles, the experimental samples are designed with three slightly different lengths of their antenna (84 m, 92 m and 100 m).

c) SIS mixer tuning

To achieve a low noise performance of the receiver, the mixing SIS junction has to be tuned to cancel its capacitance. A modified concept of the end-loaded stub is used in the tuning structure. The mixing junction can be treated as a shared load placed in the center of a microstrip line half-way from two antennas. Each half of the microstrip feeder is acting as an inductive tuner which cancels capacitance of the half-junction at the specified frequency of about 500 GHz.

The insulation film of SiO_2 ($_r$ 3.8) is currently used that defines an optimal length of the tuning lines as 2 60 m while the optimal distance between the antennas is 2 35 m ($_r$ 11.7). Unlike a double-slot antenna [8], it seems not possible to bend the tuning lines freely in the space available between two dipole antennas. This problem was solved by tuning each dipole antenna with an additional capacitive tuner (Fig. 1 and Fig. 3). To make length of the complete tuning structure as short as possible, thinner insulation of 150 nm is used for the tuners instead of 250 nm for the rest of the chip circuitry. The same tuning microstrip is used for supplying the magnetic field to the junction. A strip of narrower width can give a stronger magnetic field in the vicinity of the junction. The width of 3 m is chosen

for the tuning strip because of the limited mask alignment accuracy. A fabrication misalignment not more than 0.5/1 m is desired/allowed for the proper operation of the device. A microphotograph of the double-dipole antenna SIS mixer is shown in Fig. 3.

d) LO power coupling

To couple the LO power from FFO with an estimated output impedance of about 0.4 [1, 2], the two-stage impedance transformer has been synthesized empirically as a stair-type microstrip connection. The SiO_2 insulation of 150 nm is used for the widest section of the transformer. The LO power is supplied from FFO to the mixing junction via a microstrip transmission line of about 900 m long and 4 m wide. The characteristic impedance of the line is about 14 . A *dc*/IF break in both leads [9] is inserted at about half-way between the LO and the mixer (Fig. 1 and Fig. 2).

To couple the LO power from FFO to the mixing junction, a microstrip T-connection working similar to a cold beamsplitter is implemented. The LO port is presented by a 1 m wide strip which acts as a section of a quarter-wave transformer providing high impedance of the LO path (60) in parallel to the mixing SIS junction. The impedance of the LO port allows about 20-30 % of the signal to be lost.

To avoid the signal loss, the concept of a balanced SIS mixer have been developed [2]. The balanced device can use 100 % of both signal and LO power that may result in the lower noise temperature of the receiver.

II. Single Pixel Test Unit

A special unit is developed to test each pixel for the array separately (Fig. 4). The SIR chip device (4 mm 4 mm 0.5 mm) is centered within an accuracy of 10 m and then glued to the lens at the corners with soft epoxy art. 2216 from "3M". All electrical contacts are provided by the wire bonding (Al wire 50 m) to a printed circuit board which presses the lens down against a cold metal frame. The pentagonal frame of the pixel is mounted on a copper "leg" which is holding the chip far enough from the opening of the shielding can. The shield of the test unit is made similar to one described in [2], but smaller in size. The shield and the "leg" are thermally isolated from each other having independent heat contacts to the bottom of the liquid helium bath. The external layer of the shield is bent from -metal; internal one is made from copper galvanically covered with 100 m layer of led. Both the internal superconducting shield and the chip can be heated independently above their superconducting transition temperature point to remove trapped magnetic flux. All wiring of the chip (including IF cable) is made through the same and only opening of the shielding can.

III. Experimental Data and Discussion

a) Magnetic shield test

A shield around the integrated receiver chip is necessary because any current or magnetic field noise

influences the LO frequency of integrated FFO. The magnetic shield (Fig. 4) was tested qualitatively by placing a magnet with strength 1000 Gauss near the cryostat window at the distance of 5 cm from the opening of the shield. The effect of about 4 V shift of the FFO bias point has been measured that is equal to the LO frequency shift 2 GHz. This effect can be compensated by the FFO control line current of approximately 50 A that in terms of magnetic field means a suppression factor of 10^{-3} - 10^{-4}. As a consequence the flux trapping only seldom occurred for the experimental chips.

b) SIS mixer control line test

It is known that superconducting strips of a few microns most efficiently generate a local magnetic field. However, is has been found experimentally that for the Nb film of 3 m wide and 0.6 m thick, the critical current can be reduced to about 10 mA due to the non-rectangular (diffused) profile of the film fringe. To get the rectangular profile of the fringe, the fabrication procedure for the wiring layer has been improved. Third minimum of $I_c(H)$ is achievable now with the control line current of 80 - 100 mA for 1 - 2 m^2 junction.

c) FTS test

To learn about the instantaneous bandwidth, a FTS test is performed for each SIR chip assembled into the cryostat. The preliminary dipstick test does also show a frequency response of the SIS mixer since the internal FFO is emitting approximately equal *rf* power within the 450 - 650 GHz frequency range [9]. However, this estimate is usually a bit higher than one made in the cryostat because the installation of the backing reflector is decreasing the antenna resonant frequency 15 - 20 GHz. The FTS experiments have demonstrated the central frequency of the new silicon SIRs within 490 - 520 GHz and the instantaneous bandwidth of 70 GHz and 90 GHz for the single and balanced mixers respectively that agrees well with the design values.

d) Antenna beam test

The typical antenna beam pattern of the new silicon SIR is shown in Fig. 5. The SIS mixer was operating in the video-detection mode that limits the dynamic range to 25 - 30 dB. Taking into account the radiation pattern of the 2 mm aperture used to obtain the wide-angle illuminating, the following data are obtained for the SIR chip H7341 at 490 GHz: the sidelobe level of about - 16 dB, the full 3 dB beamwidth of about 3.7 and the full 10 dB beamwidth of about 6.7. The first minima in the radiation pattern occurs approximately at 4.5. This corresponds roughly to a f/9.4 beam with a waist size w_0 3.6 mm.

The antenna beam of a reference SIS mixer *without* LO path was similar, indicating that LO circuitry has a minor effect. The choke filters are connected now to the capacitive tuners at more distant position that may reduce the distortion of the antenna beam pattern. To minimize the space occupied by the choke filters without reducing their quality, the high-impedance section is designed as a coplanar two-wire line while the low-impedance sections are made as overlaps (microstrip line) that provides desirable discontinuity (variation) of impedance. The antenna beam had a gaussian profile with sidelobes at the level of about - 17.5 dB that is close to the theoretical prediction [5]. The receiver DSB noise temperature measured for the reference SIS mixer is about 130 - 140 K at 490 - 495 GHz (corrected to the 20 m Mylar beamsplitter). The goal of the study is to achieve the same noise temperature with the complete Integrated Receiver.

IV. "IRTECON" System for Data Acquisition and Receiver Control

The experimental study of the Integrated Receiver devices was started with manually controlled bias supply comprising four floating *dc* sources adjusted separately (Fig. 1). It took hours even for the short *dc* check. A data acquisition system called IRTECON was developed for the ***I***ntegrated ***R***eceiver ***Te***st and ***Con***trol (Fig. 6). It collects *dc* and *rf* data automatically. The program is written under LabWindows. Two computer cards from "National Instruments" are used: 16 bit resolution card for FFO and 12 bit resolution card for the SIS mixer. The GPIB interface for SR510 lock-in amplifier, 4 DAC and 10 ADC are used in the system to hookup the analogue bias supply and HP436 power meter to the computer. The complete test run takes now about 45 minutes per device including mounting into dipstick and printing the selected data-graphs (Fig. 7).

One of the routines does optimization of magnetic field for the FFO and the best bias for the SIS mixer providing minimum of the receiver noise temperature, T_{RX}, at particular frequency, f_{LO}, related to the FFO voltage, V_{FFO}, with the Josephson's relationship

$$f_{LO} = 2eV_{FFO}/h.$$

Here e and h are the charge of electron and Plank's constant respectively.

The LO power supplied to the SIS mixer is varied via FFO bias current while the LO frequency is kept constant being adjusted via magnetic field (control current of the FFO). The Y-factor is measured at IF 1.5 GHz with a fast *rf* detector, lock-in amplifier and running "hot/cold" chopper. Since the traces of T_{RX} versus mixer bias are *not* usually crossing each other, the lowest noise figure always belongs to the lowest curve. It means that optimum pump level can be found using any bias voltage, V_{SIS}, within the range of about 1-2.5 mV. The data on the receiver

DSB noise temperature at the level of 250 K optimized by IRTECON are presented in Fig. 8. For the balanced SIS mixer [2] a noise temperature of 110 - 150 K at 515 GHz has been measured recently.

Conclusion

The performance of the Superconducting Integrated Receiver (SIR) with a silicon lens/substrate has been demonstrated as following: center frequency is about 500 GHz, instantaneous bandwidth 15 %, DSB receiver noise temperature 200 - 250 K at the center frequency, the antenna beam f/10 with sidelobes below - 16 dB.

The shielding of FFO was tested and found to be sufficient at the magnetic field about 1000 Gauss.

Recent results of a balanced SIS mixer [2] are promising: T_{RX} 110-150 K at 515 GHz and instantaneous bandwidth 20 % (FTS data).

The system IRTECON is proven to be a useful tool in selection and operation of Superconducting Integrated Receiver.

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References:

[1] V. P. Koshelets, S. V. Shitov, L. V. Filippenko and A. M. Baryshev, H. Golstein, T. de Graauw, W. Luinge, H. Schaeffer, H. v.d. Stadt. *First Implementation of a Superconducting Integrated Receiver at 450 GHz*, Appl. Phys. Lett. **68** (9), pp. 1273-1275 (February 1996).

[2] S. V. Shitov, V. P. Koshelets, A. M. Baryshev, L. V. Filippenko, J.- R. Gao, H. Golstein, Th. de Graauw, W. Luinge, H. van de Stadt, N. D. Whyborn, P. Lehikoinen. *Study of a quasioptical superconducting integrated receivers for imaging applications at 400-700 GHz*. Proc. of 8th Int. Symp. on Space Terahertz Technology, Harvard Univ., Cambridge, MA, pp. 281-290 (March 1997).

[3] V. P. Koshelets, S. V. Shitov, A. V. Shchukin, L. V. Filippenko, J. Mygind, A. V. Ustinov. *Self-pumping effects and radiation linewidth of Josephson flux-flow oscillators*. Phys. Rev. B, 56, No. 9, pp. 5572-5577 (September 1997).

[4] A. Skalare, Th. de Graauw and H. van de Stadt, *A planar dipole array antenna with an elliptical lens*, Microwave and Optical Technology Letters, vol. 4, pp. 9-12, 1991.

[5] M. J. M. van der Vorst, *Design and Analysis of integrated lens antennas*, Graduation report, Fac. of Electrical Engin., Eindhoven Univ. of Tech., 1995.

[6] J. Zmuidzinas, N. G. Ugras, D. Miller, M. Gaidis, H. G. LeDuc, J. A. Stern. *Low-Noise Slot Antenna SIS Mixers*. IEEE Trans. on Appl. Superconductivity, vol. 5, No. 2, p. 3053, June 1995.

[7] M. J. M. van der Vorst, P. J. I. de Maagt and M. H. A. J. Herben, *Matching layers for integrated lens antennas*, Proc. of the Int. Symp. on Antennas, (JINA '96), pp. 511-515, 1996, Nice, France.

[8] J. Zmuidzinas, and H. G. LeDuc, *Quasi-optical slot antenna SIS mixers*, IEEE Trans. on Microwave Theory and Tech., vol. 40, pp. 1797-1804, 1992.

[9] S. V. Shitov, V. P. Koshelets, A. V. Shchukin, A. M. Baryshev, I. L. Lapitskaya, L. V. Filippenko, Th. de Graauw, J. Mees, H. Schaeffer, H. van de Stadt. *Experimental Study of a Superconducting Integrated Receiver at Submillimeter Wavelengths*. Digest of 19th Int. Conf. on Infrared and Millimeter Waves, Report M7.11, pp. 122-123, Sendai, Japan, (October 17-20, 1994).

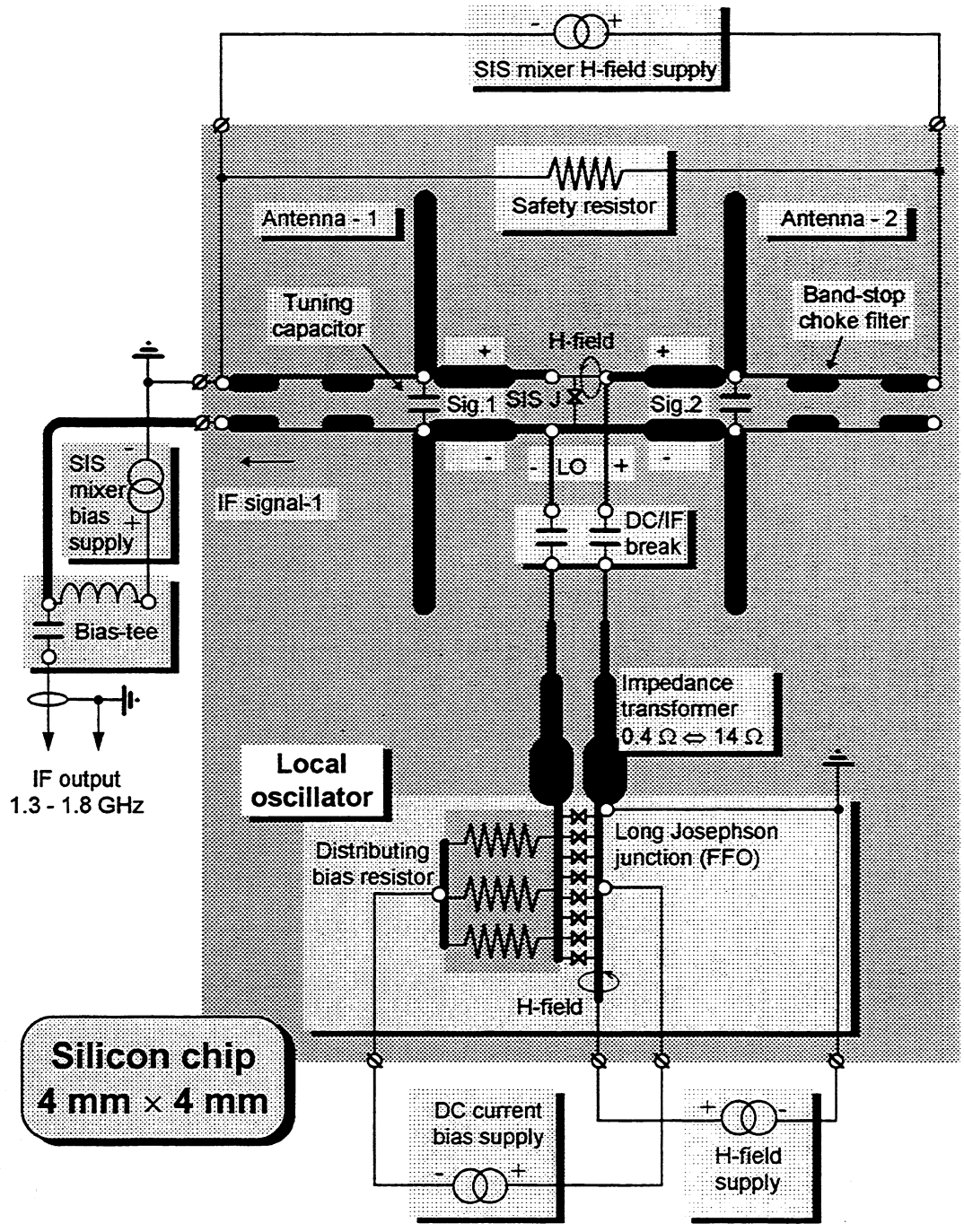

Fig. 1. Simplified equivalent diagram of the single mixer Integrated Receiver chip for 500 GHz; SISJ presents the mixing junction. Typical power consumption of the chip is defined mainly by FFO and estimated as 20 - 40 μW.

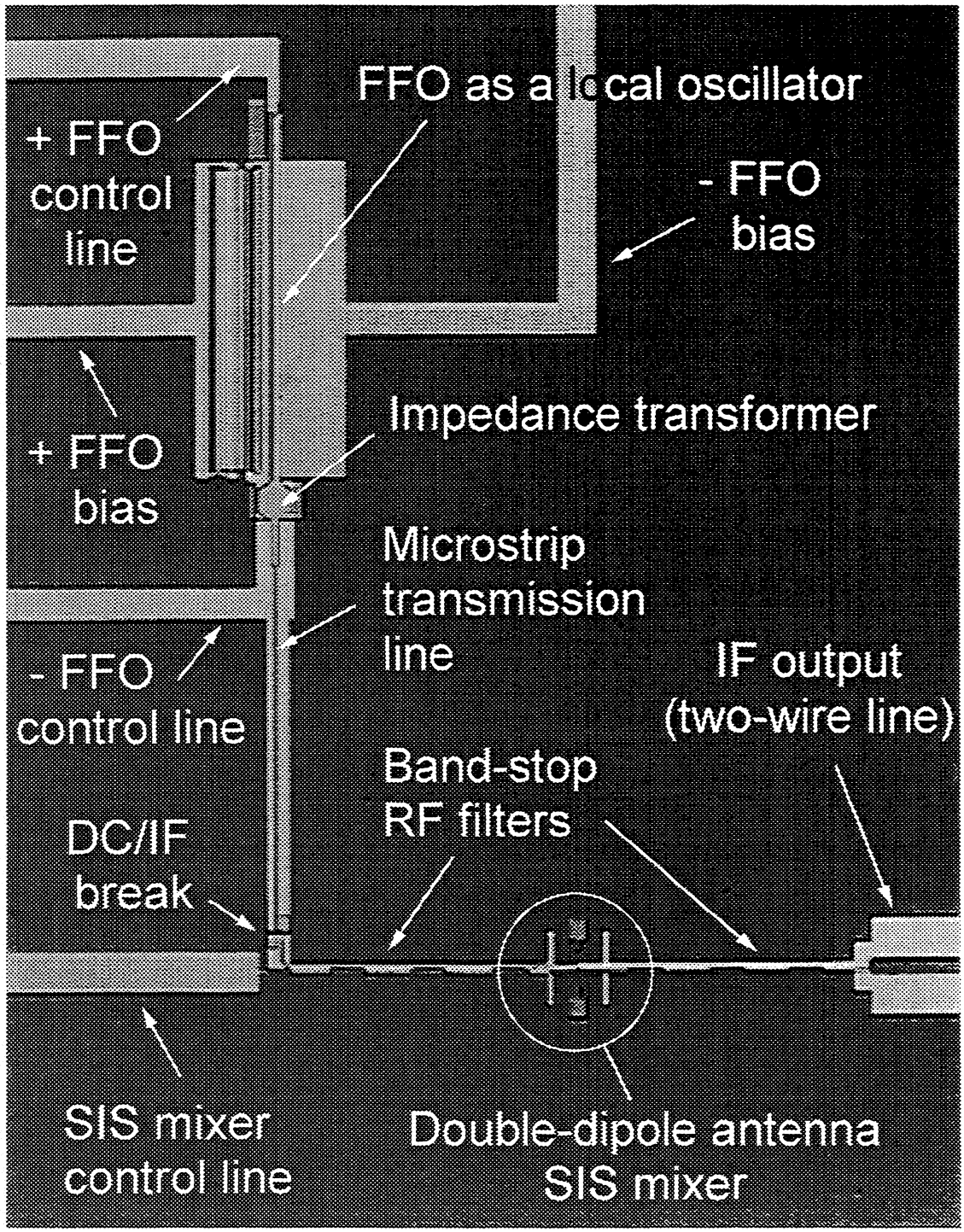

Fig. 2. Microphotograph of central part of the silicon Integrated Receiver chip; all main elements presented; the backing reflector is not installed; some details of wiring and contact pads are out of the field of view which is about 1 mm × 1.5 mm.

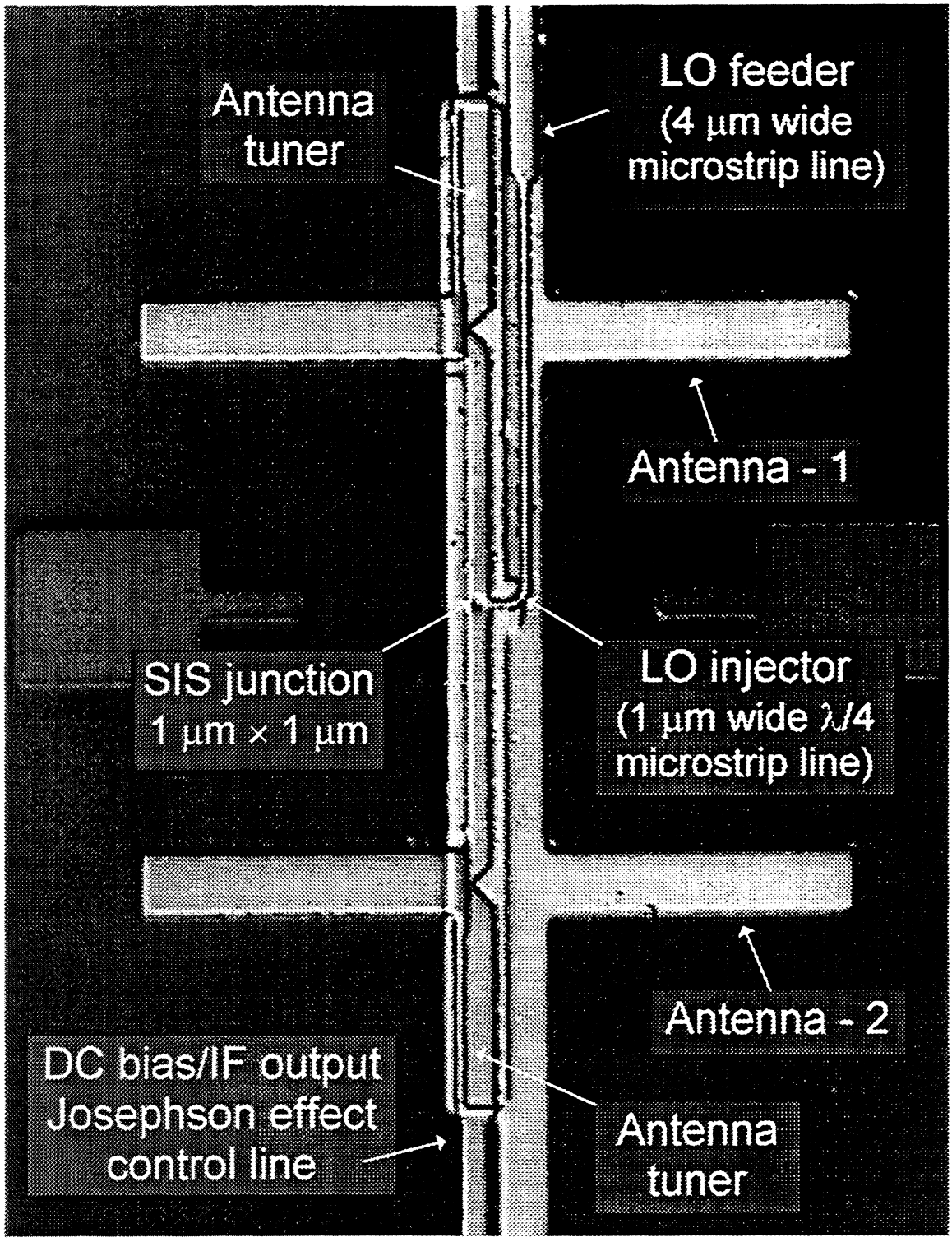

Fig. 3. Microphotograph of the double-dipole antenna SIS mixer of the Integrated Receiver; both antennas are tuned by special microstrip tuners; the local oscillator feed is shown. Complete field of view is about 100 μm × 150 μm.

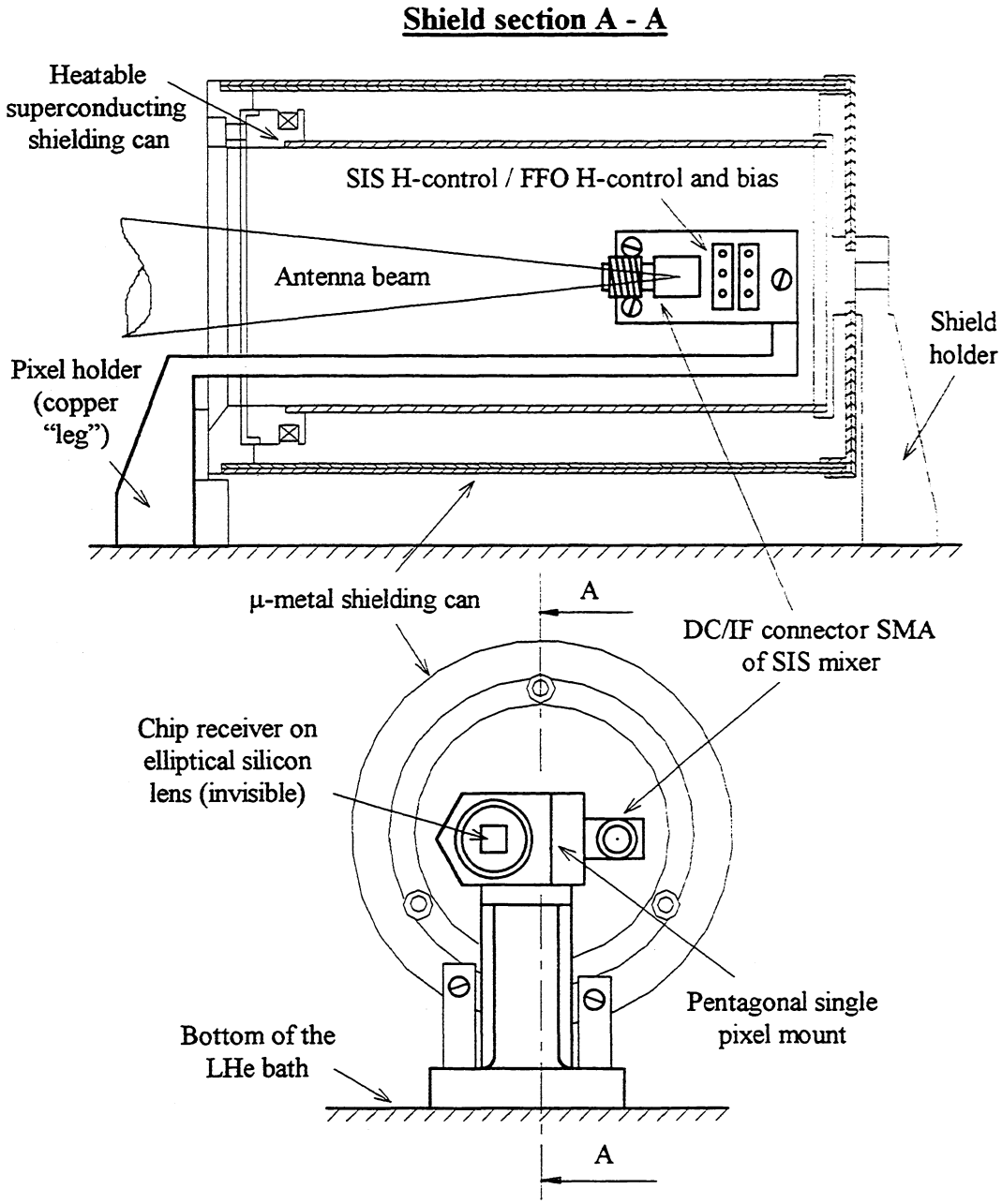

Fig. 4. Schematic drawing of the test mount for single pixel measurement. Note that the optical axis of the silicon lens is not centered in respect to the shielding can. This configuration should simulate the antenna beam conditions for a side pixel of the array receiver. Coaxial IF cable and bias wiring are not shown for simplicity.

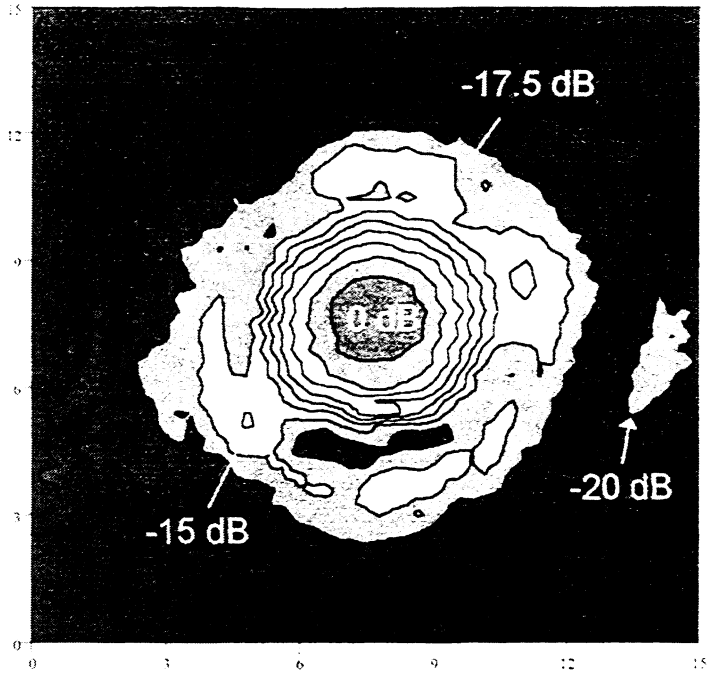

Fig. 5. Far field beam pattern of the Integrated Receiver sample with 92 μm long antenna: contour step is 2.5 dB; covered area is 150 mm × 150 mm; distance from the chip is 33 cm.

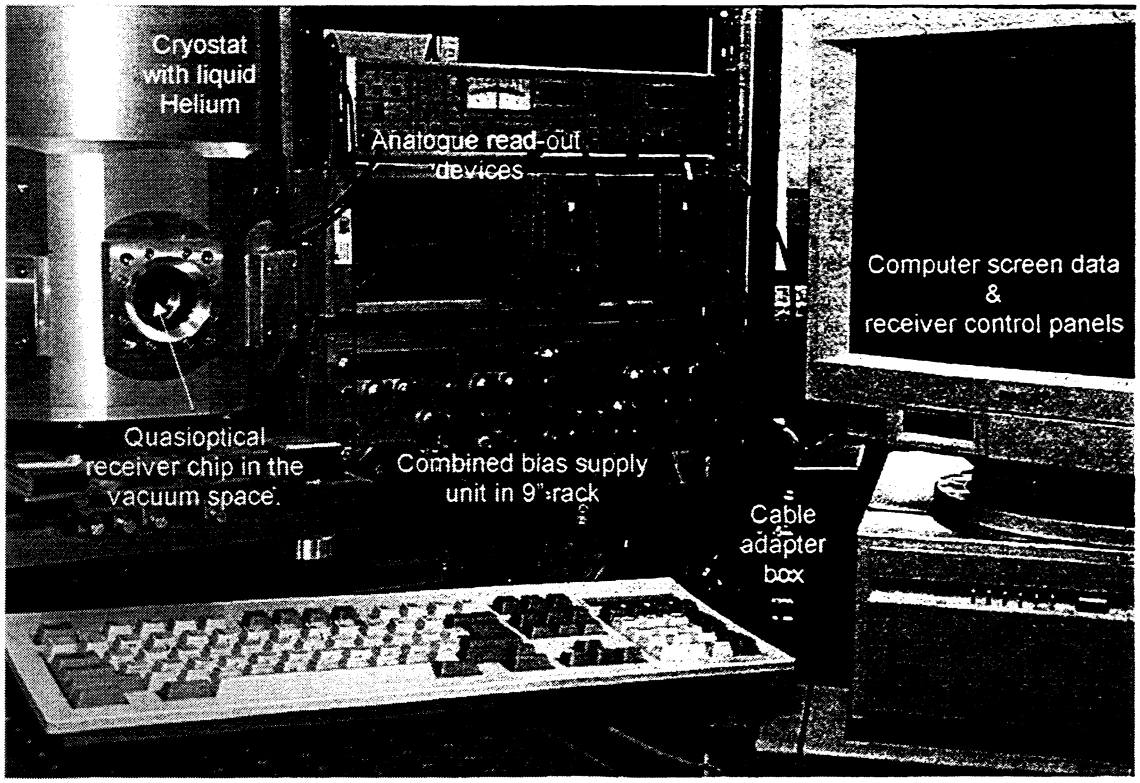

Fig. 6. Photo of the experimental setup: optical liquid Helium cryostat with the receiver, bias supply unit and controlling computer are shown.

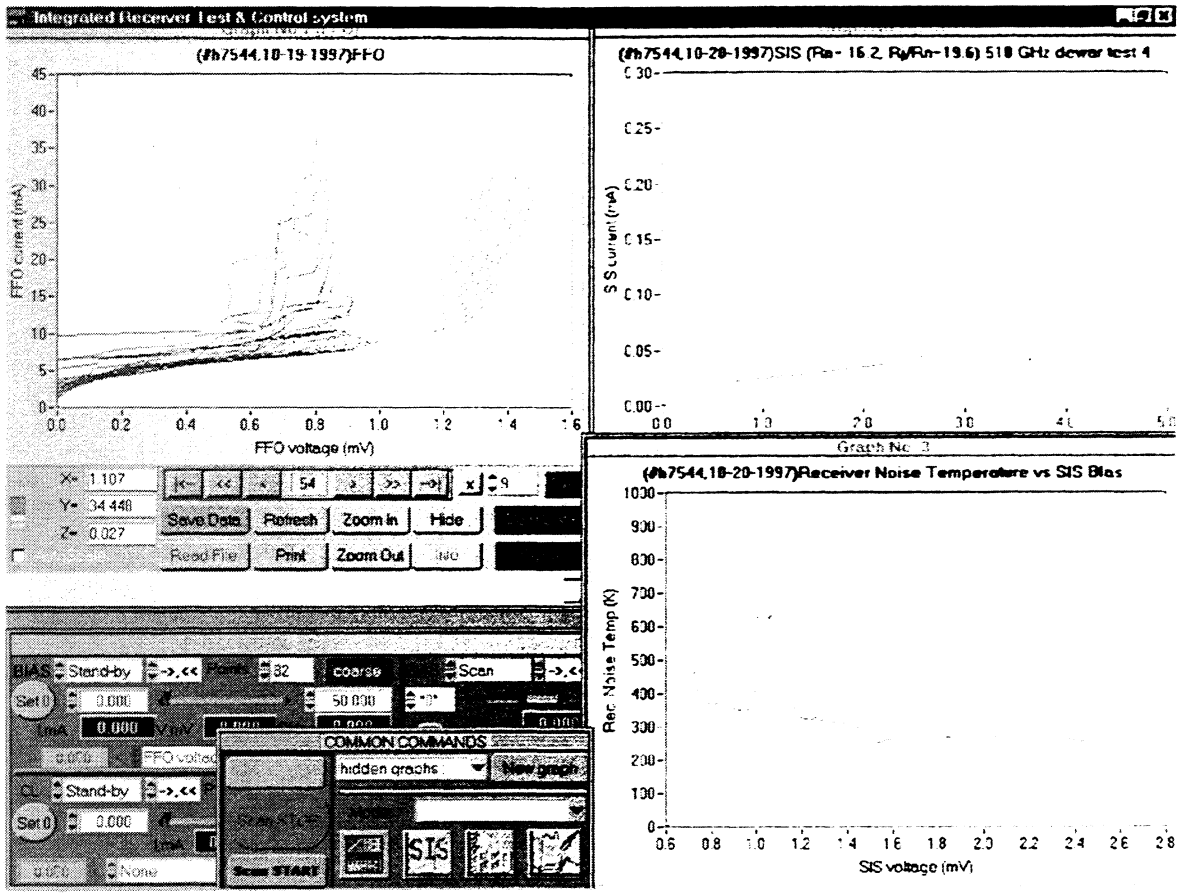

Fig. 7. Computer screen of "IRTECON" - Integrated Receiver Test & Control system: FFO IV-curves (top-left); unpumped and pumped IV-curves of SIS mixer (top-right); receiver noise temperature vs. mixer bias voltage (bottom-right); receiver control panels (bottom-left).

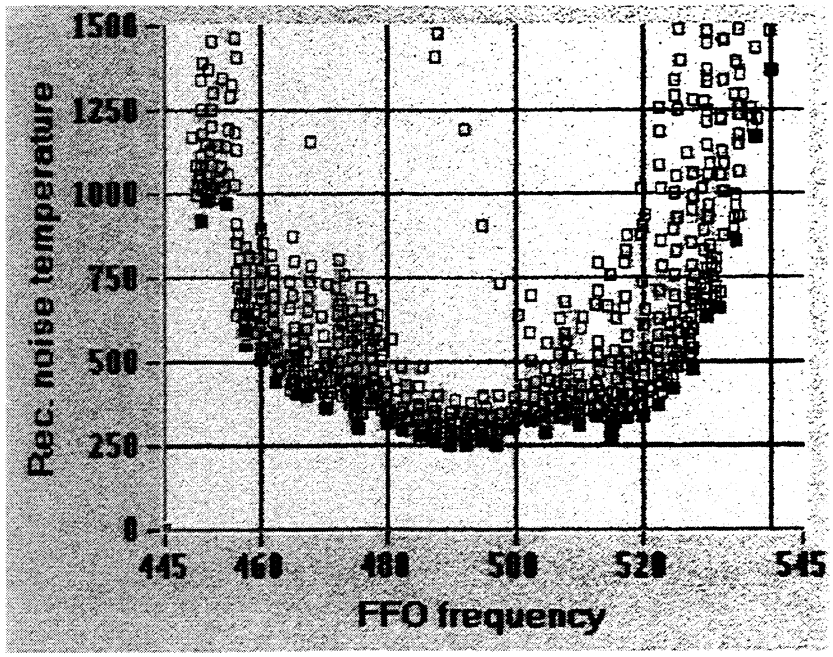

Fig. 8. Receiver noise temperature optimized by IRTECON (print-screen colored copy). The search process is presented by the light "bubbles" of intermediate (non-optimal) points.