WIDEBAND HIGH EFFICIENCY PLANAR DIODE DOUBLERS

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ABSTRACT

Very wideband heterodyne receiver systems are planned for many astronomical applications during the next 5-10 years extending up to 2.7 THz for space and airborne applications. At present the only means to provide sufficient local oscillator power for these submillimeter receivers is the Schottky varactor diode frequency multiplier. Using these devices in a chain of multipliers will require high output power with high efficiency in the early stages. This paper describes two new designs for planar varactor doublers which cover wide bandwidths with fixed tuning. A doubler for 150 GHz has 28% peak efficiency with a 3 dB bandwidth of 130-168 GHz. Room temperature output is 25-40 mW and the efficiency increases to a peak of 37% with ~55 mW output when cooled to 80 K. A similar doubler has been designed for 270-340 GHz.

INTRODUCTION

Very wideband heterodyne receiver systems are planned for many astronomical applications during the next 5-10 years. These include the SOFIA airborne observatory, the FIRST spacecraft, the Millimeter Array (MMA), the Submillimeter Array and numerous single antenna ground based observatories. Of these, the requirements for FIRST and SOFIA are the most demanding in terms of frequency coverage although the MMA will require by far the most receiver systems. At present, there are plans to include receiver systems on FIRST which may extend up to 2.7 THz, and on SOFIA up to 1.9 THz. Currently the only means of supplying this LO is the Schottky varactor frequency multiplier. All of these systems require the maximum bandwidth in all of their LO components, and it is desired that the LO components use planar technology wherever possible. This paper describes work on frequency doublers which demonstrate the potential to build wideband fixed tuned planar diode doublers centered at frequencies of 150 and 300 GHz, with sufficient power output to drive subsequent multiplier stages.

Planar diodes have shown the potential to replace whisker contacted diodes throughout the mm and submillimeter range, with performance in many types of devices which is as good or better than the whiskered diodes they replace. Planar diode arrays have been used in balanced doublers for 160 and 320 GHz [1,2], achieving very high power output and efficiencies at both frequencies. However, planar diodes include higher parasitic capacitance than is usually present in whiskered diodes, and this extra capacitance tends to limit the matching bandwidth that is possible with fixed tuning. Planar diodes also open up many additional circuit concepts that are not practical with whisker contacts, and this additional circuit flexibility in many cases more than compensates for the higher parasitics. The doublers described here have fixed tuned bandwidths which are larger than has been accomplished with whiskered designs, and are very efficient. They also are fairly easy to fabricate and are sufficiently robust that they can survive and operate at 77K.

CIRCUIT DESIGN

The doubler circuits are based on balanced designs using 4 diodes, which have been previously built for 160 and 300 GHz. Earlier models have achieved high efficiencies, with a maximum power output at 160 GHz of 63 mW, and a maximum output of 7.5 mW at 320 GHz. These results were obtained with a circuit originally designed for whiskered diodes, which could deliver high efficiencies only when tuned for narrow bandwidths [1,2,3]. The new 150 GHz doubler uses the same four diode arrays that were used previously (UVa batch SC6T6) and achieved an efficiency of 40% in doubling to 158 GHz, while the 300 GHz doubler uses the same diode arrays (UVa batch SB3T2) that were used in the previous 300 GHz design, and gave doubling efficiencies of 18% at 280 GHz and 13% at 320 GHz. However, the actual circuits have been extensively changed to maximize the bandwidth, and also to make machining and assembly as easy as possible. The configurations of these diodes are shown in Fig. 1.

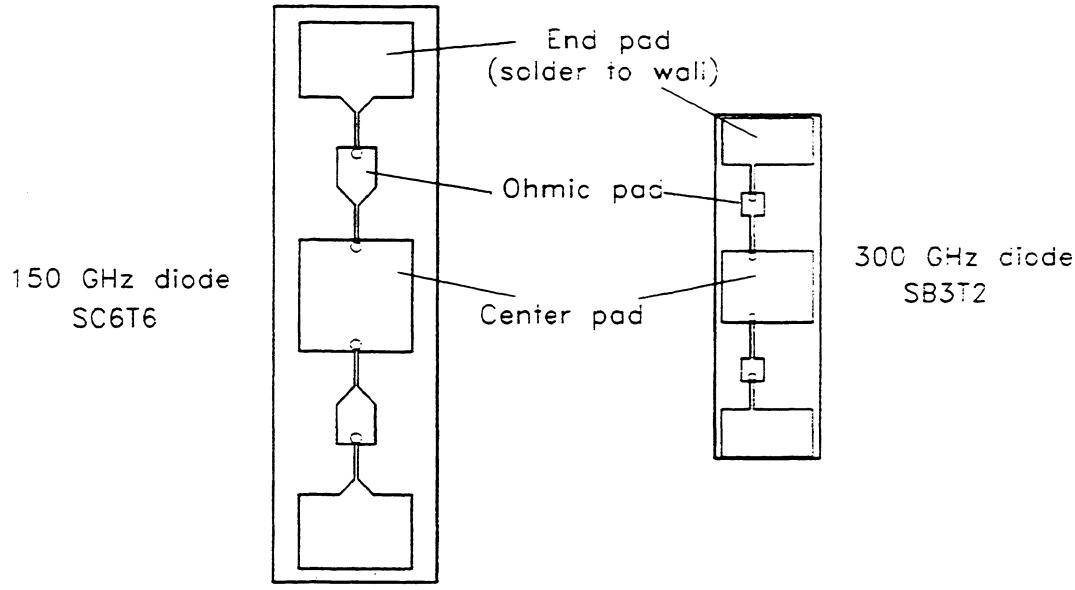

Figure 1. Planar varactor diodes used in the two doublers. The dimensions of the 150 GHz chip are 800×224 μm and those of the 300 GHz chip are 490×135 μm. Circles mark locations of the anodes.

The diodes were designed somewhat conservatively several years ago, and their relatively large pad sizes, particularly of the intermediate ohmic contacts, would appear to add serious parasitic capacitance. The overall lengths of the diodes were chosen to match the existing whisker contacted doubler designs and had nothing to do with optimized matching for a planar diode. It was believed at the time that the thickness of the GaAs substrate should also be minimized, since it increases the parasitics. However, the studies performed for this design show that the bandwidth of a complete doubler circuit is not critically dependent on any of these concerns, although all of them do have an effect on the final design. As an aid to the building of circuits which should be relatively easily fabricated, we assumed for this design that the GaAs thickness was 37 μm, although thinner diodes are available. For future layouts, we investigated modifications to the diodes which would improve the power balance between the anodes and also the modification of

the center pads to facilitate wideband matching. The goal of this work is ultimately to make a planar diode where much of the circuit would be incorporated onto the GaAs wafer, but this design is intended as a demonstration based on currently available diodes.

The circuit design is based entirely upon an HFSS [4] analysis of the planar diode as embedded in a waveguide. Experience has shown that this finite element simulator is sufficiently accurate that the results may be used for detailed circuit design without the need for prototyping or scale modeling. The diode is modeled including details of all of the metal pads, but with minimum fidelity to the areas around the anodes. The GaAs substrate is modeled as a uniform slab, without the region of high doping found under the metal pads, and with no channel under the fingers connecting the anode pads with the ohmic pads. The anodes are modeled as very short square coaxial lines which enter into the metal pads and then end. Ports are defined at the ends of these lines and are used as the diode terminals in later circuit simulation. All of the omitted detail makes the diode much easier to draw and very much quicker to simulate, and its effect on the final solution is too small to justify the effort to include it, given a number of more important parameters which are not so well known. All materials are assumed to be lossless, since the effect of losses is expected to be fairly small, and should have little effect on the design so long as inherently high loss geometries are avoided.

For simplicity, the circuit is split in half along the symmetry plane of the waveguide H-plane midline. At the input frequency the symmetry plane is a perfect electric conductor, and the waveguide is extended in both directions for a distance from the diode sufficient to attenuate higher modes, and is then ended with two ports. For the output, the symmetry plane is a magnetic conductor. The center pad of the diode connects to a metal strip extending to one of the waveguide ports, which forms the output TEM port, and the other waveguide port is not used. This method of analysis is essentially the same as that used in reference 5.

The S parameter files created with HFSS are imported into a linear simulator (HP MDS [6]) and the remainder of the circuit is initially designed using ideal circuit elements. In this simulation the diode itself is modeled as a linear element consisting of a series resistor and capacitor. The effective values of these elements were determined using a nonlinear simulation of the diode to be used, with the diode biased to the lowest voltage for which nearly optimum doubling efficiency is obtained. This bias minimizes the diode Q, which is found to be about 5.9 for the input circuit and 2.9 for the output circuit. The assumed zero bias junction capacitance of 45 fF used in the 150 GHz doubler gives an effective capacitance in the simulation of 22 fF, and an effective resistance of 16 Ω at midband. At the output frequency the capacitance is 19 fF while the midband resistance is 20 Ω.

The complete circuit for the 150 GHz doubler can be viewed with a number of simplifications in the following way. At the input the diode has significantly less than optimum inductance to resonate out the diode capacitance. As a result the diode load is quite capacitive, and this reactance is tuned out by placing the input backshort quite close to the diode. The long section of reduced height waveguide, which is necessary for TM11 mode suppression, also acts as an impedance transformer to the higher impedance waveguide. The remaining waveguide lengths were empirically chosen for the best wideband match, using series elements only, and may not represent the best input matching solution. More general forms of a matching circuit, including stubs or irises, may work better, but are more difficult to design. At the output frequency, the diode has too much inductance, and it is necessary to place a semi-lumped capacitor as close as possible to the center pad to tune it out. This capacitance is produced by the initial wide line,

which might work even better if wider, except that it is entirely within the input waveguide and would affect the input circuit. Following this element, the impedance is quite high and a quarter wave high impedance line consisting of a free standing 120 μm wide ribbon is used for matching. Finally, a half wave long mismatched (low impedance) line in coax is used to improve the broadband match. The transition to waveguide was initially designed to have no effect except as a mode transition, but the actual transition used was found to enhance the match after optimization. The output circuit was developed by working outward from the diode, adding circuit elements one at a time with each succeeding length and impedance optimized for the best match into a arbitrary resistive load. This approach ensures that the circuit has some logical structure that is likely to be close to a global optimum. In the end, all of the circuit elements were reoptimized, leading to some significant changes but the same basic concept.

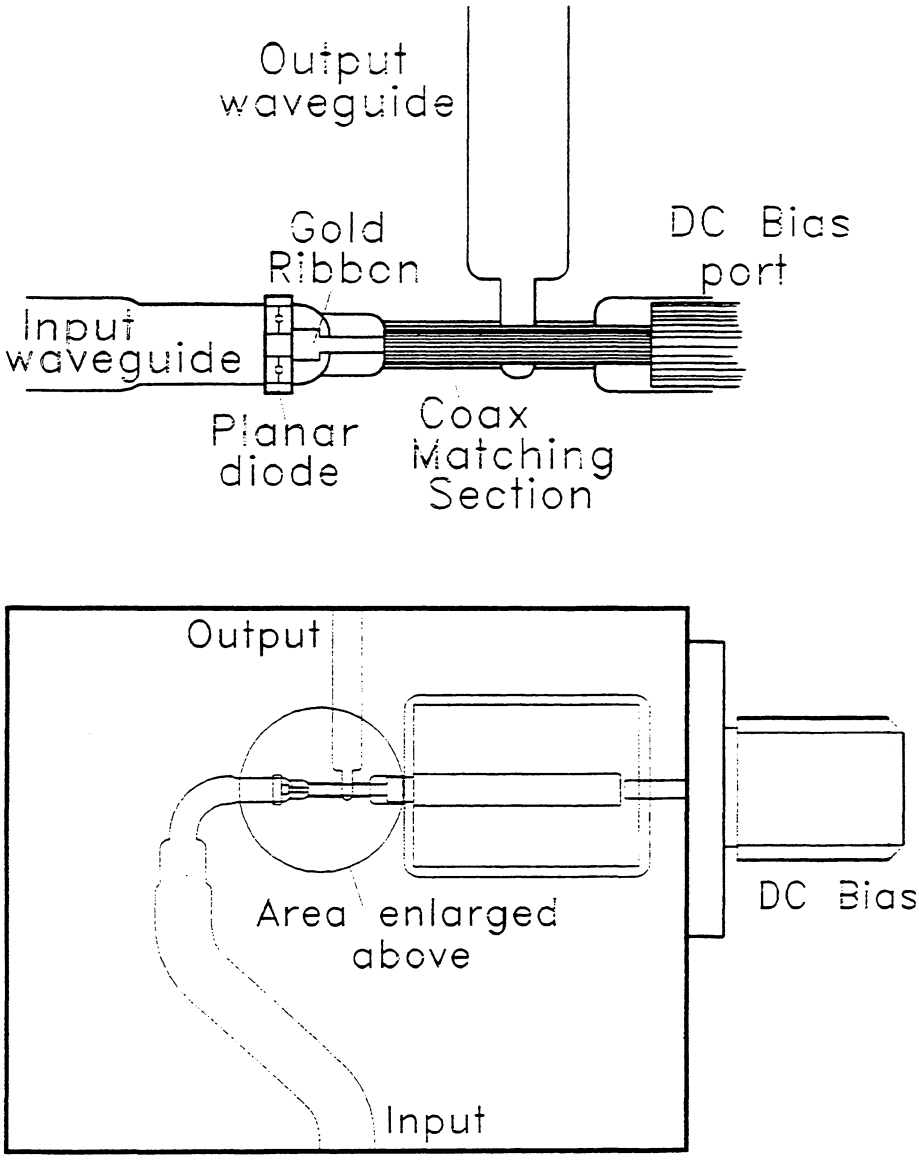

Figure 2. Internal detail (top) and overall view of 150 GHz balanced doubler.

The maximum practical bandwidth was desired, and a circuit was designed covering 135-170 GHz, with an input return loss of 7-8.5 dB over the full band and an output return loss of 9-10 dB. The resulting mismatch losses seemed to be acceptable, and predicted very flat performance over the band. The complete circuit that resulted is shown in Fig 2. The doubler is designed with the input and output directly in line, which requires bending the input waveguide tightly. To save length, one right angle bend occurs within one of the impedance matching sections. The overall size of the block is determined by flange dimensions, with a length of 1.5 cm to accomodate internal flange screws. In this design all circuit elements were constrained to be easily machined, with very high and low impedances eliminated, and both backshorts were machined in place with no provision for adjustment. The only free parameter remaining is the varactor bias voltage, and it is fairly tightly constrained (to 4-5 V per anode) in order for the diode to work well. The design is quite sensitive to varactor capacitance, and adjusting the bias voltage to compensate for errors is not very successful for more than a 10% variation. Diode thickness is also fairly critical as well, although ±12μm variation can be tolerated, particularly if the diode capacitance is changed to compensate.

The circuit assembly began by soldering in the coaxial pin which is attached to an insulating pad of an expansion matched circuit board [7]. Then a gold ribbon was cut to the correct shape to form both the low and high impedance sections, and this ribbon was soldered to the diode center pad. The diode and ribbon were laid into the block with the end of the ribbon resting in a cutout in the coaxial pin, and the two outside pads of the diode were soldered to the doubler block. The ribbon was attached to the pin by filling the cutout with conductive epoxy.

The 300 GHz doubler was designed in much the same way except that only the input circuit was designed for maximum bandwidth, with an expected matching band of 270-340 GHz. The output circuit was not designed for such a wide band except with backshort tuning, but is expected to cover the upper half of the band with a fixed setting. This doubler is still being machined so no results are available, but assuming this design is successful, a full bandwidth output circuit would be a straightforward next step. However, a problem with the diode design was noted in this process, which is that the power division between the pair of series diodes is poor in the output band, differing by over 1 dB at the highest frequencies, and is accompanied by a phase shift as well. These problems are particularly apparent if the GaAs thickness exceeds 37 μm, which is desired for the best strength of the chips. The amplitude and phase imbalance decrease the maximum efficiency of the chip and also may lead to unequal bias voltage division, further degrading the efficiency. This problem lead to a redesign of the diode chip for future fabrication, with the overall size scaled downward slightly, and the finger lengths adjusted. To facilitate a wideband output match, and also to increase the bonding or soldering area on the chip, the center pad was increased in area significantly. This should allow the output connection to the diode to be simply a high impedance line, while at the input these changes have little effect.

TEST RESULTS

Testing of the 150 GHz doubler was somewhat difficult because its bandwidth exceeds that of any source with sufficient power to drive it. This is a high power doubler and can not be properly tested with an input power below 100 mW. The plan for FIRST and other upcoming systems is to use MMIC power amplifiers to drive the complete LO multiplier chain, but these amplifiers at present are available at only 94 GHz with relatively narrow bandwidths. The purpose of these doublers are largely to demonstrate that such sources are indeed practical, and to justify the effort required to develop the power amplifiers, and other related components. At this time the

only alternative is to use several high power narrow band oscillators, and these limit test frequencies to only a few values. We used IMPATT oscillators at 75, 80 and 85 GHz with power outputs >250 mW, and Gunn oscillators with 80-130 mW output to cover the other parts of the band. Input powers for frequencies above 75 GHz, and all output powers, were calibrated with a well matched, stable calorimeter in WR10 waveguide [8] with an accuracy of 5%. At lower frequencies a commercial WR12 power sensor was assumed to be accurate.

Initially the doubler input and output return loss were measured with a small signal reflectometer to determine the general matching band. This type of measurement is useful because while the resistive part of the diode load under small signal conditions consists only of the series resistance of the diode, the varactor can be biased to simulate the actual large signal capacitance, and the reactive part of the match is much more critical. The resultant return loss curves show very poor match but the bandwidth of the match is representative of the actual large signal match. The measured input return loss showed a fairly flat return loss of 2-3 dB over the band of 65-85 GHz, with a varactor bias of 4.5 V, and a very poor match more than 3 GHz to either side of the band. The band could be shifted significantly through a change in bias, but no other bias produced a flat response. This method may be used to estimate the actual rf series resistance and the fit to this data is 4.5 Ω, as compared to a dc value of 1.7 Ω. At the output the match was measured from 135-170 GHz, and appeared to correspond to the design band, but the match was much better toward the low frequency end, and near 170 GHz was quite poor. These tests showed no narrow features, and served to justify the rather sparse sampling of the band under large signal pump.

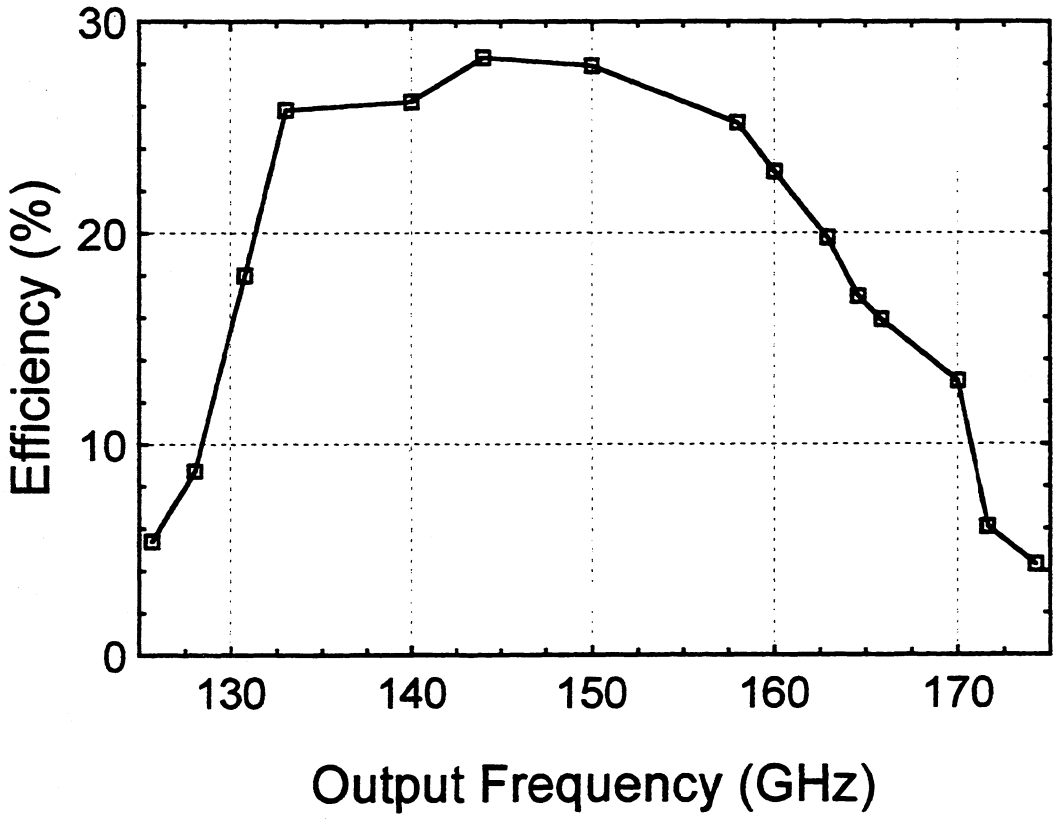

Figure 3. Maximum efficiency of the planar diode doubler. The input power for the best efficiency is 100-150 mW, with the maximum safe input power about 180 mW.

Large signal tests provided the data shown in Fig. 3 which shows the efficiency at optimum input power (or at the highest available power where input power is limited). At all frequencies, the maximum safe input power could be as large as 180 mW, with the efficiency slowly decreasing up to this power. The optimum bias voltage varies from 7 to 11 V across the band, depending on both power and frequency. Bias current is less than 1 mA for an input power below 120 mW. The operating band is shifted slightly lower than the design by about 5 GHz, while the total bandwidth meets expectations. The input return loss was measured at peak efficiency at 70, 75, 80 and 85 GHz and was found to be 6 dB ±0.2 dB at all frequencies. While this is less than predicted, the very flat match is as designed. The poorer match is probably due to interactions between the input and mismatched output impedances that were not considered in the design. Other contibutions may be small differences between the design and the actual circuit that was fabricated, and diode properties different from those of the design. It is not possible to directly measure the output match of a doubler, but it may be inferred from the improvement possible by adding an output tuner. With an input of 80 GHz, we added a Teflon quarter wavelength plug into the output waveguide and adjusted its position for the greatest output. The power increased by only 10%, indicating that the output return loss is ~10 dB, which is comparable to what is expected. The small signal measurements predict that the output match is better at lower frequencies, and this would appear to be the case based on the flat input match and the higher efficiencies at lower frequencies. Errors in the construction of the TEM line almost exclusively affect the output match, and can easily produce this response. There is no way to be certain of the power that a given varactor is capable of producing, since the dc series resistance is a poor predictor, but using the small signal fitted value of 4.5 Ω for R_s, an efficiency of 52% is predicted at 150 GHz. The best previous results with this batch of diodes gave 40% efficiency at 158 GHz output, with 120 mW input, and optimized input and output matching. The best results with this doubler, 28% at 150 GHz, if corrected for the input mismatch alone would give 37% efficiency, and the output loss due to the widebanding circuit is certain to be somewhat greater than that of the previous narrow band circuit, so it appears that this doubler's performance is consistent with expectations.

COOLED OPERATION

The increasing mobility of GaAs with decreasing temperature leads to a reduction of the series resistance and increased efficiency, as well as improved power handling. This makes cooling a multiplier chain an attractive option since each of its stages will improve [9], and at frequencies above 500 GHz the improvement in a single stage may be a factor of three. For this reason this doubler was tested at 77 K by cooling over a bath of liquid nitrogen. A single frequency of 150 GHz was measured, with an input power of 140 mW. The output power increased by a factor of 1.31, bringing the efficiency up to 36%, and the output power to 51 mW. This improvement is comparable to that measured previously in a similar doubler using whisker contacted varactors [10], and is consistent with the known mobility increase in GaAs. The improvement can not be due to a changing impedance match since the bias was unchanged, and the varactor capacitance is very nearly independent of temperature. It should be noted that the diode in this doubler is installed by soldering it in with 96C melting solder, so its operational temperature range is extremely wide. No special effort was made to ensure the survival of the diode over this temperature range except to use a thin gold ribbon as the contact to the center pad of the diode. The doubler block itself is brass with a thermal expansion coefficient very poorly matched to GaAs, but the differential expansion over the length of the diode is only ~2 μm, and the indium solder has considerable compliance.

CONCLUSIONS

A new frequency doubler has been built with 25% bandwidth to 3 dB points, centered at 150 GHz. The frequency response is flat to within 1 dB over 20% bandwidth and the minimum power output over this range is 40 mW, with ~25% efficiency The design, using planar diodes, is quite robust mechanically and operates with 30% higher power and efficiency when cooled to 77K. A second doubler for 300 GHz has been designed with comparable bandwidth, but is still under construction. Both doublers were designed with the aid of HFSS, and it appears that this computer program is sufficiently accurate to be the sole tool needed for the design of these devices without additional prototyping or modeling. This circuit is a hybrid construction of waveguide, coax, stripline and a free standing GaAs circuit, which is a bit complex to assemble. The TEM portion of the circuit could be redesigned as a microstrip circuit on quartz as has been done with a wideband 80 GHz doubler [11], which would simplify the assembly. Designing a diode specifically for a wideband circuit should improve the input and output match, and some work in this direction has been done in recent designs, particularly to help the output match. Doublers of these types could form the first stages of a multiplier chain to the THz range.

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