A 430.5 GHz Quasi–Optical HBV Frequency Tripler

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ABSTRACT *– In this paper, we present the design and the fabrication of a quasi–optical frequency tripler at 430.5 GHz. The multiplier consists in a 10×10 slot array, on a GaAs substrate, integrated with Hetero–structure Barrier Varactors. A specialized CAD tool, based on the infinite array approximation, has been developed for the design of the antenna and for the optimization of the embedding system (external filters and matching slabs).*

1. Introduction

Quasi–optical frequency multipliers in the millimeter and submillimeter wave range have been recently investigated as an alternative to the conventional waveguide devices [1, 2]. The multiplier (Fig. 1) consists of a planar antenna array integrated with non–linear devices, embedded in a quasi–optical gaussian system together with input/output filters and dielectric matching slabs [3, 4].

For an overall optimized design, two different components have to be carefully accounted for [5]: *i)* the non–linear device should be fed with a sufficient pump power, and connected to an impedance that maximizes the conversion efficiency; *ii)* the antenna and the embedding system should provide the device with the required impedance, and, at the same time, fulfil the best power coupling with the quasi–optical gaussian beam.

In this paper we discuss the use of Hetero–structure Barrier Varactors (HBVs) for the design of a frequency tripler at 430.5 GHz. We present the physical structure of the HBV, the measured $C_j(v)$ and $I_j(v)$ characteristics and the estimation of the efficiency performance and of the optimal embedding impedance, using an algorithm based on the Harmonic Balance technique.

With regards to the analysis of planar antennas we have developed a specialized code [4], based on the simplifying approximation of an infinite array, which permits to take into account the effect of external filters and matching slabs. Using this code, we designed a 10×10 slot antenna array, which allows to closely approach the estimated optimal impedance. We discuss the tuning of the embedding system and its effect on the conversion performance.

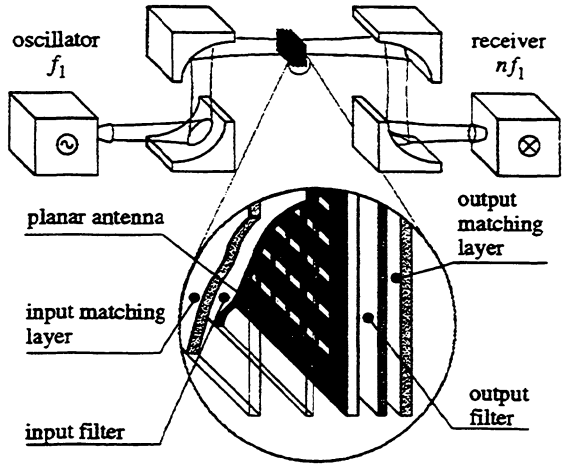

Fig. 1 – Schematic of a quasi–optical frequency multiplier, embedded in a gaussian system.

2. DEVICE ANALYSIS

In the recent years, the Hetero–structure Barrier Varactors have been largely investigated as promising devices for efficient high frequency triplers [6, 7]. In fact, these varactor devices require less design complexity compared to Schottky diode tripler circuits. This is attributed to the device characteristics, leading to the formation of only odd harmonics and hence no idler circuits are required for the even harmonics. Furthermore, since the HBV exhibits the highest non–linearity around zero bias voltage, no DC bias circuitry is required. Moreover, multiple–barrier HBV has a large degree of design flexibility in barrier number, layer thickness and doping profile; it allows for "tailoring" the device characteristics which are particularly suitable to a specific application.

In this section we consider a multiple–barrier HBV, which has been fabricated and tested at the Darmstadt University of Technology. The layered wafer structure is shown in Fig. 2: a total of four $GaAs/Al_{0.7}Ga_{0.3}As$ hetero–structure barriers have been used in the device (see the SEM photograph in Fig. 3*a*). The diameter of the structure amounts to approx. 15 μm.

The device characteristics have been measured, using the test structure shown in the photo of Fig. 3*b*. We have obtained the quasi–static $C_j(v)$ and $I_j(v)$ curves (Fig. 4) by fitting the measurement results. A series resistance $R_S = 5\ \Omega$ was measured.

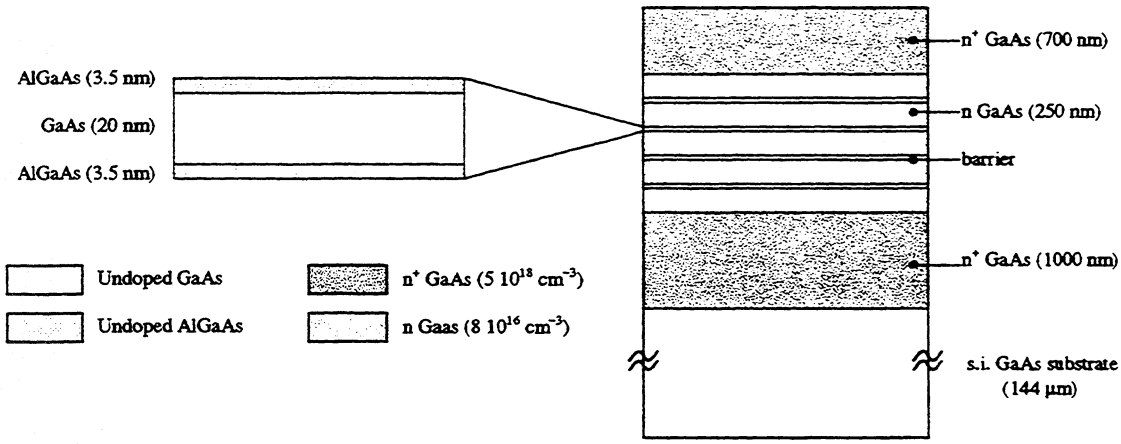

Fig. 2 – Structure of the HBV fabricated at the Darmstadt University of Technology.

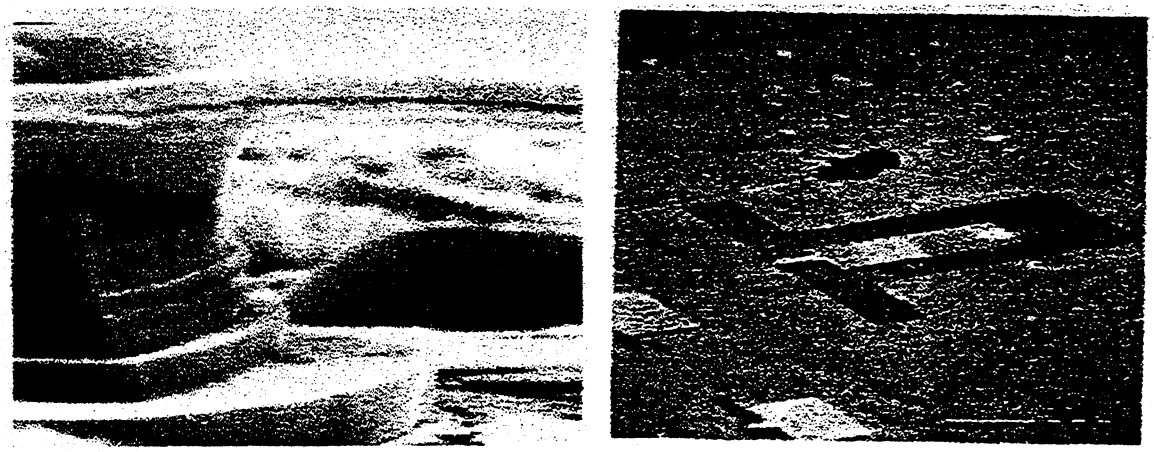

Fig. 3 – SEM photographs of the four–barrier HBV (left) and of the test structure (right).

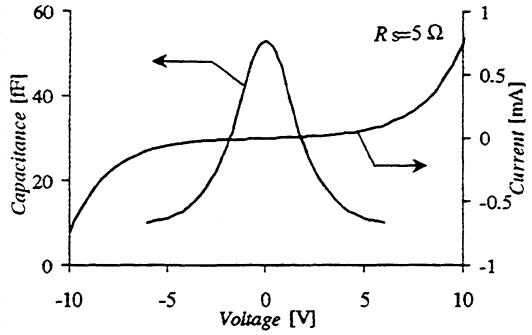

Fig. 4 – $C_j(v)$ and $I_j(v)$ characteristics of the HBV, deduced from measurements.

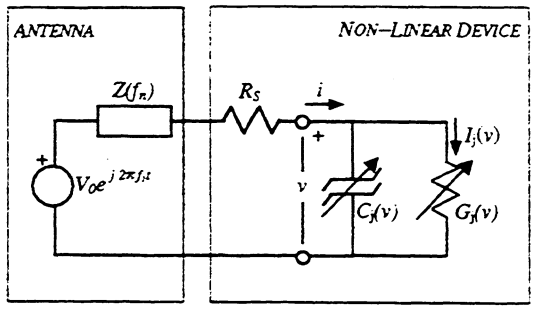

Fig. 5 – Equivalent circuit representing the elementary cell of the array.

For the simulations, we have used the equivalent circuit of Fig. 5, where V_0 represents the open circuit voltage of the (receiving) antenna at the fundamental frequency f_1, and $Z(f_n)$ is the input antenna impedance at f_n, for all the frequencies of interest. The total device current as a function of the voltage $v(t)$ is given by

$$i(v)=C_j(v)\frac{dv}{dt}+I_j(v)$$

The numerical analysis of the non–linear circuit is based on the Harmonic Balance technique. We have developed an algorithm, which is a modified version of the one presented in [8]. This algorithm resulted in a more robust routine for the analysis of circuits including HBVs.

The input data for the circuit analysis are the device characteristics and the available pump power P_0 at the device terminals at f_1. While the behavior of the non–linear device mainly depends on the technological process, the power P_0 is related to the total power P_{TOT} carried by the gaussian beam and to the antenna geometry. For a given non–linear device (modeled through $C_j(v)$, $I_j(v)$ and R_S), and an available power P_0, our code is able to find the optimal embedding impedance $Z(f_n)$ at the frequencies of interest.

An extensive use of this code allowed us for deeply investigating the HBV behavior for the operation in a frequency tripler at 430.5 GHz. We have calculated the device conversion efficiency versus the power P_0 and versus the impedance $Z(f_n)$.

The first result is that the value of P_0 has a strong impact on the maximum conversion efficiency (obtained with the optimal impedance at all the harmonic frequencies): Fig. 6 shows that the device conversion efficiency is quite poor at low pump power levels. Furthermore, different impedance values are required, in order to maximize the conversion efficiency at different pump power levels (Fig. 7).

If the embedding impedance is not the required one, the performance of the device deteriorates. We found that the impedance at the fundamental frequency is the most critical, while the efficiency has a minor sensitivity versus the impedance at the output harmonic. We experienced that the impedance at higher harmonics has a negligible effect on the efficiency up to large power levels.

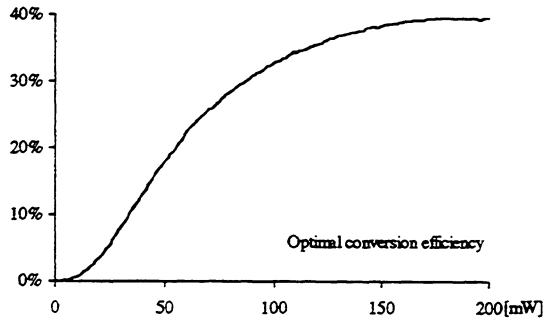

Fig. 6 – Optimal conversion efficiency of the HBV versus available pump power at the fundamental frequency (f_1=143.5 GHz).

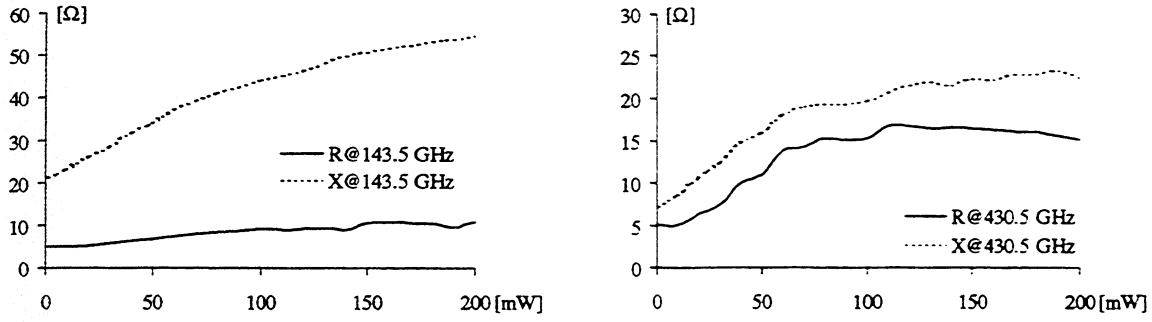

Fig. 7 – Optimal embedding impedance of HBV versus P_0 at the f_1 (left) and at $3f_1$(right).

These considerations lead to the conclusion that the embedding circuit (*i.e.* the antenna, in our case) should be designed, carefully considering the total available pump power of the source P_{TOT} and the number of elements in the antenna array. In other words, since we consider the approximation of the infinite array, the estimation of the available power per unit cell P_0 is required. On the other hand, the number of elements of the array should be large enough to allow for a good power coupling with the quasi–optical gaussian beam and, at the same time, sufficiently limited to ensure an adequate power level to each non–linear device.

These constraints determine the array size, and consequently the available P_0, once the total power P_{TOT} is fixed.

In our design, the source at 143.5 GHz is a BWO, which can provide the system with about P_{TOT}=400 mW. We estimated that the most satisfactory number of elements of the array is 100. As a consequence, the (average) P_0 is 4 mW, at the best. With this power level, the maximum conversion efficiency which can be achieved is approx. 0.1%. The required impedance values are

$$Z_{OPT}(f_1) = 5.0 + j21.7\ [\Omega]$$
$$Z_{OPT}(3f_1) = 5.0 + j7.4\ [\Omega]$$

where f_1=143.5 GHz is the fundamental frequency of the system.

In the following section, we will show how these impedance values can be obtained, by means of a careful design of the antenna and the embedding system.

3. ANTENNA ANALYSIS

In this section we describe the design of the antenna array and of the embedding system, which provide the non–linear device with the required impedance at all the harmonic frequencies. In our design, the antenna consists in a 10×10 slot array on a GaAs substrate.

For the analysis of layered structures, we have developed a novel specialized computer code, which is able to simulate the non–linear device, the planar antenna and the layered embedding structure as a whole. The analysis of the multiplier is performed making the simplifying approximations of an infinite array excited by an uniform plane wave incident from the broadside direction.

Under these assumptions, the study of the structure reduces to the analysis of the unit cell of the array, which, in turn, leads to the equivalent circuit of Fig. 5. The aperture, as seen by the non–linear device, is represented by an equivalent generator at f_1 and by equivalent loads $Z(f_2)$, $Z(f_3)$, ... at the harmonic frequencies f_2, f_3, ... Either the open circuit voltage V_0 and the impedances $Z(f_n)$ are deduced from a full–wave analysis, based on the Method of the Moments (MoM) in the spectral domain, of the multi–layered structure embedding the antenna at frequencies $f_1, f_2, \ldots$. The effect of the filters is taken into account by their plane–wave reflection / transmission coefficients at the harmonic frequencies. The number and the type of the dielectric layers, the shape, the size and the separations of the apertures

and the frequency response of the filters can be given arbitrarily. Once the equivalent circuit has been determined, the frequency spectrum of the current flowing in each non-linear device is found by the Harmonic Balance method. These results permit to find the scattered field at the fundamental frequency and at the harmonic of interest, thus leading to the calculation of the overall conversion efficiency of the multiplier.

A careful dimensioning of the whole structure allows to obtain an efficiency very close to the maximum one, that can be deduced from circuit analysis, as described in the previous section.

To this aim, we have integrated the analysis code into an optimization routine (Fig. 8). Using this routine, we have optimized the aperture dimensions, the array geometry, the characteristics and the position of the dielectric matching slabs, together with the positions of the input and output filters, in order to approach the maximum conversion efficiency.

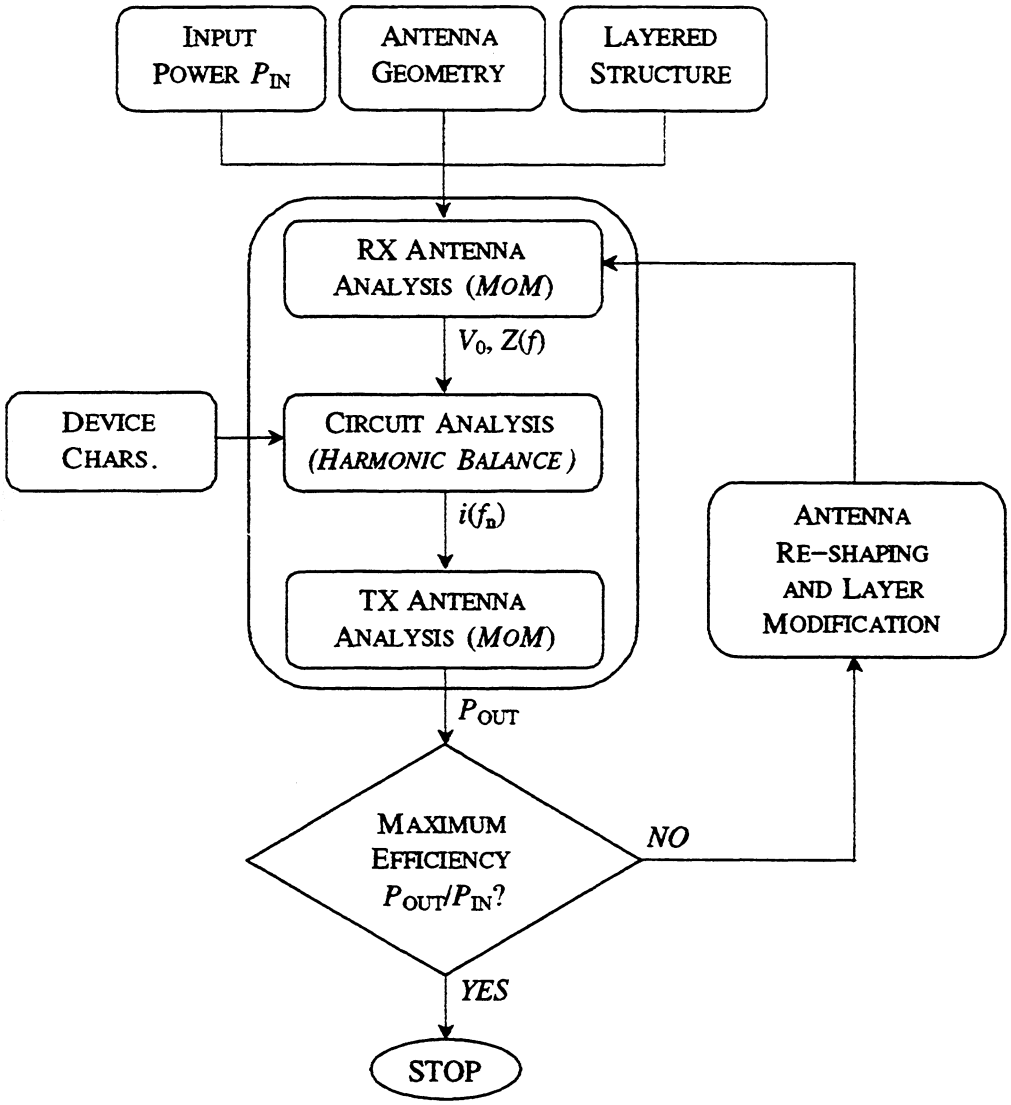

Fig. 8 – Block diagram of the computer code for the analysis and the optimization of the multiplier.

Fig. 9 – Photograph of the 10×10 slot array

In our design, we used a 144 μm thick GaAs substrate (ε_r=12.9, tan δ_E=0.002); as shown in [3], the chosen thickness is effective against the substrate wave propagation.
The optimal dimension of the slot antenna resulted 175×20 μm^2, while the 10×10 array element spacing was 300 μm in both directions. The tripler chip has been fabricated at the Darmstadt University of Technology (see Fig. 9)
From the simulations resulted that the input matching structure should consist of two alumina slabs, with a relative dielectric permittivity ε_r=9 and a thickness of 170 μm; the optimal simulated spacing was 5.54 mm. Similarly, the output matching structure consists of two alumina slabs, with a thickness of 56.7 μm, with a spacing of 4.94 mm. For the input and output filters (band–pass at 143.5 GHz and 430.5 GHz, respectively) we considered free–standing metal layers, with a power transmission coefficient of approx. 95%. The complete measurement setup is sketched in Fig. 10.
With the layer spacing reported in the caption of Fig. 10, we found the following impedance values:

$$Z(f_1) = 4.7 + j27.0\,[\Omega]$$
$$Z(3f_1) = 5.3 + j6.5\,[\Omega]$$

These values are very close to the optimal ones, reported in the previous section. With these impedance values, the estimated efficiency closely approaches the maximum theoretical efficiency of the HBV (see Fig. 6).
Performing the optimization, we found that the most important parameters that must be controlled to maximize the efficiency are the position of the input matching layers and the one of the output filter.
On the basis of these simulations, the measurement setup has been prepared. Its actual optimization is still under way: this is a quite critical and time consuming task, due to the low output power.

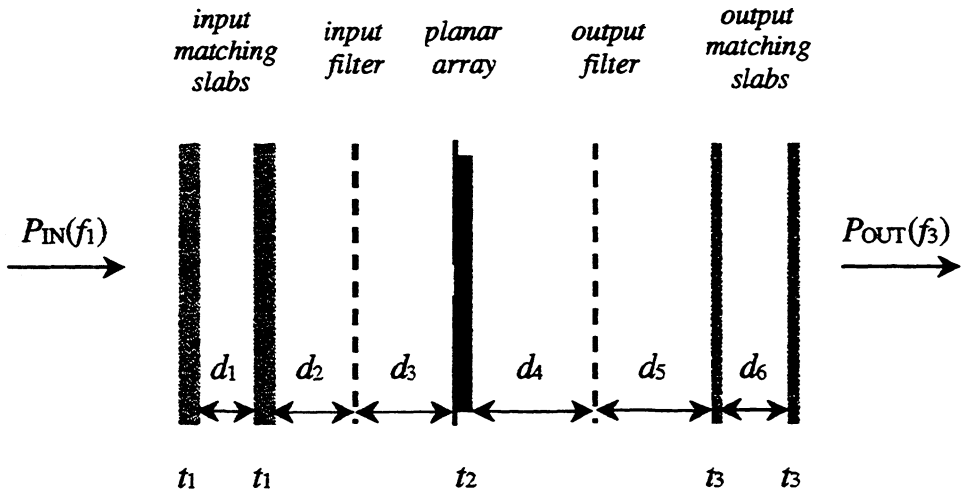

Fig. 10 – Optimized setup for the multiplier embedding system. Dimensions: d_1=5.54 mm, d_2=4.56 mm, d_3=4.87 mm, d_4=5.84 mm, d_5=4.39 mm, d_6=4.94 mm, t_1=170 μm, t_2=144 μm, t_3=56.7 μm.

4. FUTURE DEVELOPMENTS

The main factor which limits the conversion performance of the presented HBV frequency tripler is the low power P_0 delivered to each non–linear device. In order to overcome this drawback, the obvious solution could be the use of a more powerful source. Such a solution, nevertheless, leads to cumbersome systems, which are not suitable to space–borne applications.

An other possibility is represented by the integration of non–linear devices, which exhibit a satisfactory conversion efficiency at a low power level. It is interesting to observe that different devices, with the same cutoff frequency (defined like in [9]) but with different $C_j(v)$ characteristic, may have very different conversion efficiency at low power levels.

In this section, we present a comparison of the conversion performance of different HBVs, to be used in a frequency tripler at 430.5 GHz. The device named HBV#1 is the one fabricated at the Darmstadt University of Technology, and previously discussed. The characteristics of HBV#2 and HBV#3 are derived from theoretical considerations, progressively reducing the area of the devices. In a first–order approximation, a reduction of the device area leads to a proportional decrease of the junction capacitance C_j and a corresponding increase of the series resistance R_S (Fig. 11).

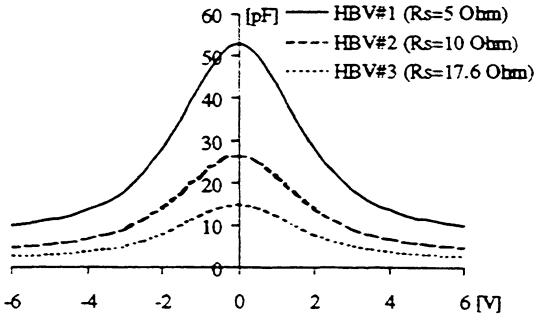

Fig. 11 – Capacitance vs. voltage characteristic of different HBVs.

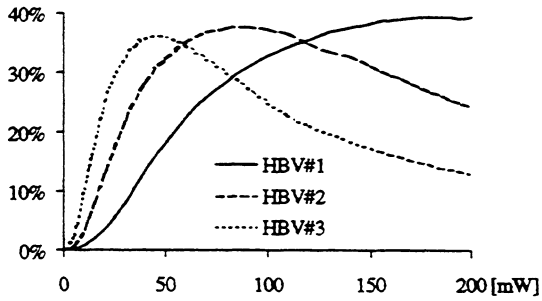

Fig. 12 – Maximum conversion efficiency versus P_0 for different HBVs.

Fig. 12 shows the maximum conversion efficiency for the three HBVs versus P_0.

It is apparent that reduced area devices are to be used when P_0 is small. Unfortunately, up to now, technological limitations prevented us from fabricating, in a reliable and repetitive way, four–barrier HBVs with diameter smaller than 15 μm.

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