QUARTZ-BASED GaAs SCHOTTKY DIODES — LIFETIME AND FAILURE ANALYSIS

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ABSTRACT

A previously reported technology that allows for the fabrication of semiconductor devices based on quartz (or other dissimilar substrates) has resulted in state-of-the-art mixer performance at frequencies up to 640 GHz. The present work will discuss the procedure that has been used to quantify the reliability of such devices for space-borne missions. A number of accelerated lifetime tests have been conducted. It is concluded that these devices exhibit lifetimes that are consistent with other GaAs devices for space applications. Our accelerated lifetime data, analyzed with the Arrhenius-lognormal model, predict a room temperature MTTF on the order of 10^{10} hours, a value that is comparable to conventional high-frequency planar Schottky diodes. This result demonstrates that the use of an appropriate epoxy to obtain GaAs devices on quartz substrates does not reduce the lifetime of the devices.

I. INTRODUCTION

For very high frequency applications, quartz is a desirable substrate material, because it has lower loss and lower dielectric constant than GaAs. One possible method of obtaining semiconductor devices on quartz substrates is to use a bonding agent such as epoxy. A technique, named QUID (for Quartz-substrate Upside-down Integrated Device), has been developed to produce GaAs Schottky diodes on quartz substrates for millimeter- and submillimeter-wave applications [1,2]. With this technique, planar GaAs Schottky diodes are mounted upside-down onto quartz substrates operating as low noise mixers at frequencies up to 640 GHz. After successful performance demonstration, it is now desirable to study the lifetime and failure mechanisms associated with such structures.

Figure 1 shows a cross-sectional schematic of the QUID structure. The anode of the Schottky diode is made with a T-anode structure similar to the T-gate technology used for HEMTs. Two such diodes are arranged in an antiparallel configuration to provide subharmonic mixing. Following the integration of the diode with the RF microstrip filter circuitry, the entire circuit is bonded upside-down onto a 50 micron thick quartz substrate with a heat-cured epoxy [3]. This bonding agent also fills the air gap under the fingers, which may affect the device's reliability. Finally, all of the GaAs substrate is etched except for two small mesas around the active region with the two planar diodes. The thin 4000Å AlGaAs layer that was used as the etch

stop layer can be either removed or left in place without affecting RF performance. However, it does have reliability consequences which will be discussed later.

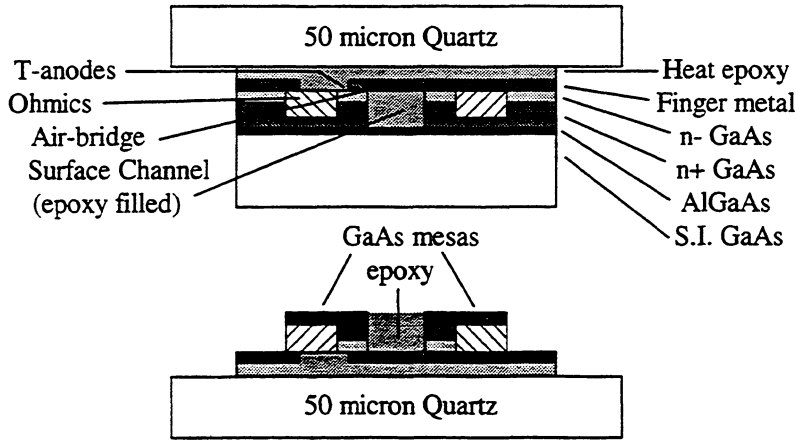

Figure 1: Cross-sectional schematic of the starting and ending point of the QUID process. (not to scale)

II. ACCELERATED LIFETIME TESTING

The accelerated lifetime tests are based on the Arrhenius-lognormal model which is widely used for GaAs MMICs [4]. It states that the failure times for a batch of devices have a lognormal distribution about the median time to failure (the time for 50% of the devices to fail). This median time to failure, in turn, is related to absolute temperature by

$$t=t_0 \exp(E_a/kT),$$

where t is the median time to failure (MTTF), E_a is the activation energy measured in eV, k is Boltzmann's constant, and T is the absolute temperature. A number of studies have been done in the past to determine lifetimes of Schottky diodes. In particular, two studies that investigate the lifetime of high frequency planar diodes made at the University of Virginia have been reported [5,6]. An important goal of this study is to determine whether the QUID process degrades the lifetime of the devices compared to conventional high frequency planar diodes.

A. Failure Criteria and Test Procedure

In defining what constitutes a failure for the QUID structures, we use a failure criteria based on the DC I-V characteristics that may help us predict the device's performance degradation at RF. These devices are being developed for a particular application, so the failure criteria is based on a quantitative degradation in the noise temperature of the subharmonic mixer. Using the procedure outlined in [7], a number of simulations were carried out with a 640 GHz subharmonic mixer. The pad-to-pad and pad-to-finger capacitance of the device were assumed to

be fixed at 4 and 2 fF, respectively [7]. A nominal device was taken to have series resistance of 6 ohms, ideality factor of 1.2 and knee voltage (voltage where current is equal to 1 μA) of 512 mV. These three parameters are then varied one by one, and the resulting mixer noise temperature is compared to the noise temperature obtainable from the nominal device. The simulation results are shown in Table 1.

% change in mixer	% change in η			% change in R_s					% change in V_0			
	4	17	21	8	17	25	33	50	-4	-10	-14	-39
T_{mix}	2.7	14.6	20.1	5.5	11.3	17.0	22.8	34.1	1.0	2.0	4.0	15.0
L_s	0.0	0.4	0.5	1.8	3.4	5.2	6.8	9.9	0.5	1.3	2.0	6.5

Table 1: Results of harmonic balance simulation of mixer RF performance, as a function of changes in η, R_s, and V_0.

It is further assumed that a 15% degradation in the noise temperature of the mixer will constitute failure. Based on this information, an anode is considered to have failed if any of the following conditions are met:

1. ideality factor, η, changes by more than 15%,
2. series resistance, R_s, changes by more than 20%,
3. knee voltage, V_0 (voltage where current is 1 μA), changes by more than 40%,
4. a combination of changes in η, R_s, V_0 results in mixer noise temperature degrading by more than 15%.

The baseline value for each of these three parameters is calculated by averaging a diode's parameter during the first few measurements at the test temperature. This is to smooth out some of the noise due to measuring errors. Further reduction of noise in the acquired data is done by local averaging of the diode's properties over time. For each device, when the device parameters meet the failure criteria, the time since the beginning of the test temperature period is recorded. The failure times are plotted on a lognormal graph paper, and an apparent linear regression line is constructed to determine the median time to failure and the standard deviation at each temperature. Infant mortalities, or devices that failed significantly earlier than the rest of the sample, were not considered in the apparent linear fit.

B. Experimental Setup

An automated system was designed to conduct the accelerated lifetime tests [8]. The QUID structures were placed unbiased in a nitrogen-purged high-temperature oven for an extended period of time. The temperature was slowly increased from room temperature with the devices already mounted inside the oven. Device I-V characteristics were monitored in situ, once every hour, with a computer-controlled data-acquisition system. Nominally fifteen devices, or thirty anodes, were tested at each temperature. The temperature range used extends from 170°C to 240°C. The devices were mounted onto ceramic chip carriers using two-part epoxy and gold wire bonds (Figure 2), and subsequently placed in a high-temperature wiring fixture designed to withstand at least 250°C. Recently we have developed a macor-based mounting that does not involve the use of solder and can withstand temperatures up to 340°C (Figure 3).

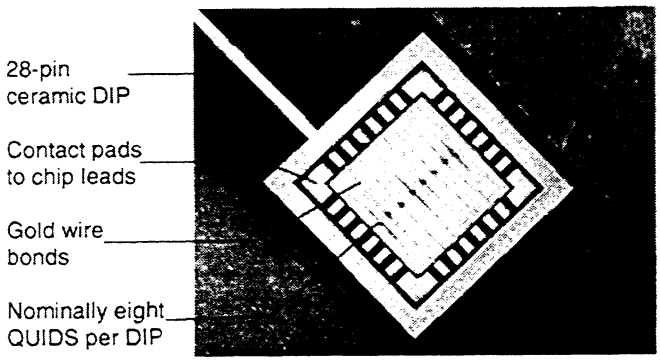

Figure 2: Devices mounted on ceramic chip carrier for thermal lifetime tests.

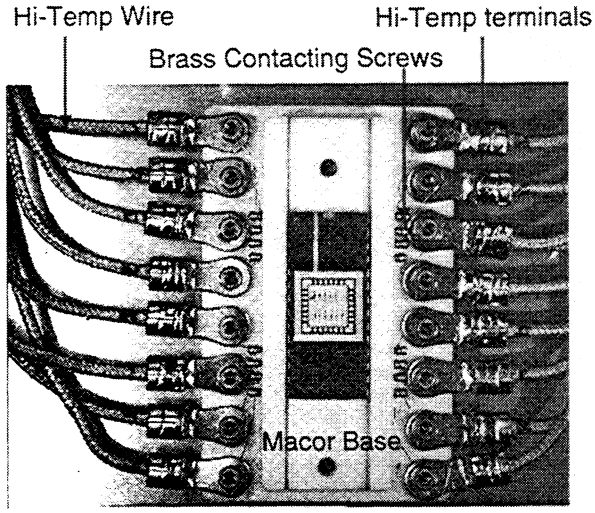

Figure 3: Macor-based solder-less mounting fixture rated to 340°C.

III. EFFECT OF PROCESSING VARIATIONS ON DEVICE LIFETIME

A nominal QUID structure and three processing variations, as shown in Figure 4, were investigated. Their effects on device lifetime are detailed below.

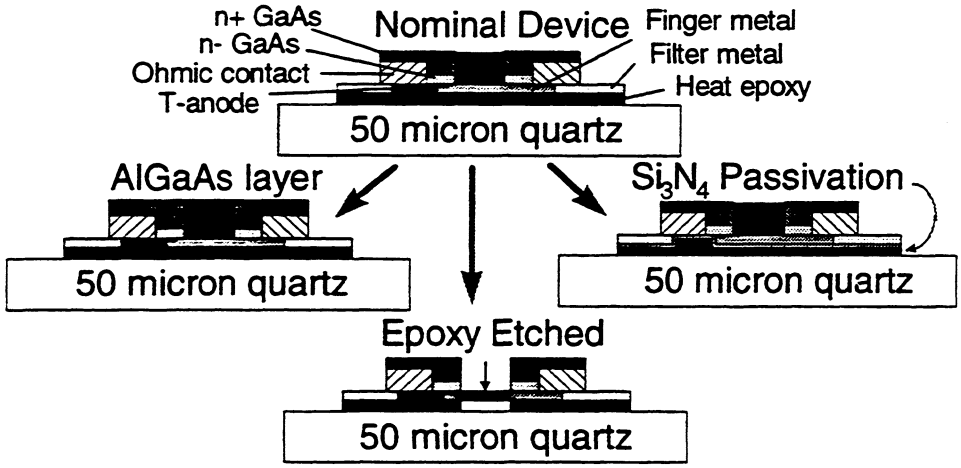

Figure 4: Device Processing Variations: (1) AlGaAs etch-stop layer, (2) epoxy-etched channel, (3) Si_3N_4 passivation. (Figures not drawn to scale)

A. Effect of the AlGaAs etch stop layer

The AlGaAs etch-stop layer, with 55% aluminum mole fraction, is a critical component that enables uniform back etching of the substrate. In earlier devices, the AlGaAs layer was left intact in order to reduce one processing step and to reduce yield loss during dicing. However, once RF measurement results made it clear that the epoxy within the channel would have to be etched, it became necessary to etch the AlGaAs layer. To investigate if this would have an effect

on the device reliability, a number of lifetime tests were conducted both on devices with the AlGaAs and devices without the AlGaAs. The results are shown in Figure 5.

Interestingly, some of the devices with the AlGaAs layer used in the tests failed catastrophically while no device without the AlGaAs layer failed catastrophically. A catastrophic failure is defined as one in which the device meets the failure criteria abruptly rather than gradually. The data shown in Figure 5 includes the devices that failed catastrophically. However, if that data is removed from the test sample, then both types of devices have identical activation energies (that is, the lines are parallel) with the AlGaAs devices having a slightly higher MTTF.

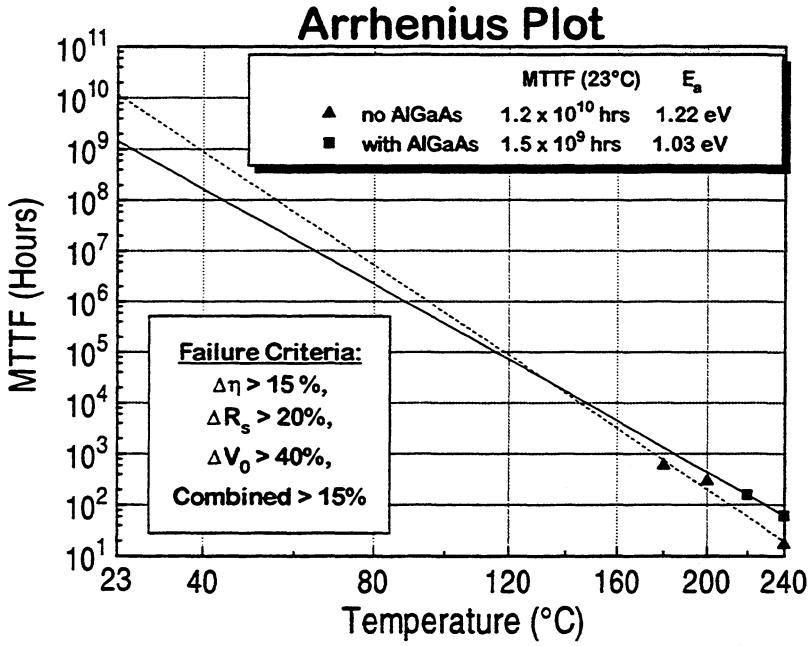

Figure 5: Arrhenius Plot for devices with and without AlGaAs etch-stop layer.

An attempt was made to determine the mechanisms that were responsible for device failures. Following the accelerated lifetime test, devices were inspected with an optical microscope and a scanning electron microscope (SEM). The SEM analysis showed that there are at least two types of failure mechanisms, and that they are related to different failure paths. Figure 6 shows a device with AlGaAs that failed catastrophically, and Figure 7 shows a device without AlGaAs that failed gradually (that is, its I-V parameters slowly degraded before it met the failure criteria).

Several observations can be made about Figure 6. The 4000Å AlGaAs layer is prone to severe cracking. This particular device experienced a catastrophic failure, and further inspection of the top finger revealed that it was broken near the right end. The high-temperature stress possibly caused a structural stress buildup before it was released in the form of a catastrophic crack. Figure 7 shows a device with no AlGaAs layer, and this device does not have signs of cracking. Currently we are investigating other non-structural failure mechanisms that might be responsible for the devices that failed with gradual degradation.

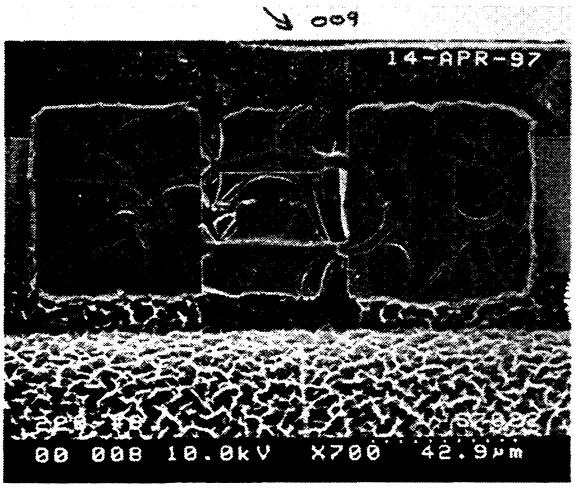

Figure 6: SEM photo of a device with AlGaAs etch-stop layer after 220°C lifetime test. This device failed catastrophically, and there is a break near the right end of the top finger.

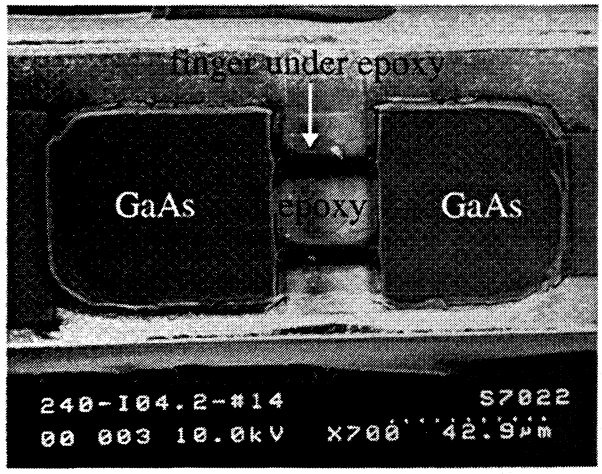

Figure 7: SEM photo of a device without AlGaAs layer, after 240°C lifetime test. This device degraded gradually, and shows no sign of cracks in the GaAs mesas.

B. Effect of epoxy inside the channel

During the procedure for bonding GaAs onto a quartz substrate, an epoxy layer is applied to the wafer, and fills the channel region underneath the metal fingers. Removing this epoxy with an oxygen plasma etch causes a 20% reduction in parasitic capacitance, and enhances the mixer RF performance. To investigate the effect of the epoxy-etch on device reliability, lifetime tests were performed on a batch of epoxy-etched devices and results compared to those without the epoxy-etch. Both batches have the AlGaAs layer already removed. Lifetime tests were conducted at three different temperatures for each type of device. The Arrhenius plots are shown in Figure 8.

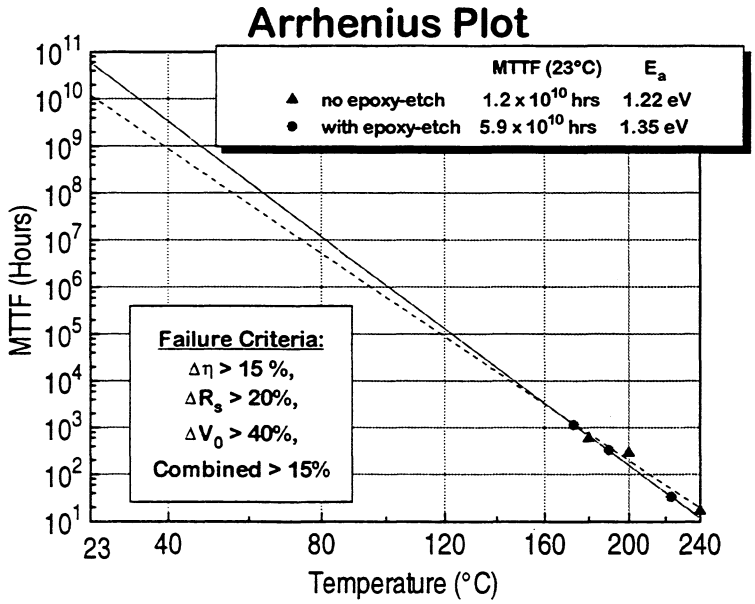

Figure 8: Arrhenius Plot for devices with and without epoxy-etch procedure.

The data collected in these tests fall on nearly the same Arrhenius line. The extrapolated MTTF values at 80°C are equal to within a factor of two, and even at room temperature, they differ by less than an order of magnitude. The activation energies differ by 0.13eV, or about 10%.

Figures 9 and 10 show the images of the two types of devices under a SEM. Both of these devices failed gracefully, although the epoxy in the channel region for Figure 9 seems to have a crack parallel to the fingers. We have already seen a correlation between cracks perpendicular to the fingers and catastrophic failures, but it appears that devices are less affected by cracks parallel to the fingers. Removing the epoxy completely from the channel, however, would reduce the risk of any epoxy cracks around the finger pair, thus reducing the risk of a catastrophic failure due to a mechanical break. This is shown in Figure 10, where the fingers are visible after the epoxy has been etched away.

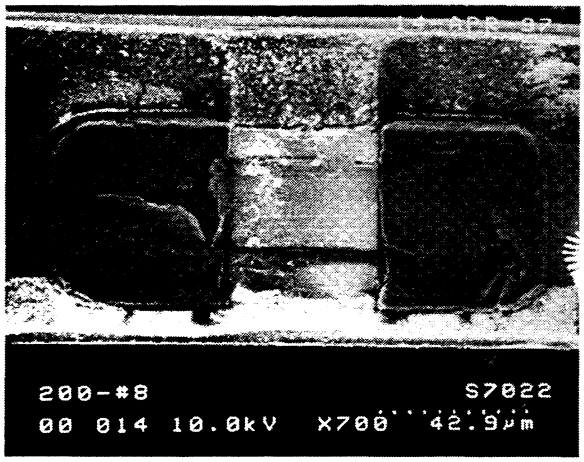

Figure 9: SEM photo of a QUID device after 200°C lifetime test.

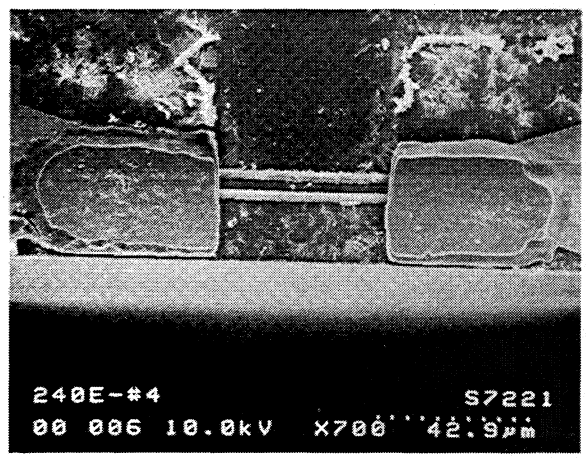

Figure 10: SEM photo of an epoxy-etched QUID device after 240°C lifetime test.

C. Effect of Si_3N_4 passivation

Prior to bonding the GaAs wafer upside-down onto a quartz substrate, a Si_3N_4 passivation layer can be put down around the anodes by a PECVD (plasma enhanced chemical vapor deposition) system. The effect of this procedure on device RF performance is currently being investigated, and its effect on device reliability is reported below.

The Arrhenius plots comparing devices with and without nitride passivation are shown in Figure 11. Both types of devices do not have an AlGaAs layer, and the epoxy inside the channels were not etched. Figure 11 clearly indicates that the nitride passivated devices have a much better lifetime than unpassivated devices. In fact, we had to tighten our failure criteria in order to keep the test from extending too long. The failure criteria in calculating the failure times are reduced by 50%. That is, the new failure criteria is $\Delta\eta > 7.5\%$, $\Delta R_s > 10\%$, $\Delta V_0 > 20\%$, or any combination of these changes that causes the mixer noise temperature to degrade by 7.5%. For a

proper comparison, the same failure criteria was applied to the batch of devices without nitride passivation.

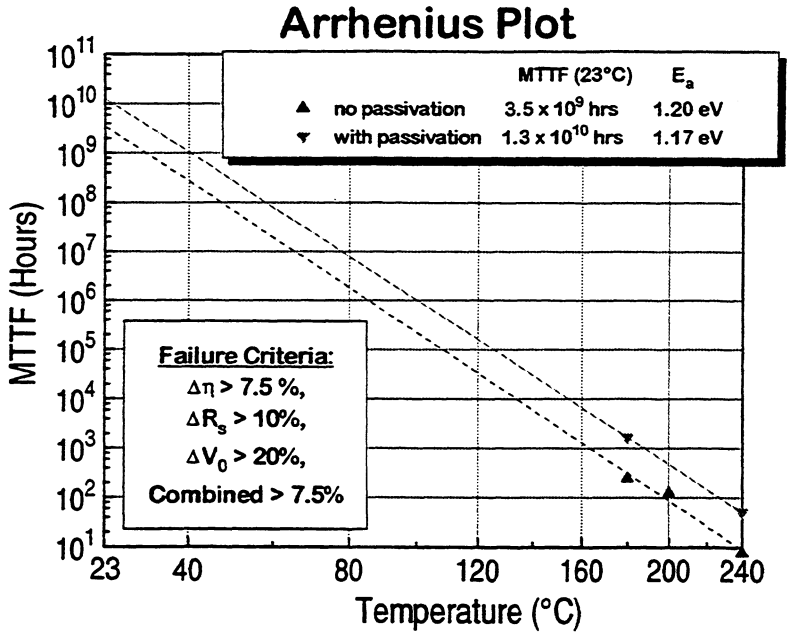

Figure 11: Arrhenius Plot for devices with and without Si_3N_4 passivation layer. Note that the failure criteria was tightened to obtain 50% sample failure from the nitride passivated devices.

Another difference that was observed in the data for passivated devices is the direction of change in the I-V characteristics. Figure 12 compares the device I-V characteristics taken at 180°C at the beginning and end of the test (after 1336 hours) for two devices, one from the unpassivated batch, and the other from the passivated batch. These two devices underwent the same test conditions at the same time, and yet their I-V curves shifted in different directions. The knee voltage for passivated devices increases, while it decreases for unpassivated devices. Currently we are investigating possible causes for this effect.

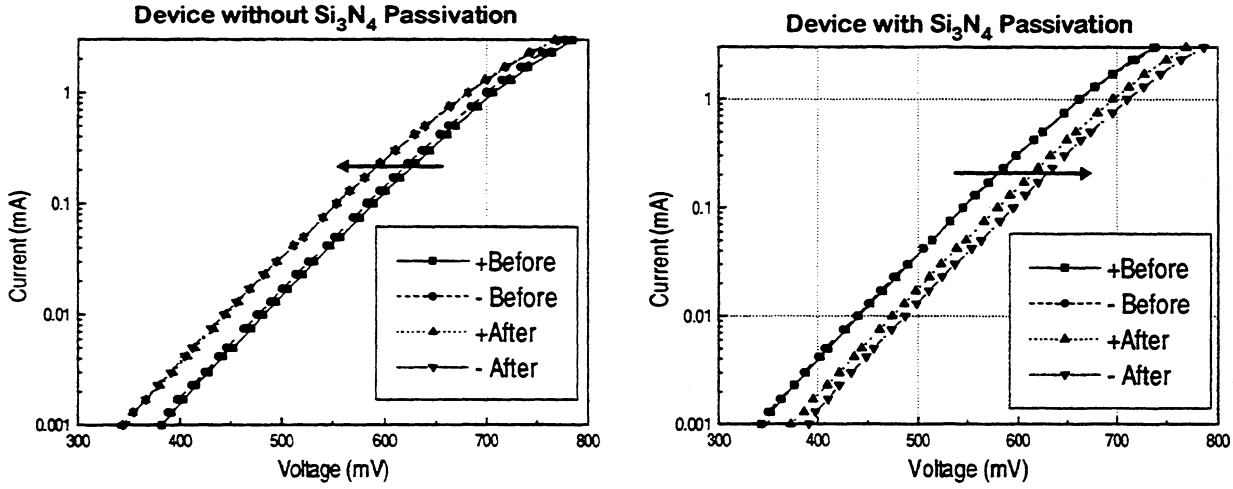

Figure 12: I-V Characteristics of devices before and after lifetime testing. These measurements were made at 180°C, at the beginning of the lifetime test and after 1336 hours.

D. Causes of failure

So far, we have observed that severe cracking in the AlGaAs layer and the channel epoxy region can cause catastrophic failures. Other mechanisms responsible for the gradual degradation could not be observed under the SEM. At this time, we have not made a complete failure analysis of QUID devices in order to determine these mechanisms. From the collected data, however, it is observed that almost all devices failed due to the series resistance meeting the failure criteria. Only the nitride passivated devices differ in that a number of passivated devices failed due to a combination of the three diode parameters.

IV. CONCLUSIONS

Based on results from numerous accelerated lifetime tests, the 640 GHz QUID circuits were determined to have a room temperature MTTF on the order of 10^{10} hours, with an activation energy of 1.2 to 1.3 eV. This value is more than three orders of magnitude higher than the five year mission that QUID devices must meet.

The effects of device processing variations on device lifetime were studied. It was found that the presence of an AlGaAs etch-stop layer can cause severe cracking under high temperature stress, thus increasing the likelihood of a catastrophic failure. The presence of the epoxy in the surface channel region was found to have little or no effect on device lifetime. The presence of a silicon nitride passivation layer, however, significantly enhanced device lifetime by nearly an order of magnitude. Observations of the changes in device I-V characteristics showed that the passivated devices have a failure mechanism different from the unpassivated devices.

Results from a more thorough failure analysis will enable us to better understand these mechanisms. The acceptable MTTF values obtained from this work show that the QUID process can be a useful technique to obtain GaAs devices on non-semiconductor substrates. This technique could also be useful for other applications where a dissimilar substrate is required.

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