E-BEAM SIS JUNCTION FABRICATION USING CMP AND E-BEAM DEFINED WIRING LAYER

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ABSTRACT

High frequency (> 0.5 THz) circuit design of SIS mixer elements used in radioastronomical heterodyne receivers demand tightly controlled junction areas with sizes smaller than 0.5 μm^2, suggesting the use of electron beam lithography (EBL). The thin PMMA electron beam resist, however, cannot be used for the usual self-aligned liftoff of the insulating dielectric. We implemented a new processing scheme similar to the PARTS (Planarized All-Refractory Technology for Superconducting electronics [1]) fabrication process developed at IBM. In this process a chemical mechanical polishing (CMP) step is used to planarize the dielectric (SiO_2). CMP of the circuits on fused quartz substrates was performed on a standard lapping machine with a simple motorized polishing head. Dielectric thickness variations across the active chip diameter (∅ 20 mm) of only ± 20 nm were achieved. In order to test the quality of our junction fabrication, square and rectangular junctions with areas ranging from 0.02 μm^2 to 25 μm^2 were fabricated and DC-tested. We further investigated EBL for the wiring layer, thus extending the process to a precise definition and positioning accuracy of all critical circuit geometries. This is especially interesting for tuning circuits at 1 THz and beyond, with typical lengths and widths in the order of a few microns. First results indicate that junctions with EBL defined wiring layers can have the same quality as those with UV defined wiring.

I. INTRODUCTION

Junction area is a crucial design factor for the integrated tuning circuits of SIS junctions. With the development of SIS mixers for frequencies at or above 1 THz, e. g. for use in the receivers of the Far Infrared Space Telescope (FIRST), junction areas have to become smaller (< 0.5 μm^2) and more precisely defined ($\Delta A_J/A_J < 10$ %) in order to ensure optimum performance of the integrated tuning circuits. At lower frequencies, ongoing developments of multi-junction circuit designs and array

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applications make tightly controlled junction areas necessary. Junction designs employing rectangular submicron areas or distributed junctions are very demanding for junction definition.

Standard UV300 contact mask-aligner lithography has its limits with linear dimensions approaching 0.8 μm and thus needs to be replaced by a more powerful technology. Two commonly employed solutions are deep UV stepper technology or EBL. In this paper we will focus on latter, as EBL technology has already been developed at KOSMA for fabrication of hot electron bolometers [2].

In the conventional self-aligned liftoff process for the fabrication of SIS junctions, a thick ($\geq$ 1.2 μm) photoresist is used both for the definition of the top electrode and for the following self-aligned liftoff of the evaporated insulating dielectric. The electron beam resist PMMA used for high resolution EBL is too thin (190 nm) to be used for these purposes (Figure 1, first column). Therefore a different fabrication scheme has to be implemented.

One possibility for pattern transfer is the use of a relatively thick polyimide underlayer beneath the EBL resist as described in [3] shown in Figure 1, second column. A disadvantage of this process is the rather difficult processing of the polyimide films and the fact that the critical liftoff step still has to be used.

A completely different approach is the use of a chemical mechanical polishing (CMP) step for planarization of the dielectric, first used in the PARTS (Planarized All-Refractory Technology for Superconducting electronics) process [1]. Here a self-aligned process step is not necessary, thus eliminating the need for a thick EBL resist. After junction top electrode RIE the dielectric is deposited onto the whole wafer without any patterning and then the dielectric is locally and globally planarized in a polishing step. Polishing is terminated when the junction top electrodes emerge at the dielectric surface (Figure 1, third column).

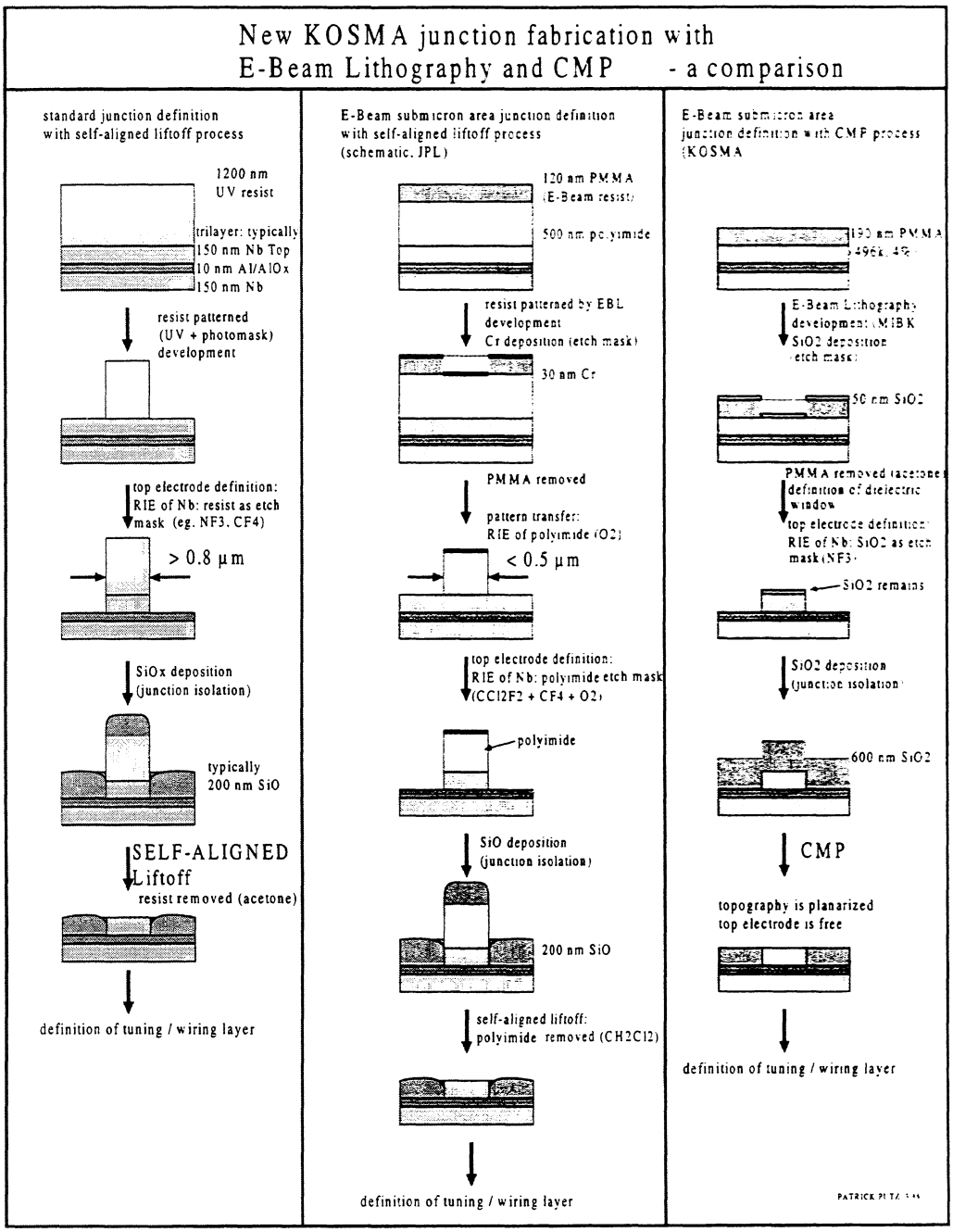

Figure 1 Comparison of junction definition with CMP to standard self-aligned liftoff and JPL processing schemes

II. CHEMICAL MECHANICAL PLANARIZATION OF INTERLAYER DIELECTRICS

CMP for planarization of interlayer dielectrics (ILD) was developed at IBM in the mid 80's for multilevel VLSI chip developments out of the need to cope with increased topography generation (also referred to as oxide CMP).

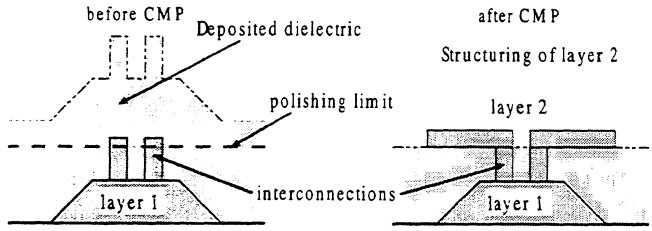

Figure 2 Illustration of ILD planarization through CMP

In a typical application the ILD, SiO_2 is deposited onto underlying circuits and is planarized through CMP and thinned until interconnections can be used for further contacting (Figure 2). During CMP the wafer is pressed onto a polishing surface (a polyurethane polishing pad) with both the wafer and the pad being rotated. A caustic aqueous polishing slurry, containing small abrasives (typically silica particles of approx. 100 nm diameter) is dispensed onto the pad. The SiO_2 surfaces of the ILD on the wafer and the silica particles become hydroxylated, and hydrogen bonding in combination with the mechanical induced slurry flow then carries away material from the ILD [5].

Because of the complex hydromechanical interactions at the ILD surface, an empirical approach for establishing the proper set of parameters for an optimal planarization yield and process stability has to be chosen. In order to establish a high planarization rate (i. e. the time it takes to reduce ILD topography to a desired level) and global uniformity of the ILD thickness, the wafer has to be in partial contact with the polishing pad. This is achieved by empirically influencing the slurry fluid film thickness through pad velocity, pad properties, wafer applied load and the wafer mounting, with the latter determining how much the wafer is recessed into its carrier. As shown in [6] for 2″ wafers, this semi-direct contact mode is achieved when the wafer sticks out less than a few mils above the carrier surface. Another important effect is the feature size dependency of the planarization rate. Structures with larger linewidths planarize slower than smaller structures due to the finite deformability of the polishing pad [6–9]. This can be a problem for

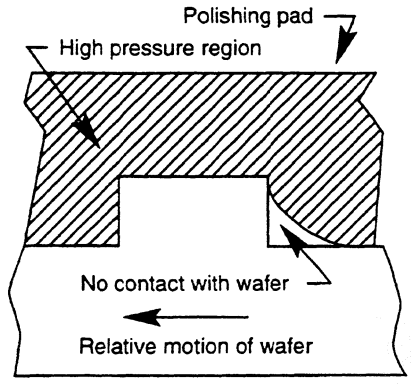

Figure 3 Deformation of polishing pad leads to greater pressure on high features and thus their planarization (from [7])

establishing interconnection of all circuits on a chip. This must be solved by the appropriate chip design.

III. KOSMA E-BEAM SIS JUNCTION FABRICATION SCHEME

The trilayer structure for the waveguide junctions is sputter-deposited onto fused quartz substrates (INFRASIL, ∅ 25 mm, 250 µm thickness) into UV lithographically patterned bilayer AZ 7212 photoresist windows [10]. The trilayer film thicknesses are 150 nm niobium for the bottom electrode, 10 nm aluminum, which is oxidized in-situ to form the AlO_x tunnel barrier with critical current densities around 17 kA/cm^2, and 230 nm niobium for the junction counter electrode. After liftoff, alignment marks are defined onto the chip through sputter-deposition of aluminum and gold, also as a liftoff process. These marks are needed for pattern alignment during EBL. Then the chip is spin-coated with a monolayer 190 nm PMMA (4 %, 496 k) and covered with 10 nm aluminum for charge dissipation during EBL.

Our EBL system, based on a CAMBRIDGE S240 SEM, is controlled by a PC running customized AutoCAD software in which the structures are defined using AutoCAD trace elements. Patterns are written into the PMMA with a beam current of 14.0 pA and doses ranging from 100 to 150 µC/cm^2 (structures are not proximity effect corrected, but larger structures receive less dose for compensation). After removing the aluminum in an acidic solution and PMMA development, 50 nm SiO_2 as the etch mask for RIE is electron beam evaporated into the PMMA patterns. A thorough O_2 plasma clean to remove H_2O from the chips' surface prior to deposition has proven to be necessary for proper SiO_2 film adhesion. After junction etch mask liftoff, a secondary etch mask, patterned with UV lithography, defines the junction isolation window. Now the top electrode is etched with RIE using NF_3 at 40 µbar, -55 V, 0.13 W/cm^2 for 48 sec.

600 nm SiO_2 as dielectric for the integrated tuning structures is electron beam evaporated (after plasma cleaning) onto the whole chip in agreement to the PARTS processing scheme (a minimal dielectric thickness according to the feature step height to be planarized, in our case 390 nm, is needed for planarization). CMP is terminated after 3–4 polishing passes when the mean dielectric thickness in the junction isolation windows is measured to be 200 nm. After CMP and post-CMP cleaning procedures – which are discussed in following chapters – the integrated tuning circuits are sputter deposited into UV-lithographically (or EBL – discussed later) patterned photoresist windows, again as a liftoff process. The wiring layer consists of 350 nm niobium covered with 30 nm gold for wire bonding. Prior to deposition the chip is argon plasma cleaned (4 min, 3.0 Pa, -450 V, 0.4 W/cm^2) in order to remove any residue from CMP (in particular the modified niobium layer on the junction tops). The chip is then diced into several parts, ultrasonically wire bonded and DC tested.

IV. EXPERIMENTAL ASSEMBLY FOR CMP

CMP was developed on a standard lapping machine [11]. This machine is equipped with a 12″ plate drive with continuously variable speeds from 0–70 rpm and a semi-circle roller sweep arm, with variable sweep amplitude and frequency, to guide the lapping / polishing head (Figure 4). Because this machine is also used for lapping fused quartz substrates it was placed in our clean room facilities or in an individual flow box environment.

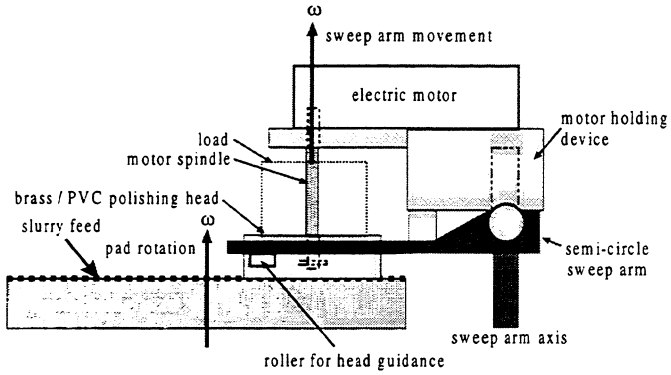

Figure 4 Schematic side-view of CMP assembly

A machined DELRIN (PVC) disc containing the wafer pocket on the bottom is mounted to the polishing head. The disc is grooved to improve slurry flow towards the wafer pocket. The applied load on the wafer is controlled by adding a specific weight on top of the polishing head. Because we use delicate 250 µm thick fused quartz substrates they are wax mounted onto a 2″ silicon wafer. A thin (2–3 µm) wax films ensure the necessary planarity of the configuration. The wafer/substrate pocket depth is designed to project the chips' surface 4 mil above the polishing head underside (Figure 5).

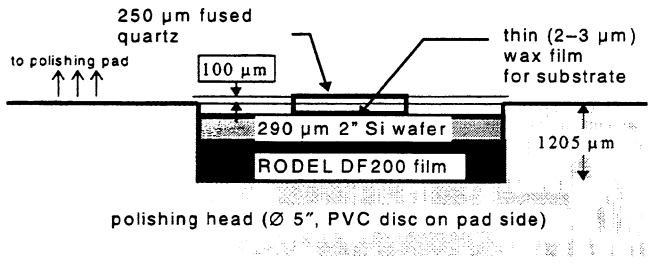

Figure 5 Schematic view of wafer pocket with wax mounting of substrate

The wafer pocket is backed by a soft buffed poromeric self-adhesive film [12] for reasons of reducing pocket surface roughness and therefore unifying load distribution onto the wafer / substrate combination. The polishing head is driven by an electric motor, its speed is adjusted according to the polishing pad speed to ensure constant relative velocity for all points of the wafer [7].

We chose a similar configuration as investigated in [6] for pocket geometry, polishing pad and slurry [12]. The IC-1000 is a hard polishing pad and exhibits greater

planarization capabilities than softer pads [6]. Slurry feed is automated by a membrane dose pump. All CMP relevant process data can be found in Table 1.

polishing head		polishing pad		slurry	
size	Ø 5″	brand	RODEL IC-1000	brand	RODEL ILD-1200
pocket size	Ø 2″	material	perforated polyurethane with soft backing	pH	11.0
wafer projection	4 mil			specific gravity	1.08
rotation speed	60 rpm	pad velocity	0.96 m/sec (60 rpm)	abrasive	silica
position	center of pad radius	size	Ø 12″	mean particle size	Ø 140 nm
sweep arm	frequency 0.1 Hz amplitude ± 2 cm	compressibility	5 %	flow rate	6 ml/min
		specific gravity	0.6–0.8	silica concentration (dilution with H_2O)	3 % weight
applied load	55 N	surface roughness	12 µm rms		
wafer backing	RODEL DF200 film	removal rate	12 nm/min		

Table 1 Summary of current CMP process data

V. CMP RESULTS

We observed no negative influence of the non-cleanroom surrounding of our CMP assembly. This can partly be explained by careful cleaning procedures, which include the storage of polishing pad and head in containers and thorough H_2O rinsing of all parts prior to CMP. We believe that the conditioning of pad surface with H_2O and the slurry also has a cleaning effect. The very small number (< 10) of microscopical scratches result from broken away material at edge of the fused quartz substrates. As a result only a few devices (of 248) on the chip actually become useless through scratching, because most of the scratches only extend 2–3 mm from the edge.

This area of the chip cannot be used anyway, because in this edge region the removal rate of the dielectric is much higher than the remainder of the chip. This effect is actually common to CMP and is described in [6]. In order to compensate for loss of chip area through this edge exclusion zone, we increased the diameter of our fused quartz substrates from 22 to 25 mm.

The IC-1000 is conditioned after every polishing pass with a diamond conditioning head to ensure constant surface roughness, which is essential for constant planarization results.

Figure 6 shows the progress of planarization on trilayer-generated SiO_2 topography, and a typical planarization result is shown in Figure 7.

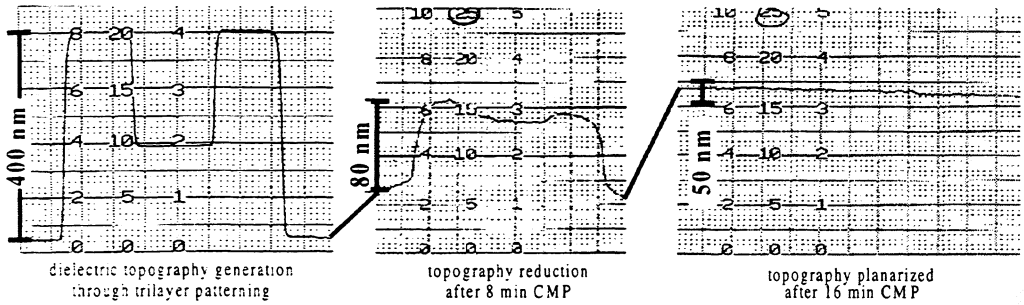

Figure 6 Profilometer scans of planarization progress (note: ordinate scale changes and is not absolute)

Another important observation we made is effect of planarization feature size dependency: The geometry of the individual waveguide mixer devices in our chip layout result to a higher SiO_2 planarization rate at the junction area (the tapered waveguide probes) than on the larger bondpads at the end of each device (Figure 7). Contact problems arising from this situation were solved by patterning windows into the dielectric on the bondpads.

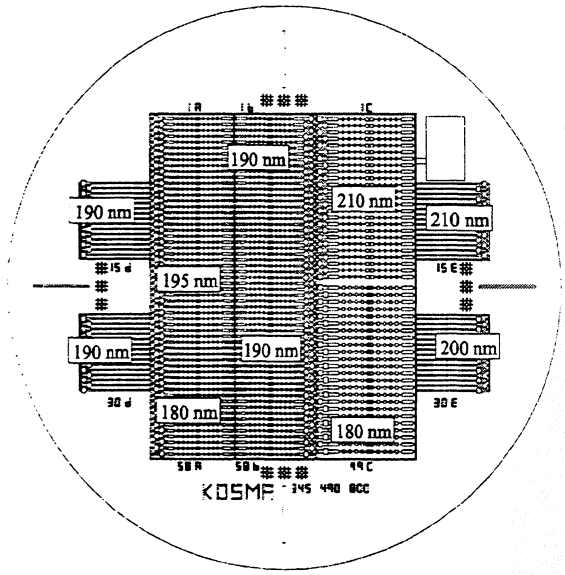

Figure 7 Typical global planarity result of CMP process on dielectric: ± 20 nm

Post-CMP cleaning is made by extending the CMP pass for another two minutes, with stopped slurry flow but generous H_2O rinsing of the polishing pad. The wafer/substrate combination is kept wet for transport into the cleanroom and then swabbed with H_2O and dried with IPA on a photoresist spinner.

VI. Investigation of EBL Defined Wiring Layer

Terahertz mixer circuits react very sensitive to misalignment of the integrated tuning structures relative to the SIS junctions. Typical tolerances of 1–2 μm in wiring positioning by optical mask-aligner tolerances are not tolerable for circuits working at these high frequencies. We therefore investigated EBL definition of the integrated

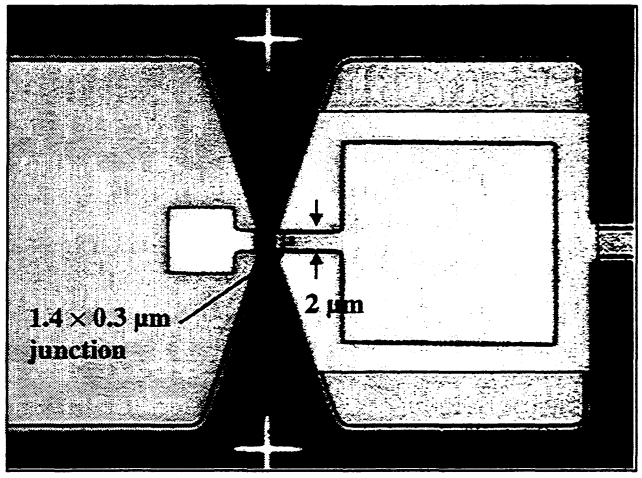

Figure 8 Photograph of a 800 GHz shorted stub tuning structure EBL patterned in photoresist prior to wiring layer deposition

tuning circuits, which allows a relative positioning accuracy of about 100 nm. This precision makes it possible to use tuning circuit designs which are even more critical in adjustment, such as rectangular junctions embedded in narrow tuning lines (Figure 8).

Another large advantage of EBL of tuning circuits is its flexibility. Changes in tuning designs can easily and fast be incorporated into the fabrication process, as there is no need to fabricate chrome masks for UV lithography.

EBL defined tuning structures could easily be integrated into our new EBL/CMP junction process scheme described earlier: After CMP the wafer is spin-coated with a 600 nm thick UV photoresist (AZ 5206, resolution 0.3 µm) and 10 nm copper is deposited on top for charge dissipation during EBL. The tuning structures are written with a beam current of 14.0 pA and a dose of 15 $\mu C/cm^2$ without any proximity effect corrections. After removal of the copper layer through an $FeCl_3$ solution etch, the photoresist is developed with AZ 400K (diluted 1:3 with H_2O).

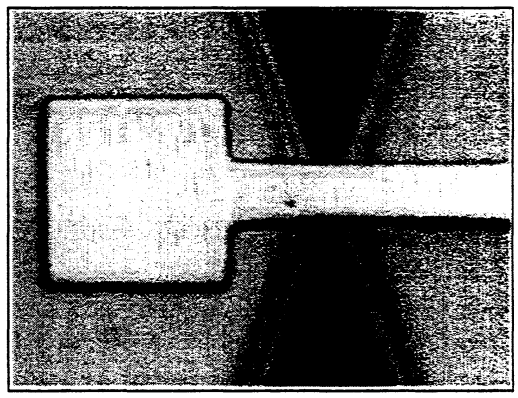

Figure 9 Close-up on waveguide feed of the same tuning structure depicted in Figure 8 after liftoff of 380 nm thick wiring layer

The wiring layers are then sputtered into these photoresist windows as a liftoff structure in the same manner as described previously for UV definition. Pattern alignment during wiring EBL is made with the same alignment marks as used for junction EBL.

Liftoff of the 380 nm thick wiring in the 600 nm thick photoresist produces very smooth edges (Figure 9). We attribute this to the fact that EBL intrinsically produces undercut photoresist sidewall profiles, because a large exposure contribution is made by backscattered secondary electrons from underneath.

VII. DC I/V ANALYSIS

Junction areas of square and rectangular shape ranging from 0.02 to 25 μm^2 were defined and their subgap leakage characteristics examined. The tuning structures were UV-lithographically and EBL defined for different parts of the chips in order to investigate possible adverse effects of wiring EBL on junction quality.

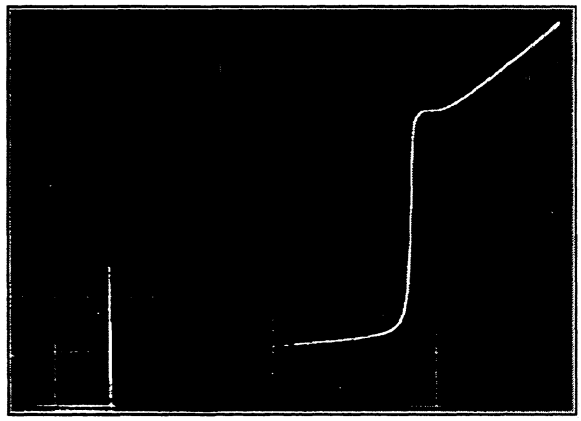

Figure 10 I/V-curve (0.5 mV/div, 5 μA/div) of a 0.1 μm^2 Nb/AlO_x/Nb SIS junction (J_c = 17 kA/cm^2, R_{subgap}/R_N = 18) with E-Beam defined wiring layer

To present date our I/V analysis data does not give clear indication that the junction barrier quality is deteriorated due to charge buildup during wiring EBL

All junctions, with areas from 0.1 μm to 0.6 μm analyzed, were fabricated with EBL wiring.

share of junctions with $R_{subgap}/R_N > 10$	share of junctions with $R_{subgap}/R_N > 15$	variation of junction area < 0.6 μm^2
84 %	**38 %**	**7 %**
80 junctions measured		20 junctions measured

Table 2 Junction process yield of one chip (all junctions measured have EBL wiring, J_c = 13 kA/cm^2)

The precision of area definition was calculated from the junction normal resistance variance, as it is not easy to measure such small area deviations in an optical microscope. The junction area variations are below 10 %.

CONCLUSION

It has been shown that a CMP process step in combination with EBL defined SIS junctions on thin fused quartz substrates for use in radioastronomical heterodyne waveguide mixers is feasible with off-the-shelf equipment. The approach of using an existing lapping machine with a simple polishing head and the "piggyback" mounting of fused quartz substrates on 2″ Si wafers delivers very promising first results. We are convinced that further evaluation of the process and more detailed investigation of all input variables will improve the global planarization results.

With R_{subgap}/R_N ratios well above 10 our new fabrication process delivers $Nb/AlO_x/Nb$ junctions with the same quality as with the present standard self-aligned liftoff junction fabrication, with highly reproducible junction areas as small as 0.2 μm^2.

EBL definition of the wiring layer does not noticeably deteriorate junction quality and will lead to an increased precision in alignment and definition of the integrated tuning circuits.

ACKNOWLEDGMENT

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