WEB-BASED SIMULATION OF MIXERS, MULTIPLIERS AND OSCILLATORS

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Abstract - The Applied Electrophysics Laboratory at the University of Virginia has developed a web based device simulation environment to accurately model and simulate high frequency mixers, multipliers and oscillators. The simulation environment uses a three-tier client server architecture to free the user from low level computing details. The user interfaces for the devices being simulated have been developed in Java. A major benefit of Java programs is that they can be run on any hardware architecture for which a Java virtual machine exists, allowing our simulation programs to run on a variety of platforms. The simulation environment has been successfully implemented, and is being used by researchers for simulation and design of high frequency devices. This environment hides the less important details of simulation and lets the researcher concentrate on the most important parameters. This environment has the additional benefit of allowing researchers to run simulations from any computer connected to the Internet.

I. INTRODUCTION

Computer simulation is widely used in many fields for design, development, and research. Semiconductor researchers in particular employ a wide variety of tools to simulate material processing and device performance. The millimeter and submillimeter-wave regions of the electromagnetic spectrum continue to be areas of increasing interest. Millimeter waves correspond to the frequencies between 30GHz and 300GHz, while the submillimeter-wave range is defined to be the region between 300GHz and 3THz. In recent years, scientists and engineers have intensified their efforts to create more complex systems at millimeter and submillimeter wavelengths affording improved range, increased frequencies, frequency stability, and durability. In order to effectively design these complex systems, which consist of highly nonlinear circuits such as large-signal amplifiers, frequency converters such as mixers and multipliers, or oscillators, various accurate and fully self-consistent computer aided simulation tools have been developed.

In general these simulation tools operate as computationally intensive Fortran programs. Expensive and powerful computing hardware is required to run these tools effectively. Many of these simulation tools are potentially reusable for related research efforts and educational purposes. However, they tend to be used only at the places where they were developed because of limited availability of required resources and the problems inherent to porting and distributing software. The complex nature of these Fortran codes coupled with the cost of the necessary computing hardware makes the large-scale distribution of these codes impractical and inefficient. Hence, an ability to quickly access and run such tools via the Internet would be very beneficial to designers.

The main aim of this research is to develop a simulation environment that allows designers and researchers around the world to run these tools quickly and effectively without the need to maintain expensive and powerful computing hardware. We describe a simulation environment which allows for accurate modeling and simulation of high frequency devices and circuits. The applications developed under this simulation environment include Heterostructure Barrier Varactors (HBV), GaAs Schottky Barrier Diode Mixers (SBM), GaAs Schottky Barrier Diode Varactors (SBV), InP & GaAs Transfer Electron Oscillators (TEO), and high frequency Bipolar Junction Transistors (BJT).

These applications are divided into three categories: Local Applications, Relatively Fast Network Applications and Slow Network Applications. The Local Applications, also known as Quick Design applications, are developed to aid in the HBV and SBV full simulations. Prior to the submission of a full simulation, the user can run the corresponding Quick Design application, which returns results in few seconds. Though the Quick Design application results are less accurate than the full simulation results, they provide insight into the optimal embedding impedance values and device parameters. After the iterative process of using the Quick Design application to estimate the results of full simulation, the user can then run the full simulation to obtain more accurate results. The HBV and SBV full simulations, which are Slow Network Applications, have simulation times as high as few hours. The Local Applications are run exclusively and entirely on the end-user's system and do not make use of the network for simulation purposes.

The Relatively Fast Network Applications and the Slow Network Applications are network-aided applications. Actual simulations are run on high-end Unix machines, which reside at the University of Virginia. These applications use a client-server architecture to transfer data between the simulation clients and the compute servers running the actual simulations. The input parameters and results are transferred between the client and the server over the network, which in our case happens to be the Internet. The Relatively Fast Network Applications have faster computation times than the Slow Network Applications.

The simulation environment has been developed in Java using a client-server architecture. The platform independence of Java programs allows the applications in our simulation environment to be run from a variety of platforms. This environment allows a worldwide workgroup of design and research engineers to concurrently share the same computational resources without getting lost in the minute details of computing.

II. APPLICATIONS DEVELOPED

We have developed six applications – two Local Applications, three Relatively Fast Network Applications and one Slow Network Application. All applications are up and running and can be downloaded from our web-site. The Schottky Barrier Varactor (SBV) Quick Design for design of 50-600 GHz GaAs SBV frequency doublers and the Heterostructure Barrier Varactor Quick Design for design of 100-900 GHz AlGaAs/GaAs HBV frequency triplers are the two Local Applications. The SBV Quick Design employs the equivalent circuit model proposed by Jones and Lipsey [1] with the semi-empirical coefficients derived from the Monte-Carlo Harmonic Balance (MCHB) simulator. The HBV Quick Design employs the equivalent circuit model proposed by Jones and Stake [2] with the design coefficients derived from the Drift-Diffusion Harmonic Balance (DDHB) simulator. The simulation times for both these applications are on the order of a few seconds and the results are displayed in text format.

Transferred Electron Oscillator (TEO) Design, Bipolar Junction Transistor (BJT) Design and Schottky Barrier Diode Mixer (SBM) Design are the three Relatively Fast Network Applications. For these three applications a combination of textual, tabular, and graphical results are displayed on the end-user's machine once the simulations are completed on the high-end Unix workstations. The TEO Design is for analysis and design of 50-200 GHz InP and GaAs transferred electron devices. It employs the integrated DDHB simulator developed by Jones and Zybura [3]. The simulation time varies with the tolerance parameter – the lower the tolerance, the higher the simulation time. The simulations take from a couple of minutes to a maximum of ten minutes depending on the tolerances. The BJT Design is for analysis and design of bipolar transistors. It employs the Vertical Bipolar Inter-Company (VBIC) [4], which is an equivalent circuit model. VBIC was defined by a group of representatives from the IC and CAD industries as an industry standard replacement for the Spice Gummel-Poon (SGP) model. VBIC is public domain and the complete source code is available at **http://www-stall.rz.fht-esslingen.de/institute/iafgp/neu/VBIC/**. The simulation time for this application varies from 30 seconds to a couple of minutes. The SBM Design is for analysis and design of 100-1000 GHz Schottky diode mixers. This application employs the integrated Equivalent Circuit/Harmonic-Balance (ECHB) simulator proposed by Siegel and Kerr [5]. The simulation time for this application is comparable to the BJT Design. It varies from 30 seconds to a couple of minutes.

Heterostructure Barrier Varactor (HBV) Design, the Slow Network Application, is for analysis and design of 100-1000 GHz GaAs/AlGaAs HBV frequency multipliers. This application employs the integrated DDHB simulator developed by J.R. Jones and S.H. Jones [6]. The simulation time for this application depends on the tolerance parameter. It varies from a few minutes to a couple of hours. It is impractical to expect the user to be logged on and wait for the results for this amount of time. Hence, the results are sent to the user by email once the simulations are completed.

III. SIMULATION ENVIRONMENT ARCHITECTURE

In this section we discuss the details of the simulation environment. Figure 1 gives a graphical description of our system. The simulation environment uses a three-tier client server architecture comprising of simulation clients, simulation servers, and middle-ware to connect the client and server. The simulation client consists of a graphical user interface (GUI) where the simulation parameters are entered. These clients have been implemented as Java applications. We have developed clients for the high frequency devices mentioned above.

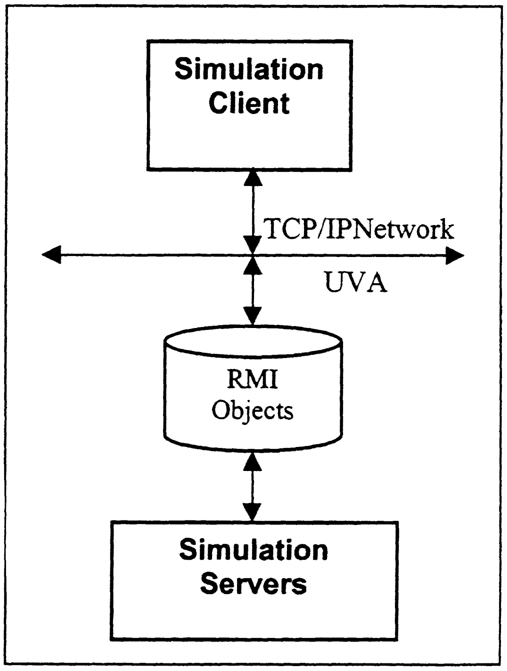


Figure 1 Simulation Environment Architecture

The simulation servers are where the actual execution of the simulations takes place. These machines are powerful UNIX servers running the Fortran programs developed for the devices.

The RMI objects allow for communication between the clients and the servers. RMI (Remote Method Invocation) is a Java technology that allows Java objects to invoke methods on other Java objects residing on different machines. This allows our simulation clients, residing on any machine connected to the Internet, to start simulations on machines residing at UVA. This also allows the simulation servers to return results back to the clients. Each simulation application has a RMI object on the simulation servers listening for messages from the respective simulation client.

The steps that take place in executing a simulation in this environment are as follows. The user starts the client associated with the particular device being simulated. The parameters are entered into the input fields of the client application. The simulation is then initiated. If the simulation is a Quick Design, the computation takes place on the user's machine and the results are displayed in a few seconds. If the simulation is a Network Application, the user is presented with a list of machines on which that particular simulation is available. The user then selects one machine on which the simulation will take place.

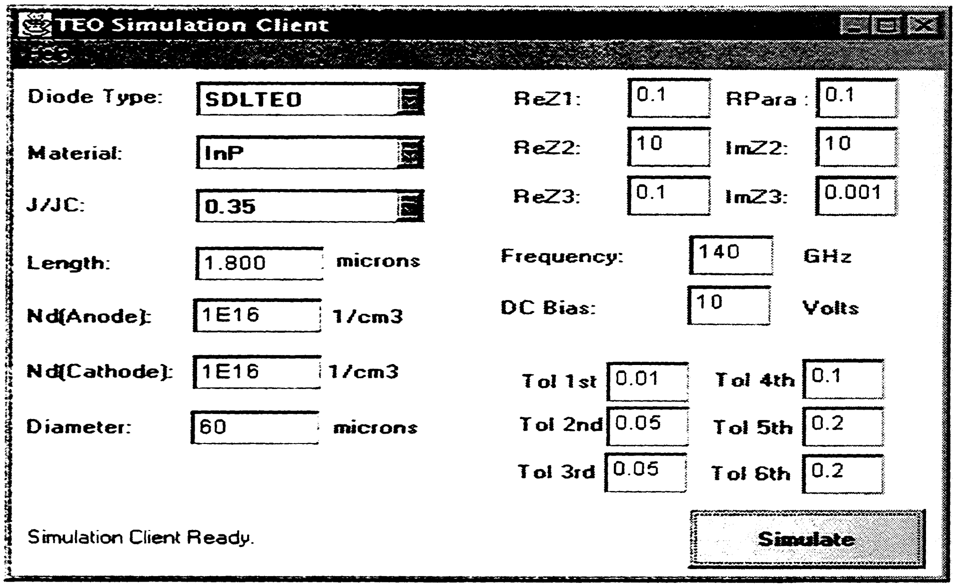
Once a machine has been chosen, the client invokes a method on the RMI object residing on the selected machine, requesting the execution of a simulation. This method invocation also results in the input parameters being transferred to the RMI object. The RMI object then uses the input parameters to create a input file for the simulation. The RMI object then starts the simulation engine for the device being simulated. Once the simulation is completed, the RMI object collects the results and returns it to the client. The Slow Network applications email the results back to the user, as it is unreasonable to expect the user to wait a few hours for the results.

In order to use this simulation environment, the software for the clients needs to be downloaded from our web site. We currently have a convenient client installation program available for users running Windows 95/98 and Windows NT on their machines. Users on Unix platforms currently have to manually install the client software on their machines (An automatic install option is currently being developed).

Our simulation environment is advantageous to the researcher for several reasons. We are able to offer an ever increasing library of device simulation programs. All that is required of the researcher is a one-time download of the client software. Moreover, the clients can be run from any platform and from any computer connected to the Internet. The three-tier architecture also gives us flexibility in maintaining the simulation servers. We are able to quickly bring in newer, more powerful servers into the environment without bringing down the entire simulation environment. Overall, this simulation environment gives researchers a powerful, virtual compute center for carrying out an array of high frequency device simulations.

IV. DEMONSTRATION APPLICATION

This section gives a walk-through of the simulation environment using one of the device simulations. Accurate and efficient analysis of InP & GaAs 50-200 GHz Transferred Electron Oscillators can be obtained with the TEO Design application. This application employs the integrated drift and diffusion device/harmonic-balance (DDHB) nonlinear circuit simulator developed by Jones and Zybura. When the application is started, the GUI window shown in Figure 2 is displayed. The device parameters such as the length of the device, diameter, anode and cathode doping, the initial condition (J/JC), fundamental frequency, dc bias, and the impedances and tolerances at different harmonics are entered through this window. This application allows the analysis of two types of TEDs: the conventional Gunn diode and the Standard Depletion Layer (SDL) TED. The Gunn diode employs a n^+-n-n^+ epitaxial doping profile whereas the SDL TED employs a n-n^+ epitaxial doping profile. The semiconductor material for these TEDs can be either Gallium Arsanide (GaAs) or Indium Phosphide (InP). Users can select the diode type and the material for the diode from the GUI window.



TEO Simulation Client

Diode Type: SDLTEO
Material: InP
J/JC: 0.35
Length: 1.800 microns
Nd(Anode): 1E16 1/cm3
Nd(Cathode): 1E16 1/cm3
Diameter: 60 microns
ReZ1: 0.1
RPara: 0.1
ReZ2: 10
ImZ2: 10
ReZ3: 0.1
ImZ3: 0.001
Frequency: 140 GHz
DC Bias: 10 Volts
Tol 1st 0.01
Tol 4th 0.1
Tol 2nd 0.05
Tol 5th 0.2
Tol 3rd 0.05
Tol 6th 0.2

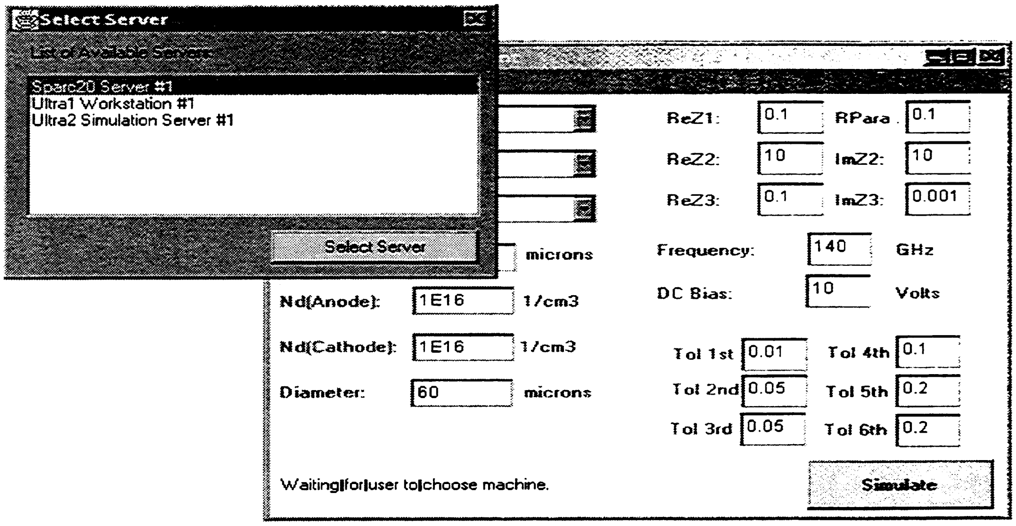
Simulation Client Ready.

Figure 2 TEO Simulation Client GUI

After entering all the necessary parameters, the simulation is started by clicking the "Simulate" button. After the "Simulate" button is clicked, a machine selection dialog box is displayed. The machine selection dialog box along with the GUI window is shown in Figure 3. This dialog box has a list of machines on which the simulations can be run. The user can select a particular machine depending on the level of computation necessary for the simulation.

Once the machine has been selected, the simulation is started on that particular machine. The results are sent back to the client on the end-user's system after the simulation has finished execution. When the client has received the results, the window shown in Figure 4 is displayed. This window contains device data such as the power, voltage, impedance and admittance values at the six harmonics, starting and ending temperature of the active layer, and the D.C. current and voltage values. Other results can be viewed by selecting the options provided on this window. This window has options for displaying graphs and tabular data for the following results:

- Terminal Currents (i) Vs. position (x), time (t)
- Electron concentration (n) Vs. x, t
- Voltage (P) Vs. x, t
- Electric Field (E) Vs. x, t



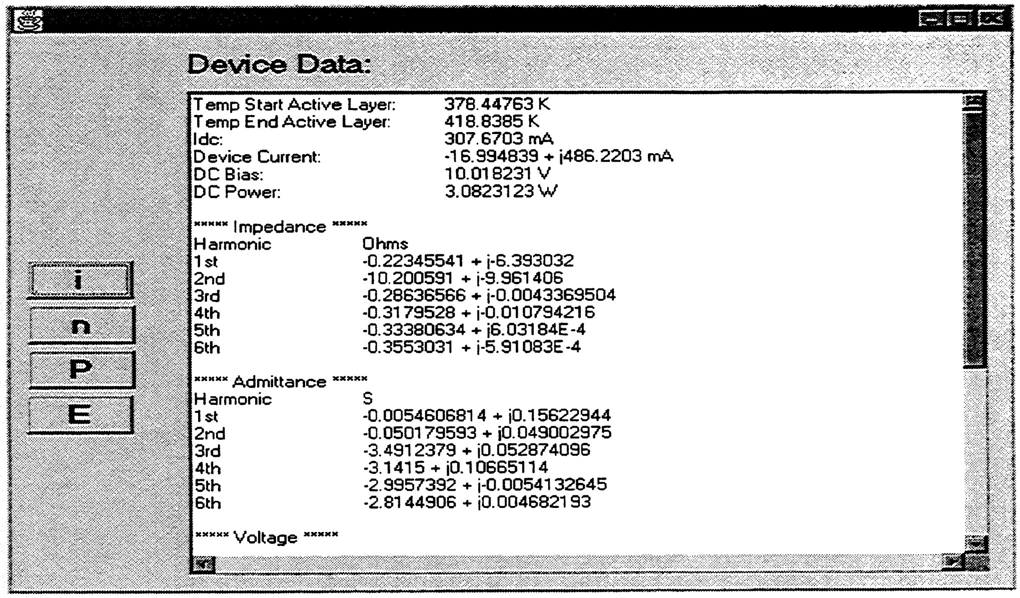
Sparc20 Server #1
Ultra1 Workstation #1
Ultra2 Simulation Server #1

microns
Nd(Anode): 1E16 1/cm3
Nd(Cathode): 1E16 1/cm3
Diameter: 60 microns

ReZ1: 0.1 RPara: 0.1
ReZ2: 10 ImZ2: 10
ReZ3: 0.1 ImZ3: 0.001
Frequency: 140 GHz
DC Bias: 10 Volts
Tol 1st 0.01 Tol 4th 0.1
Tol 2nd 0.05 Tol 5th 0.2
Tol 3rd 0.05 Tol 6th 0.2

Waiting for user to choose machine.

Figure 3 TEO Application Machine Selection



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Temp Start Active Layer:    378.44763 K
Temp End Active Layer:      418.8385 K
Idc:                        307.6703 mA
Device Current:             -16.994839 + j486.2203 mA
DC Bias:                    10.018231 V
DC Power:                   3.0823123 W

***** Impedance *****
Harmonic              Ohms
1st                   -0.22345541 + j-6.393032
2nd                   -10.200591 + j-9.961406
3rd                   -0.28636566 + j-0.0043369504
4th                   -0.3179528 + j-0.010794216
5th                   -0.33380634 + j6.03184E-4
6th                   -0.3553031 + j-5.91083E-4

***** Admittance *****
Harmonic              S
1st                   -0.0054606814 + j0.15622944
2nd                   -0.050179593 + j0.049002975
3rd                   -3.4912379 + j0.052874096
4th                   -3.1415 + j0.10665114
5th                   -2.9957392 + j-0.0054132645
6th                   -2.8144906 + j0.00468293

***** Voltage *****
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Figure 4 TEO Application Results Summary

The TEO application has demonstrated the feasibility of our simulation environment. Using the simulation environment, researchers concentrate on the most important simulation parameters while not having to deal with minor computing details. The client uses a simple GUI to gather information from the user. The platform-independence of Java programs allows the simulation client to be run from a variety of hardware platforms. Finally, the user is able to submit simulations from any computer connected to the Internet.

V. CONCLUSION

We have described a new simulation environment for the simulation of high frequency mixers, multipliers, and oscillators. Existing device simulation applications run as stand alone applications on expensive Unix servers. The complex nature of these codes and the effort involved in porting them to other platforms prevents large-scale distribution of these applications. Our approach uses a three-tier architecture of simulation clients, simulation servers, and Java RMI middleware to connect the clients and the servers. Using our simulation clients, users can initiate device simulations from any computer connected to the Internet. Users also have access to an expanding library of device simulation applications. Our simulation environment allows researchers all over world to execute an array of device simulations without having to buy expensive computing hardware or maintain complex simulation codes.

ACKNOWLEDGEMENTS

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