IMPROVED DIODE GEOMETRY FOR PLANAR HETEROSTRUCTURE BARRIER VARACTORS

Jan Stake[1], Chris Mann[2], Lars Dillner[1], Mattias Ingvarson[1], Stephen H. Jones[3], Stein Hollung[1], Henini Mohamed[4], Byron Alderman[4], Martyn Chamberlain[4], and Erik Kollberg[1]
[1]Chalmers University of Technology, SE-412 96 Göteborg, Sweden
[2]Rutherford Appleton Laboratory, Chilton, Oxon, UK
[3]Virginia Semiconductor, Inc., Fredericksburg VA 22401, USA
[4]School of Physics and Astronomy, University of Nottingham, Nottingham NG7 2RD, UK
Email: stake@ep.chalmers.se

Abstract—We report state-of-the-art performance of tripler efficiency and output power for a new design of AlGaAs-based heterostructure barrier varactor diodes. The new diodes were designed for reduced thermal resistance and series resistance. An efficiency of 4.8% and a maximum output power of 4 mW was achieved at an output frequency of 246 GHz.

Index Terms—HBV, varactor frequency tripler, self-heating.

I. INTRODUCTION

Recent progress in planar Heterostructure Barrier Varactor (HBV) design [1], has given performance comparable to Schottky varactor diodes at output frequencies below 400 GHz. The first planar HBVs were fabricated with a non-optimal diode geometry with high thermal resistance (~2 K/mW) [2] as well as high conduction current due to a low barrier height (0.17 eV). Consequently, self-heating of these HBVs [3], resulted in an increased conduction current as the temperature increased, and hence, reduced multiplier efficiency. As thermionic emission dominates the electron transport across the barrier region of standard $Al_{0.7}GaAs/GaAs$ HBVs, lattice matched InP material systems have been used to significantly reduce the conduction current in these devices [4]. However, to grow many stacked barriers and very thick epitaxial layers in an InP material system is difficult and expensive. Furthermore, the conversion efficiency critically depends on the parasitic series resistance which generally increases with temperature. The effect of current saturation is also increased with temperature due to a lower maximum electron velocity [5, 6]. A GaAs system is cheaper and is easier to process.

In this paper, we present a new batch of $Al_{0.7}GaAs/GaAs$ HBV (CTH-NU2003) diodes. The new diodes were designed for reduced thermal resistance and parasitic resistance. Experimental tripler results for the new design (hbv-3a) show state-of-the-art performance for $Al_{0.7}GaAs/GaAs$ based HBVs.

II. THE DEVICE

A. Fabrication

The $Al_{0.7}GaAs/GaAs$ epitaxial structure (NU2003), MBE grown on semi-insulating GaAs substrate by the University of Nottingham, consists of two barriers, and an n^{++} $InAs/In_{1.0\text{-}0.0}Ga_{0.0\text{-}1.0}As/GaAs$ epitaxial capping layer to improve the specific contact resistance of the resulting ohmic contacts (see Table I). This material design is similar to the UVA-NRL-1174 HBV material [2]. The measured I-V and C-V characteristic are shown in Figure 1. Simple test structures were fabricated and the measured I-V and C-V characteristics are consistent with the results from the UVA-NRL-1174 material. A back-to-back geometry, shown in Figure 2, has been utilised to double the number of barriers and to compensate for any asymmetries. The HBVs were fabricated using standard photolithography techniques for isolation and ohmic contact patterning, Cl-based reactive ion beam etching for anode definition, and wet etching for the mesa/pad isolation [2]. The surface channel was planarised prior to airbridge formation using a low-viscosity thermosetting epoxy and a planarising superstrate [2, 7]. The fingers were Au-electroplated to a thickness of ~4 µm. Special attention was given to the ohmic contact formation and the anode isolation etch, since these steps affect the series resistance, and thus the tripler performance, drastically. The Au/Ge/Au/Ni/Au ohmic metallic scheme [8] was alloyed for one minute at 400°C. The resulting specific contact resistance is less than 50 $\Omega\mu m^2$. The HBVs were diced into individual chips with the overall dimensions of 20 x 150 x 60 μm^3.

TABLE I: NU2003 LAYER STRUCTURE

Material	Doping [cm^{-3}]	Thickness [Å]
InAs	1×10^{19}	100
$In_{1\rightarrow0}GaAs$	1×10^{19}	400
GaAs	1×10^{19}	3000
GaAs	8×10^{16}	2500
GaAs	Undoped	35
$Al_{0.7}GaAs$	Undoped	200
GaAs	Undoped	35
GaAs	8×10^{16}	5000
GaAs	Undoped	35
$Al_{0.7}GaAs$	Undoped	200
GaAs	Undoped	35
GaAs	8×10^{16}	2500
GaAs	1×10^{19}	40000
GaAs	SI	-

B. Parasitic resistances analysis

The new planar HBV design incorporates a shorter finger with a larger cross section area, mainly to reduce the thermal resistance of the diode. Changing the anodes from an almost circular to a rectangular shape will both reduce the thermal resistance and the spreading resistance between the anodes. Furthermore, reducing the distance between the anodes from 5 μm (hbv-o) to 3 μm (hbv-3a) will also reduce the series resistance.

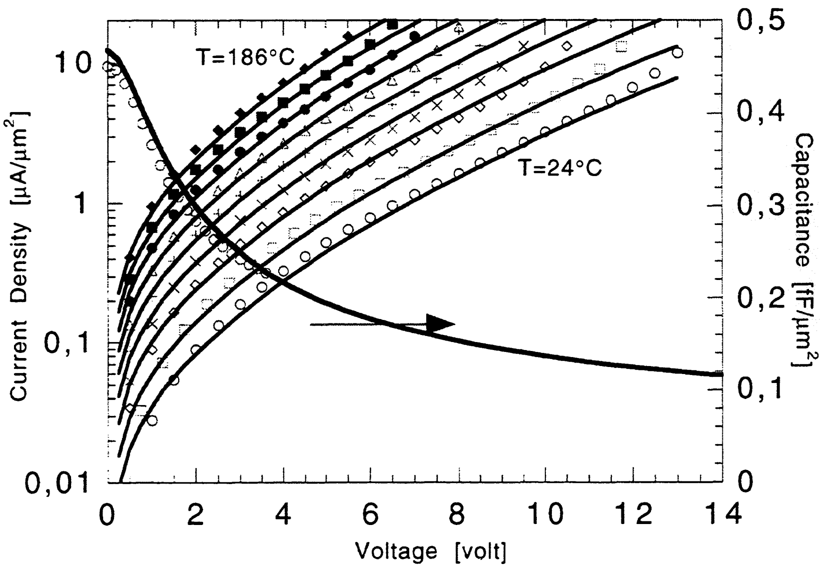

Figure 1: Measured I-V and C-V characteristics (UVA-NRL-1174 material).

The parasitic series resistance is the sum of the resistance of the undepleted active layers, the spreading resistance, and the ohmic contact resistance. All these resistive elements have different temperature dependence. In general, it is difficult to determine the series resistance of HBVs or back-to-back Schottky varactor diodes from DC-measurements, given the large junction resistance over the normal operating range of the device. For the HBVs described and with a specific contact resistance of ~ 50 $\Omega\mu m^2$, a room temperature series resistance of 12 Ω was estimated for hbv-o and 10 Ω for hbv-3a, see TABLE II. These values were calculated using standard expressions for contact resistance, mesa resistance and spreading resistance in the n^{++} island that connects the two diodes, as well as using impurity dependent mobility values for GaAs [9].

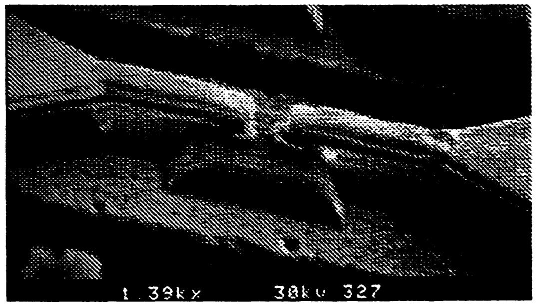

Figure 2: SEM picture of the new planar design (hbv-3a).

Assuming a point heat-source in the middle of the active region, Jones [10] has estimated the thermal resistance through the finger and the GaAs substrate to $R_t \approx 2\ K/mW$ for the old device geometry, by using a combination of analytical models and FEM-simulations. The same technique was used to estimate the thermal resistance of the new HBV diode design. The theoretical parasitic resistance and thermal resistance for the new diode design and the original planar HBV design [2] are summarised in TABLE II. Room temperature material data has been used for the calculations.

TABLE II: PARASITIC RESISTANCES

HBV / Batch	Area [μm^2]	R_s [Ω]	R_t [K/mW]	Finger size [μm^3]
3a / CTH-NU2003J	52	10	0,7	17x4x5
o / UVA-NRL-1174	57	12	2	50x4x4

III. TRIPLER MEASUREMENTS

The tripler block used was a Rutherford Appleton Laboratory (RAL) block (HBVII) which was designed for use with symmetric varactor diodes. Compared to a conventional varactor tripler block, there is no need for idler cavity or DC-bias line. The planar HBV chip was lapped to a thickness of about 20 µm and mounted across the output waveguide. The tripler block is equipped with two input tuners and two output tuners.

Input power was provided by a J.E. Carlstrom (H270) Gunn oscillator which can be tuned over a frequency range of 75 - 90 GHz. For the higher frequency range, 90 - 110 GHz, an ELVA BWO was used. Sufficient power was available so that an isolator, an attenuator and directional couplers could be included in the input chain to determine input and reflected power levels. Input and output powers were measured using separate Anritsu power heads and meter type ML 83A, which had previously been compared with a Thomas Keating power meter and had been found to agree to +/- 5%. In order to match the output waveguide to that of the output power head it was necessary to include a waveguide transformer section. The additional loss the transformer section introduced was not corrected for.

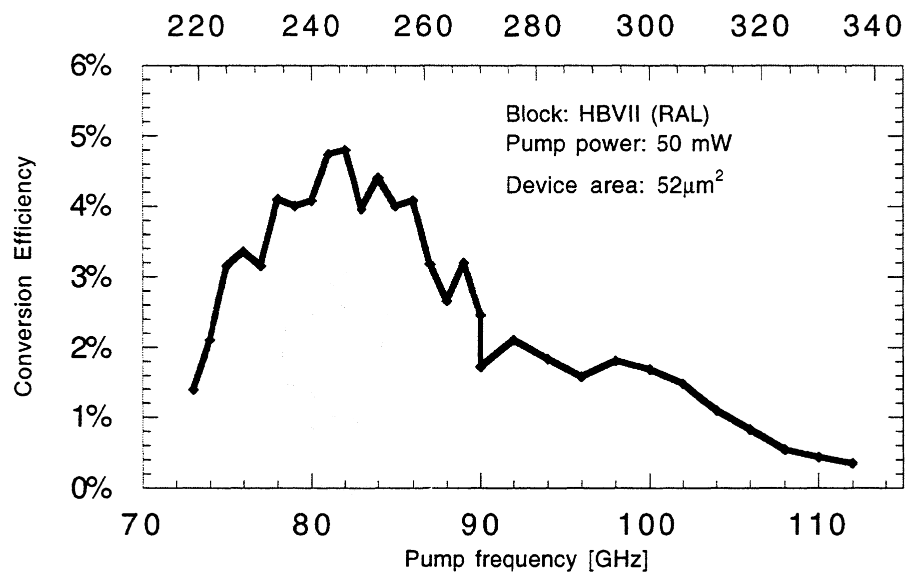

Figure 3: *Conversion efficiency versus pump frequency for an input power of 50 mW (hbv-3a).*

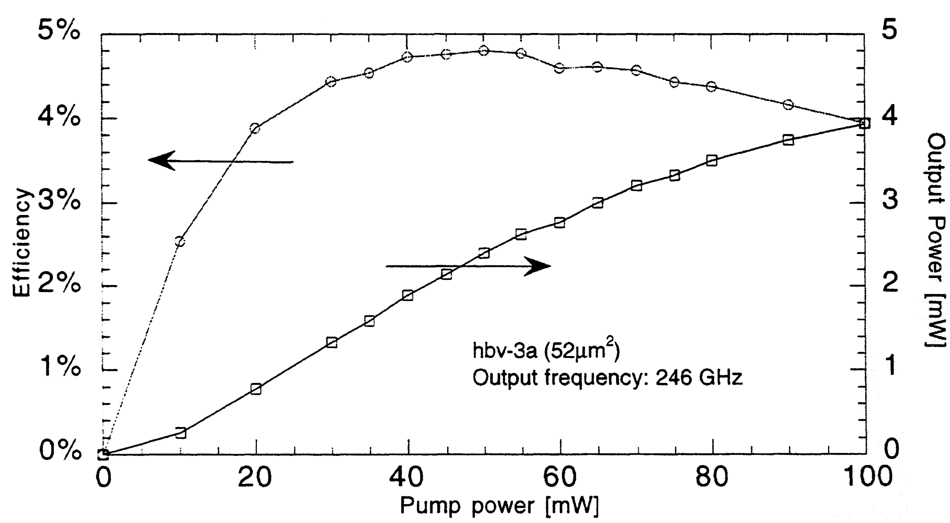

Figure 4: *Output power and tripler efficiency versus pump power (hbv-3a).*

IV. Results and Discussion

For an input power of 50 mW, the maximum output power was obtained at a pump frequency of 82 GHz for hbv-3a, see Figure 3. A maximum output power of 4 mW was generated at 246 GHz and a peak flange-to-flange efficiency of 4.8% was achieved at an available input power of 50 mW, see Figure 4. These results should be compared with an efficiency of 3.1 % and a maximum delivered output power of 2 mW achieved with hbv-o in TABLE II (UVA-NRL-1174-17) [3]. The improvement is expected to be due to a lower series resistance and thermal resistance.

V. Conclusions

In this paper we have reported an improved planar HBV diode geometry. The thermal resistance and series resistance have been reduced with the new design and hence the tripler efficiency has been improved. Also, the use of InGaAs spacer layers to improve the effective barrier height [11, 12], reduces the conduction current and improves the elastance modulation ratio. This should improve the overall tripler performance.

VI. Acknowledgment

The authors would like to thank Emmanuil Choumas and Göran Reivall for their support during device fabrication.

References

[1] X. Mélique, C. M. Mann, P. Mounaix, J. Thornton, O. Vanbésien, F. Mollot, and D. Lippens, "5 mW and 5 % Efficiency 216 GHz InP-based Heterostructure Barrier Varactor Tripler," *IEEE Microwave and Guided Wave Letters*, vol. 8, pp. 384-386, 1998.

[2] J. R. Jones, W. L. Bishop, S. H. Jones, and G. B. Tait, "Planar Multi-Barrier 80/240 GHz Heterostructure Barrier Varactor Triplers," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 512-518, 1997.

[3] J. Stake, L. Dillner, S. H. Jones, C. M. Mann, J. Thornton, J. R. Jones, W. L. Bishop, and E. L. Kollberg, "Effects of Self-Heating on Planar Heterostructure Barrier Varactor Diodes," *IEEE Trans. on Electron Devices*, vol. 45, pp. 2298-2303, 1998.

[4] E. Lheurette, P. Mounaix, P. Salzenstein, F. Mollot, and D. Lippens, "High Performance InP-based Heterostructure Barrier Varactors in Single and Stack Configuration," *Electronics Letters*, vol. 32, pp. 1417-1418, 1996.

[5] J. G. Ruch and W. Fawcett, "Temperature Dependence of the Transport Properties of Gallium Arsenide Determined by a Monte Carlo Method," *J. Appl. Phys.*, vol. 41, pp. 3843-3849, 1970.

[6] J. T. Louhi, A. V. Räisänen, and N. R. Erickson, "Cooled Schottky Varactor Frequency Multipliers at Submillimeter Wavelengths," *IEEE Trans. on Microwave Theory and Techniques*, vol. 41, pp. 565-571, 1993.

[7] W. L. Bishop, K. McKiney, R. J. Mattauch, T. W. Crowe, and G. Green, "A Novel Whiskerless Schottky Diode for Millimeter and Submillimeter Wave Applications," presented at 1987 IEEE MTT-S International Microwave Symposium Digest, Las Vegas, 1987, pp. 607-610.

[8] P. A. Verlangieri, M. Kuznetsov, and M. V. Schneider, "Low-Resistance Ohmic Contacts for Microwave and Lightwave Devices," *IEEE Microwave and Guided Wave Letters*, vol. 1, pp. 51-53, 1991.

[9] S. M. Sze, "Carrier Transport Phenomena: mobility," in *Physics of Semiconductor Devices*, 2nd ed. Singapore: JOHN WILEY & SONS, 1981, pp. 27-38.

[10] J. R. Jones, S. H. Jones, and G. B. Tait, "Self-Consistent Physics-Based Numerical Device/Harmonic-Balance Circuit Analysis of Heterostructure Barrier Varactors Including Thermal Effects," presented at Sixth International Symposium on Space Terahertz Technology, Pasadena, California, 1995, pp. 423-441.

[11] J. R. Jones, S. H. Jones, and G. B. Tait, "GaAs/InGaAs/AlGaAs Heterostructure Barrier Varactors for Frequency Tripling," presented at Fifth International Symposium on Space Terahertz Technology, Ann Arbor, Michigan, 1994, pp. 497-513.

[12] V. Duez, X. Mélique, O. Vanbésien, P. Mounaix, F. Mollot, and D. Lippens, "High capacitance ratio with GaAs/InGaAs/AlAs heterostucture quantum well-barrier varactors," *Electronic Letters*, vol. 34, pp. 1860-1861, 1998.