HIGH Q InP-BASED VARACTOR DIODES

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Abstract **-We report on high quality-factor Heterostructure Barrier Varactor making benefit of epitaxial stacking and planar integration, with a cut-off frequency in the far infrared region. To this aim, high doping concentrations in the depletion (2x10 ^{17} cm^{-3}) and contact (1x10 ^{19}cm^{-3}) InGaAs regions lattice matched to an InP substrate and an InAlAs/AlAs blocking barrier scheme were used. Planar integration of the devices with a number of barriers up to eight in coplanar waveguide and series-type configurations shows a zero-bias capacitance of 3.4 fF/µm^2 per barrier and a conductance of 3.3 nS/µm^2 along with an intrinsic capacitance ratio of 4.3:1.**

Index terms **-Varactor diode, harmonic multiplier, heterostructure, substrate-transfer, InP**

I. INTRODUCTION

Recently, we reported record performances in terms of conversion efficiency (12.5%) and delivered power (9mW) for a waveguide Heterostructure Barrier Varactor tripler at 250 GHz [1]. These state-of-the art performances can be explained by the use of InP-based materials, which permit us to dramatically improve the voltage handling of the devices by reducing the leakage current [2] increasing by this fact the intrinsic quality factor of the devices. Also, the use of narrow gap cladding and contacting layers were found to be of great benefit in achieving a high modulation velocity of the depleted region [3] and for reducing the series resistance contribution to the cut-off frequency. In order to further increase these performances in terms of frequency and power capability, some improvements were subsequently brought to the epitaxial layers and to the technology aiming at (i) further increasing the current capability of the devices in the undepleted zone alleviating by this means the saturation effect at higher operation frequencies [3] and (ii) reducing the intrinsic series resistance through the use of highly-degenerated thick access and contact layers. In addition, the functionality of the device for a use as a medium-power high-frequency multiplier was improved with the fabrication of air-bridged devices in double and quadruple mesa configurations, with two barriers being stacked during epitaxy. This means that the overall number of elemental devices can be as high as eight. In this communication, we report on the dc and ac characterization of this new batch of

devices integrated in: planar coaxial schemes, coplanar waveguide (CPW) and planar series-type configurations.

II. TECHNOLOGICAL GUIDELINES

The epitaxial material used for fabricating the devices starting from a Semi-Insulating InP substrate, consists of: (i) a 1µm-thick $1x10^{19}$ cm^{-3} InGaAs buried layer, (ii) a 200nm-thick $2x10^{17}$ cm^{-3} InGaAs cladding layer, (iii) an undoped InAlAs-5nm/AlAs-3nm/InAlAs-5nm barrier, (iv) a 200nm-thick $2x10^{17}$ cm^{-3} InGaAs cladding layer and (v) a 500nm-thick $1x10^{19}$ cm^{-3} InGaAs capping layer. The Indium content is 53% and 52% for InGaAs and InAlAs respectively, whereas the strained AlAs layer was grown under pseudomorphic conditions. A two barrier-scheme, namely the series integration of two elemental diode structures during epitaxy, was grown without interruption. A higher doping concentration (twice that in previous work [4]) with thicker buried layers was chosen for this batch despite the difficulty to grow under lattice matching thick ternary InGaAs alloys. The epitaxial quality was found to be instrumental in order to achieve the high quality factor device. This fact explains why the AlAs layer thickness was kept at 3nm (3D growth was found for 5nm AlAs layers) hence, two barriers were integrated.

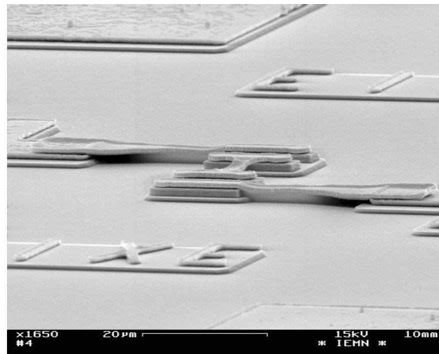

Figure 1: SEM view of an eight-barrier device. The air-bridges, 3µm-width, 40 µm-long and 0.8 µm-thick, were fabricated by photoresist molding techniques and electron gun evaporation.

III. INTEGRATION TECHNIQUES

The devices were fabricated for the realization of harmonic triplers at J band (220-325 GHz). Also a more prospective project targeting the integration of the diodes in a non-linear transmission line was investigated. With respect to these goals, it was decided to further integrate the devices by taking advantage of a planar integration in close proximity by low dimensional air-bridge connection. To this aim, advanced fabrication techniques were employed which consist in the writing of the micron-

sized dimension top contacts by electron beam (PMMA resist), the ohmic contact deposition by electron gun evaporation (a sequential Ni/Ge/Au/Ti/Au multilayer ohmic contact annealed by RTA at 400°C during 40 s), the etching of mesas by Reactive Ion Etching ($CH_4/H_2/Ar$ gases) and the fabrication of evaporated air-bridges using a double resist layer molding scheme. The underneath resist layer was pyrolized in order to achieve a convex mold shape and avoid resist mixing [5]. Figure 1 shows a Scanning Electron Micrograph of a completed device. For the present example, the number of barriers was eight (2 epitaxially $\times$ 4 mesas in series).

IV. DC AND AC MEASUREMENTS

For the characterization of the devices, we took advantage of various transmission line topologies. The outputs are the values of the small signal equivalent circuit, which permits one to subsequently simulate the large signal behavior of the devices under large signal conditions by a harmonic balance method. Also the electromagnetic (EM) behavior of the devices can be assessed using EM codes combined with network analysis through the use of scattering matrix [6]. The intrinsic elements, namely the level of conductance, which describes the leakage current through (tunneling effects) and over (thermionic emission) the barrier along with the intrinsic capacitance non-linearity, can be obtained using the coaxial type configuration (see Figure 5). Figure 2 shows the locus of the complex reflection coefficient versus frequency between 500 MHz and 40 GHz at zero-bias. A near pure capacitive behavior is apparent in this figure. The real part of the impedance was found to be as low as 0.8 Ω, irrespective of the applied bias.

@ 300K

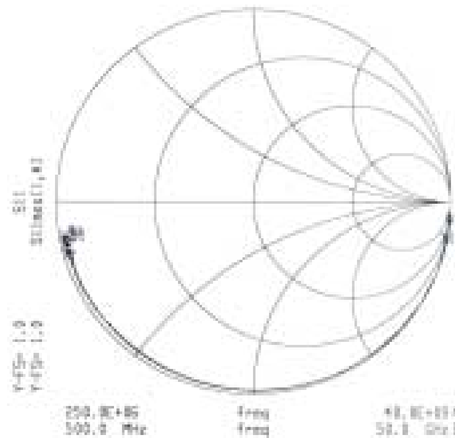

Figure 2: Plot on Smith chart of the frequency dependence of the reflection coefficient at zero-bias for a coaxial-type device configuration (∅ 20 µm).

These measurements can be used for investigating the intrinsic capacitance-voltage characteristics whose examples are shown in Figure 3. The devices exhibit an excellent symmetry with respect to the Y-axis. For this dual barrier scheme the zero-bias capacitance is 1.7 fF/µm^2. At 8V the capacitance reaches practically its saturation value of 0.39 fF/µm^2, yielding a capacitance ratio of 4.3:1. Concerning the leakage current, which is characterized by the conductance-voltage plot (also shown in Figure 3), we found a value of 1.37µS/µm^2 at the reference voltage of 6 V, which corresponds to an increase in the conduction mechanisms due to impact ionization in the 2×10^{17} cm^{-3} InGaAs (Eg =0.8 eV) cladding layer. The quality factors at 5 GHz are 20800 (0V), 2720 (2V), 80 (4V), 11(6V) respectively. By assuming a predominance of displacement current (J_D) for J_D/J_C= 10:1 (J_C being the leakage current) it is believed that the diode could operate correctly under a full 8V peak to peak pump voltage @ 250 GHz.

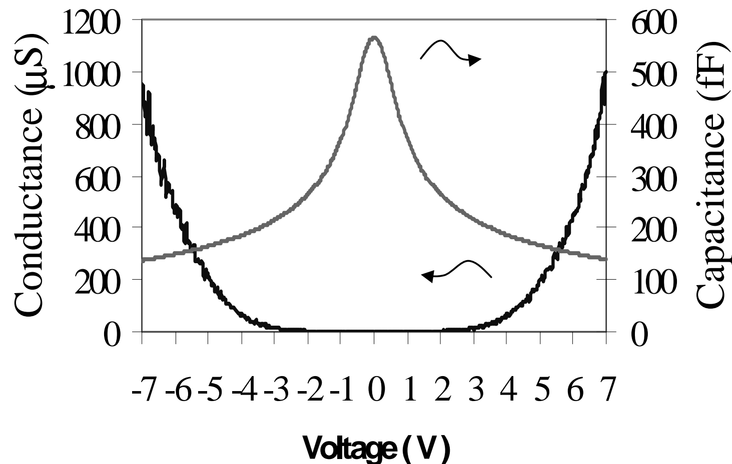

Figure 3: Measured capacitance and conductance-voltage characteristics for a two-barrier coaxial-type device (∅ 20 µm).

V. INFLUENCE OF DOPING CONCENTRATION

In order to have further insight into the capacitance-voltage relationship when the doping concentration is varied, we show in Figure 4 the simulated capacitance-voltage curves for a one barrier scheme. In order to obtain these data, we solved the Poisson equation in the Thomas-Fermi approximation. This means that the charges resulting from the leakage current are neglected (zero-current approximation). The electronic charges in the accumulation layer, which are trapped in front of the blocking barrier, can be calculated using a semi-classical distribution function.

Doping (cm^{-3})	1×10^{17}	2×10^{17}	4×10^{17}
C_0 ($fF/\mu m^2$)	2.6	3.25 (3.4)	3.6
Csat ($fF/\mu m^2$)	0.4	0.65 (0.78)	0.9
C_0/ Csat	6.5:1	5:1 (4.3:1)	4:1

Table 1: Summary of C-V characteristics in terms of zero-bias (C_0), capacitance saturation (C_{sat}) and capacitance ratio. The measured data are in brackets.

Further details on the assumptions and the numerical procedure can be found in ref [7]. A comparison between calculated and measured data (shown in brackets in table 1), for the 2×10^{17} cm^{-3} doping concentration, gives a satisfactory agreement and supports the validity of calculations. With respect to the trends, as a function of the doping concentration, it can be noted, as expected, that any increase in the donor concentration degrades the capacitance contrast with a concomitant increase in the capacitance level. However such a degradation is of minor importance in comparison with the associated benefit in terms of current capability.

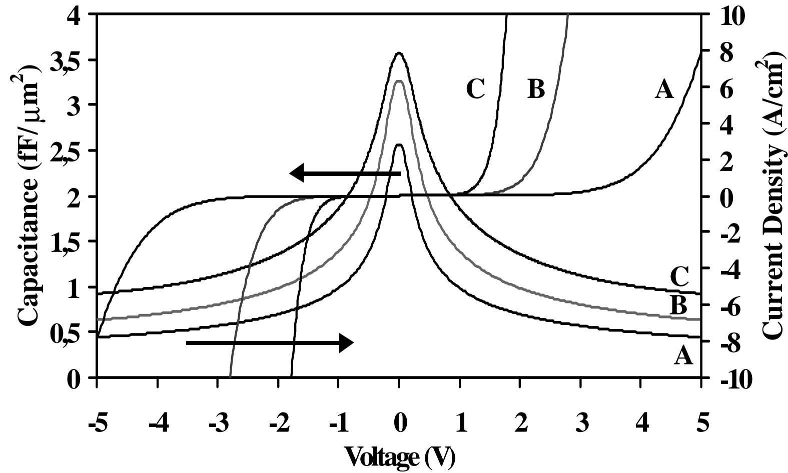

Figure 4: Simulated capacitance and current-density characteristics for different doping concentrations (single barrier), A=$1\times10^{17}cm^{-3}$ B=$2\times10^{17}cm^{-3}$, C=$4\times10^{17}cm^{-3}$.

From the leakage current point of view, a degradation of voltage handling can be observed. Therefore for a 8 A/cm^{-2} reference, the breakdown voltages are 5V (1×10^{17}), 2.8V (2×10^{17}) and 1.9V (4×10^{17}), respectively. Tunneling effects through the barrier are responsible for the leakage current at moderate voltages whereas the breakdown effect can be explained by impact ionization in the adjacent low gap layer. Increasing the doping concentration strengthens both leakage mechanisms via an increase in the Fermi level and the internal electric field in the InGaAs layer. On the basis of this study carried out on a single barrier device, which takes the doping concentration as a parameter, the benefit of epitaxial and/or planar stacking is quite

obvious by preserving the voltage handling of the device and a capacitance level which are compatible with high frequency operation. However, in order to alleviate the decrease in the capacitance ratio, it is believed that other routes have to be chosen, notably those involving planar doping or pre- and post-well configurations. In both cases, the basic idea is to shorten the screening length by accumulating electrons closer to the barrier (quantum well scheme or delta doped concentration). Both techniques have respective advantages and some conclusions can be found in ref [8] and [9].

VI. DE-EMBEDDING AND FURTHER IMPROVEMENTS

The capacitance variations can also be recorded for the CPW and series type configurations. For the latter, which have to be "flip-chip" mounted in the tripler blocks, there are no coplanar footprints for wafer probing of the devices, only pads. In this particular case, two of the three probes were used to contact the two pads facing each other. It can be shown that this kind of arrangement gives experimental data sufficiently accurate for de-embedding an equivalent circuit, which now takes into account, not only the intrinsic elements, but also the parasitics depending on the topology of the diodes.

These parasitics are the self-inductance and the pad-to-pad and bridge-to-pad capacitances, due to interconnections and the series resistance. A knowledge of these parameters is of prime importance for accessing the capability of the device for use in a tripler block, and for operating at very high frequency via the cut-off frequency. Ideally, special patterns have to be planned in the mask set to help in the derivation of parasitics. Notably a TLM pattern is generally set in the test field along with open-circuit (Cp) and air-bridged pads (Lp). Short-circuited devices yielded a self-inductance value in the 60 pH range for a single device whereas the capacitance parasitic value was found in the 20 fF range, with a large uncertainty due to the calibration and error measurements of reflection coefficients.

It can be shown, provided no extra resistive term was added, that the tripler efficiency is not affected by the reactive elements. This is true only for a perfect matching of the large signal admittance of the diode to the circuit, which is not always satisfied in practice. Improvements in the parasitics were demonstrated over the past through an optimized topology and/or the surface channel technology [10]. Deep etching was not performed here explaining why the parasitic capacitance is relatively high. This can be envisaged on the basis of Schottky technology carried out at the University of Lille [11] for which a post-process deep-etch was conducted, aimed at lowering the value of Cp.

Another key figure of merit is the series resistance. With respect to this specific issue, encouraging results were shown in Figure 2 with value as low as 0.8 Ω being observed. However, a major drawback associated with the planar integration of series type devices, instead of full epitaxial stacking, stems from an increase in the series resistance. The overall series resistance increases as the number of interconnected

devices increases, due to the combination of vertical and planar topologies. Reducing the total series resistance can be achieved by reducing the "spreading resistance", which is believed to be a major contribution towards r_s. There are currently two methods to achieve this goal : increasing the epitaxial thickness of the buried n+ layer [12] and/or increasing the doping density of this layer. In our current work, we kept the thickness to 1 μm since increasing this thickness to several microns is not technologically realistic using MBE growth, whilst we increased the doping density to $1x10^{19}$ cm^{-3}. We believe that the low value of the series resistance, which was observed in our measurements, is a direct consequence of the elevation of this doping density. Remembering that the n+ layer serves two purposes (i) ohmic contacts and (ii) mesa interconnect, another potential method is to introduce a transfer step [13]. Prior to this transfer, a gold layer can be deposited, this metallic layer can now function as the mesa-contacting layer. By these means we have greater control over the device topology. Therefore a quasi-vertical topology can be achieved. In the past such a scheme had been attempted by taking benefit of substrate-less technology [14]. However such a technology was found to be very difficult to fabricate practically whereas a transfer technique onto a host substrate could avoid most of the difficulties encountered with free standing membrane structures having post-metallization. In order to illustrate the advantages afforded by a substrate-transfer process onto a host quartz substrate, Figure 5 shows an SEM view and corresponding schematics of two transferred devices. In the type I configuration, the "spreading resistance" dominates the value of r_s, whereas in the type II configuration, a vertical current flow is preserved so that an improvement in the series resistance can be pointed out. Details of the technology of SU-8 grafting techniques and RF assessment can be found in [15].

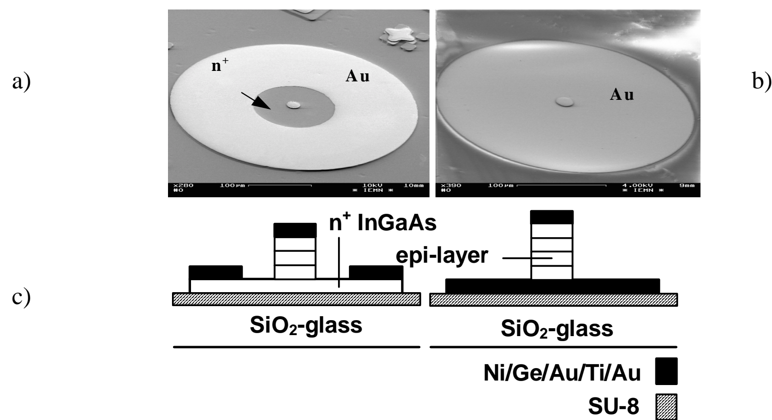

Figure 5: SEM view of various topologies of transferred HBV devices (a) **type I**: n^+mesa-contact, (b) **type II**: gold mesa-contact and (c) schematics of both topologies.

V. CONCLUSION

New degrees of freedom in the fabrication of high performance devices were afforded by epitaxial stacking and planar integration, which open the way to a full 3D integrated solid-state multiplier. The advantage of a series type connection was demonstrated with a zero-bias capacitance as low as 0.425 fF/μm^2 for a eight-barrier scheme, while preserving a capacitance ratio of 4.3:1.

A significant degradation of the series resistance (r_s) was noted for air-bridge contacted devices with respect to vertical devices which exhibit a record r_s as low as 0.8 Ω. Nevertheless it is believed that intrinsic cut-off frequencies in the far infrared region can be achieved owing to the drastic decrease in the capacitance level. High quality factors have been obtained together with a high power handling capability. A different device topology is also proposed, which could lead to a further reduction in the value of r_s. This has been made possible by using substrate-transfer techniques.

VI. ACKNOWLEDGMENTS

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