# Fabrication and Characterization of a 600 GHz Resonant Distributed SIS Junction for Fixed-tuned Waveguide Receiver

## Teruhiko Matsunaga<sup>1</sup>, Cheuk-yu Edward Tong<sup>2</sup>, Takashi Noguchi<sup>3</sup> and Raymond Blundell<sup>2</sup>

- Department of Astronomical Science, The Graduate University for Advanced Studies, Nobeyama, Minamimaki, Minamisaku, Nagano, 384-1305 Japan.
- 2 Harvard-Smithsonian Center for Astrophysics, 60 Garden St., Cambridge, MA 02138 USA.
- 3 Nobeyama Radio Observatory, Nobeyama, Minamimaki, Minamisaku, Nagano, 384-1305 Japan.

#### Abstract

The non-linear quasiparticle distributed tunnel current flowing in а superconductor-insulator-superconductor (SIS) transmission line resonator has been exploited in a low-noise heterodyne fixed-tuned waveguide receiver in the 600 GHz band. The mixer employs two half-wave or full-wave distributed SIS long junctions connected in series. These devices have been fabricated with optical lithography. Preliminary results show that a noise temperature of 240 K is routinely obtained at around 600 GHz. The best double-side-band receiver noise temperature measured so far is 161 K at 597 GHz. The achieved RF bandwidth is only about 5 % and the center frequency of the resonance is also shifted towards lower end of the target frequencies.

### I. Introduction

Distributed mixer based on the nonlinear quasi-particle tunnel current in a superconductor-insulator-superconductor (SIS) nonlinear transmission line requires a lower current density tunnel barrier, simpler matching circuitry, and lower magnetic field to operate when compared with conventional lumped-element SIS mixers. Waveguide receivers incorporating such long SIS junctions have demonstrated quite wide bandwidth, very low noise temperatures at submillimeter wavelengths [1][2]. However, the widths of these junctions have to be submicron to achieve reasonably high impedance for ease of matching. Consequently, they have to be fabricated using electron beam lithography [3] or with edge junction technique [4].

In standard fabrication process with optical lithography, the junction area is commonly defined through square or round resist stencils. In order to fabricate long distributed

junctions, long, narrow stencils are required. Such geometry is not ideal from the point of view of fabrication process, in particular the reactive ion etching steps. Damaged stencils result in too large variation of the individual junction size over a wafer. In addition, the lift-off process after SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> sputter deposition is difficult or even not possible at very narrow line widths. In this work, we have experimented with wider (> 1  $\mu$ m) and shorter (= $\lambda_g$ ,  $\lambda_g/2$ ) SIS transmission lines. This type of resonant distributed mixer was proposed by Belitsky [5] and a quasi-optical version of it has been tested by Uzawa [6].

To achieve good matching between the waveguide embedding circuit and such a large distributed junction, we employ 2 resonant junctions connected in series, each with its own quarter-wave transformer section. This design allows for a lower circuit embedding impedance. Also the IF capacitance is reduced by half. The details of fabricated and laboratory test data will be presented below.

#### II. Non linear transmission line resonator mixer design

The characteristic impedance of our 1.4  $\mu$ m wide non-linear transmission line is only about 1  $\Omega$ . At its half-wave resonant and full-wave resonant frequencies, the input resistance becomes reasonably large and the reactance vanishes. Fig. 1 shows the theoretical [7] input impedance at 660 GHz as a function of the length of the resonator. Note that the resonance structures are clearly observed.

A waveguide horn couples the RF radiation to the waveguide and mixer chip. Fig.2 illustrates the layout of the mixer design, and Fig. 3 is an SEM photograph of a single SIS long junction. Two types of resonant long junctions have been designed: the 5.7  $\mu$ m long half-wave resonator (labeled HWR) and the 11.4  $\mu$ m long full-wave resonator (labeled FWR). The nominal junction width is 1.4  $\mu$ m. Two series connected resonator junctions are each integrated with a quarter-wave transformer. This arrangement has a dual purpose. First, it halves the IF output capacitance. Thus, the output capacitance of a HWR chip is about 0.4 pF and that of an FWR chip is about 0.8 pF. Secondly, the embedding impedance seen by each device is reduced. We need only to match each resonator to an impedance of about 20  $\Omega$ . We have incorporated a quarter-wave transformer with a characteristic impedance of 8  $\Omega$  on the HWR chip and 6  $\Omega$  for the FWR chip.

#### III. Junction Fabrication

The Nb/AlO<sub>X</sub>-Al/Nb tunnel junction was fabricated using standard SNEP (Selective Niobium Etching Process) incorporating the anodization technique [8]. The processing

steps are illustrated in Fig. 4.

Waveguide mixer elements for high frequencies require substrate materials with low dielectric constants and low absorption. Therefore crystalline quartz substrates are used. The fabrication of the SIS mixer circuit starts with the deposition of a Nb/AlO<sub>X</sub>-Al/Nb tri-layer in a photoresist mask defining the low-pass filter for the IF output. The base Nb layer is 200 nm thick. The film stress was measured [9] using the film on an extra wafer processed in same batch and it is adjusted to about  $0.5 \pm 0.1$  GPa to achieve high quality (subgap to normal resistance ratio, R<sub>SG</sub>/R<sub>N</sub>~20) SIS junction. The measured stress of films is shown in Fig. 5. Just after the deposition of the base layer, a 6 - 8 nm thick Al film is sputtered in same chamber. The oxidation of the Al film is performed in the load-lock chamber with 53 mTorr Ar +  $10\%O_2$  for 30 min. The target critical current density is 7.5 kA/cm<sup>2</sup>. Then 100 nm thick Nb counter electrode is deposited. After the lift-off of the photoresist, 75 nm SiO<sub>2</sub> is deposited on the whole wafer to protect the surface of the Nb counter electrode from being oxidized in the later anodization process. For the definition of the junctions, first lines are patterned on top of the tri-layer using positive resist ip3100HS [10] and the Canon PLA501 contact mask aligner operating Deep-UV. Then the unprotected parts of the SiO2 and counter Nb film are etched away to obtain the long junctions. In order to avoid short-current at the junction edges, periphery of the junctions are anodized, followed by the deposition a 270 nm SiO<sub>2</sub> and a 90 nm Al<sub>2</sub>O<sub>3</sub>. After lifting off the resist, the SiO<sub>2</sub> layer is removed, and exposed area of the top Nb electrode is etched with 1.5 Pa Ar plasma for 4.5 min. Finally, the wiring Nb layer was deposited and patterned and, a gold layer was evaporated by e-beam deposition to provide good contact pads for the IF port and ground.

#### IV. Receiver noise measurement

The mixer chip is installed in a fixed-tuned waveguide mixer block developed for the Sub-Millimeter Array [1]. For laboratory noise temperature measurements, we have employed a liquid helium cryostat. The measurement setup, as shown in Fig. 6, is identical to what was previously described by Tong [8]. The IF is 1.5 GHz. Local oscillator power is provided by a cascade of solid-state multipliers pumped by a Gunn oscillator. The LO beam is collimated by a 90 degree off-axis parabolic mirror. A Martin-Puplett interferometer provides LO and signal diplexing. The beam reflected off the paraboloid passes through several layers of infrared blocking filters, made from porous Teflon sheet, at 77 K and 4.2 K, is then focused on the mixer feed using a parabolic mirror.

The heterodyne receiver noise measurements were made using the standard Y-factor method for room temperature (295 K) and liquid-nitrogen-cooled (77 K) loads. Double-side-band noise temperature is computed from the experimental Y-factor with no correction for Planck's radiation law.

#### V. Results and Discussion

Using resistance data from large (5.0, 3.0, 2.0, 1.75 and 1.5  $\mu$ m square) junctions fabricated on same wafer, the current density of the barrier is determined to be about 7.0 kA/cm<sup>2</sup>, which is close to the design value. The subgap to normal state resistance ratio (R<sub>SG</sub>/R<sub>N</sub>) is typically > 15. Fig. 7 shows a typical I-V curve of a full-wave long junction (nominally 1.5  $\mu$ m x 10.8  $\mu$ m= 16.2  $\mu$ m<sup>2</sup>), together with its measured heterodyne response at 579 GHz to hot and cold loads. From the normal state resistance of this device of 3.98  $\Omega$ , we infer that junction size is 13.6  $\mu$ m<sup>2</sup>. This means that there is a difference of around 0.22  $\mu$ m in both length and width of device compared with the design values. At a bias voltage of 3.8 mV, a Y-factor of 1.72 is obtained. This corresponds to a double-side-band receiver noise temperature of 226 K.

A number of chips have been tested. A noise temperature of 240 K is routinely obtained at around 600 GHz. The measured noise temperature as a function of LO frequency is plotted in Fig. 7 for both an HWR and a FWR chip. When the helium bath temperature is lowered to 2.5 K, the receiver noise temperature is reduced by about 100 K. The lowest noise temperatures measured at 2.5 K is 161 K at 597 GHz. The double sideband conversion loss corresponding to the lowest receiver noise point are estimated to be  $8 \pm 2$ dB and  $7 \pm 2$  dB, for the half and full wave resonators, respectively. The IF-amplifier noise temperature is around 5 K.

The achieved RF bandwidth of all measured devices is only about 5 % that is around 30 GHz. The center frequency of the resonance is also shifted by about 10 % toward the lower end of the target frequencies. We believe that the frequency shift and the narrow RF bandwidth are result of the undersized junctions; we estimate 0.22  $\mu$ m of shrinkage for a nominally 1.4  $\mu$ m design. The measurement setup can also be improved to give better sensitivity toward the higher end of the frequency band.

#### VI. Conclusion

Preliminary tests have been made on a distributed superconductor-insulator-superconductor (SIS) resonant mixer in a fixed-tuned waveguide

mount in the 600 GHz band. The best double-side-band receiver noise temperature measured so far is 161 K at 597 GHz. However, the achieved RF bandwidth of every measured device is only about 5 % (that is about 30 GHz) and the center frequency of the resonance is also shifted 10 % (that is around 60 GHz) towards lower frequencies. These effects are caused by impedance mismatch between waveguide and the junctions, because the design parameters are slightly different, and because the resonator width was shrunk by about 0.22  $\mu$ m during fabrication process, especially photolithography and RIE. We are currently working on a second batch of devices designed with parameters extracted from the measurement data.

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## VIII. References

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Fig. 1 Calculated real and imaginary parts of the input impedance of a 1.4  $\mu$ m wide open-ended SIS transmission line. Note that around integer multiples of  $\lambda_g/2$  (6  $\mu$ m in this case), the reactance vanishes and the resistive part becomes larger.

		HWR	FWR
Transformer	Width [µm]	9.0	14.0
	Length [µm]	36.5	36.5
Junction	Width [µm]	1.4±0.2	1.4±0.2
	Length [µm]	5.1±0.3	11.4±0.3

Table 1 Size of sections in a mixer.



Fig. 2 Layout of the resonant SIS mixer chips.



Fig. 3 SEM photograph of a full wave resonant distributed SIS quasiparticle tunnel junction.



1. Base Electrode Patterning



2. Tri-layer Deposition



3. Lift-off & SiO2 Deposition



4. Junction Patterning



 Counter Electrode Etching & Anodization



6. SiO2 & Al2O3 Deposition



7. Lift-off, SiO2 Etching& Wiring Layer Deposition



8. Wiring Layer Patterning



9. Wiring Layer Etching & Resist Remove



Fig. 4 Fabrication steps for SIS tunnel junction with Selective Niobium Etching Process (Selective Niobium Etching Process) incorporating with the anodization technique.



Fig. 5 SIS quality factor,  $R_{SG}/R_N$ , as a function of internal stress of base Nb film. Minus sign represents compressive stress. Thin film with about 0.5 GPa compressive stress gives relatively high quality junctions.



Fig. 6 Layout of receiver experiment. The mixer assembly, parabolic mirror and HEMT amplifier are mounted on the 4.2 K-cold plate.



Fig. 7 DC current-voltage characteristics of the resonance distributed SIS junction mixer without and with incident LO power at 579 GHz. Also shown is the receiver IF output power as a function bias voltage for hot and cold loads. A Y-factor of 1.72 is noted at a bias voltage of 3.8 mV.



Fig. 8 DSB noise temperature as a function of frequency. Results are shown for FWR ( $\lambda_g$ ) and HWR ( $\lambda_g/2$ ) resonator length mixer noise temperature at 2.5 K and 4.2 K, respectively.



Fig. 9 Simulated conversion gain of resonant SIS mixer. Note that the center frequency changes with the junction width because of changes in the capacitance of the non-linear transmission line.