1500 GHz Tunable Source Using Cascaded Planar Frequency Doublers

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Abstract

A complete source for 1.5 THz has been built using a cascade of four planar doublers following a MMIC based HEMT power amplifier. This driver is in turn driven by a times nine multiplier so that the complete source may be synthesizer controlled. The source is intended for use at 120 K and has been tested at 60-90 K. The peak output powers of the stages are: first stage 53 mW, second stage 15 mW, third stage 2.0 mW and final stage 45 μW. The peak output was measured at 1484 GHz, although >1 μW is produced over the frequency range 1450-1620 GHz. Based on preliminary testing with lower power, it is expected that a power of 1 μW is sufficient to drive an HEB mixer.

Introduction

The heterodyne instrument on the Herschel (FIRST) space observatory will cover frequencies from 500 to 1900 GHz, presenting very demanding requirements on LO sources. The most challenging requirement is at the highest frequencies where LO sources with power >1 μW are needed in the 1.4-1.9 THz range with 10% tuning bandwidth. For best reliability, the source must use all-planar components with no mechanical tuning. While initially this appeared to be a very ambitious goal, planar diode technology has recently evolved to the point where this is possible. At this time, diode fabrication is relatively consistent, and multiplier designs work very well at nearly all required frequencies. Fairly complex circuits can be fabricated monolithically, on GaAs of any needed thickness. Efficiencies of many multipliers actually exceed expectations, and the operating bandwidth is near the goal. This paper describes a chain for 1.5 THz with sufficient output power over a 10% band to meet the system goal, although work remains to make this an optimal source. The entire LO system for Herschel is intended to be operated at a temperature of 120 K, so most of the data is measured at low temperatures.

The source uses a cascaded chain of four passive doublers (net x16 multiplication), with a high power driver in the 100 GHz range. The initial stage of the driver is a x9 multiplication to 89-106 GHz band, which is followed by amplification to a typical power of 150 mW. The power amplifiers are GaAs MMIC's fabricated at TRW, and assembled into waveguide housings at UMass and JPL. The driver is a synthesizer or sweeper in the 10-12 GHz range, so frequency control is quite simple.

All of the final four doublers are balanced designs using planar diode arrays. The number and size of diodes used in each doubler depends on the required input power level. Most of these doublers have been described previously, but current results are better than previously reported and the full cascade of stages is entirely new.

First stage doubler

The doubler for 200 GHz was built at UMass using a 6 diode array. This doubler has been described previously [1,2,5], and is a balanced design using a diode array which is soldered in place, as shown in figure 1. The bias circuit is decoupled from the output with just a beam lead planar capacitor using a SiN film, and the diode is coupled to the output with a gold bond wire. The design bandwidth is 188-212 GHz output with a flat response, and the circuit seems to work well across this full band, as shown in figure 2. The optimum input power for this doubler is 150-180 mW. Limited input power at the highest frequencies causes the data be scattered, but the points with optimum drive show nearly constant efficiency. There is a substantial advantage to operating this doubler at low temperature as seen in the efficiency vs temperature curve of figure 3. The diodes use an epitaxial layer doping of $1x10^{17}/cm^3$, which gives a significant increase in carrier mobility at lower temperature, leading to lower series resistance and a 60% increase in efficiency at 80 K. At the expected operating temperature of 120 K, the efficiency should be 33%. Power was measured at all frequencies using a waveguide calorimeter having very flat frequency response from 75-2000 GHz [3,4].

A comparable design built at JPL uses beam leads rather than solder joints to mount the diode, and a bias structure which is fully integrated with the diodes. This integrated doubler appears to work about the same as the discrete design, although data is not quite as complete on this unit. This style of construction is preferred due to its easier and more repeatable assembly. However, the beam leads do lead to a larger temperature rise for the diodes.

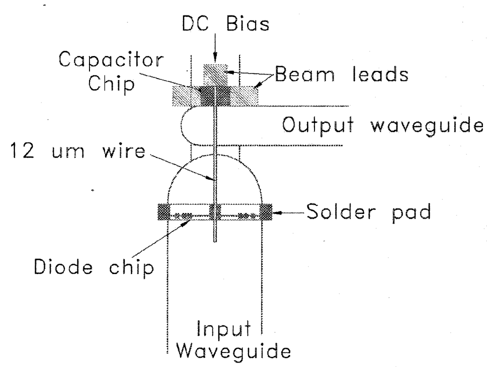


Figure 1. Schematic of the 200 GHz doubler showing just the inner region of the block. Outside of this area, waveguide steps provide the required wideband matching.

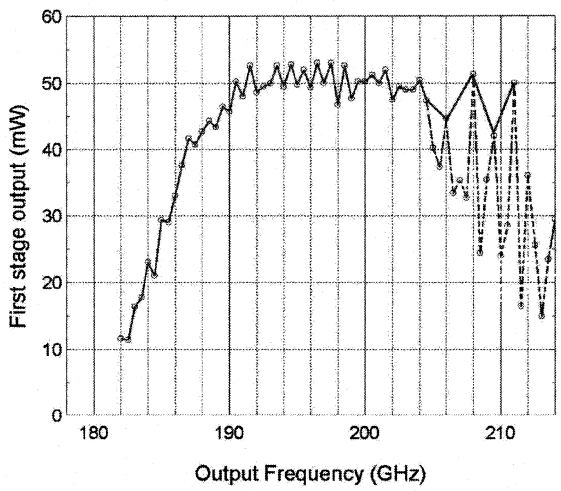


Figure 2. Output power of the first stage at 80 K with 140 mW input (up to 204 GHz). The source power is too low for points on the dashed line, and only points on the solid line have 140 mW input.

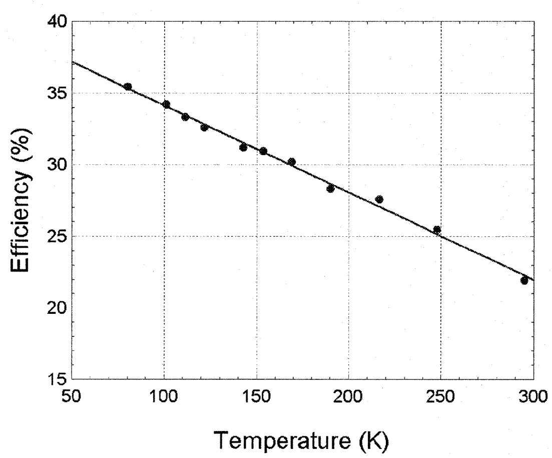


Figure 3. Efficiency of the 200 GHz doubler as a function of temperature.

Second Stage Doubler

The doubler for 400 GHz was designed and assembled at JPL using a 4 anode planar array. In concept it is identical to the 200 GHz doubler, but with a higher level of integration. The design is one with minimal substrate, consisting mostly of suspended metal with beam leads for mounting and grounding. It has been described previously [5]. The installation requires no soldering, or any difficult assembly. As with the 200 GHz doubler, the diode chip is quite simple, and much of the impedance matching over a wide band is done with machined waveguide steps. The view of one block with the diode installed is shown in figure 4.

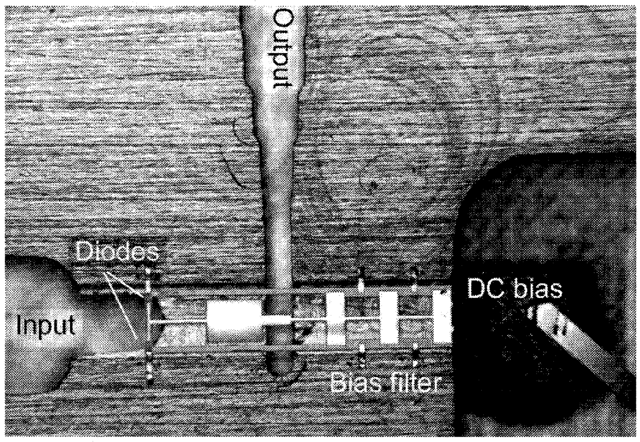


Figure 4. Internal assembly of 400 GHz doubler, using "substrateless" design.

This doubler was tested with drive from the 200 GHz doubler, with no isolator between stages. While isolators for this band are practical, and are planned for eventual use, one was not yet available suitable for vacuum operation at the needed power level. The resultant power vs frequency, shown in figure 5, shows a lot of ripple, which is likely to be mostly due to the interaction between stages. The room temperature efficiency is 16% and the 80 K efficiency is estimated to be 24%, with a diode epilayer doping of $2x10^{17}$. This doubler appears to be tuned a bit lower than its nominal design band of 375-425 GHz, and this is a typical problem with many multipliers designed for this work. Most of the effects of actual device fabrication seem to shift the frequency lower than the idealized models used for design purposes. No designs so far have been tuned high.

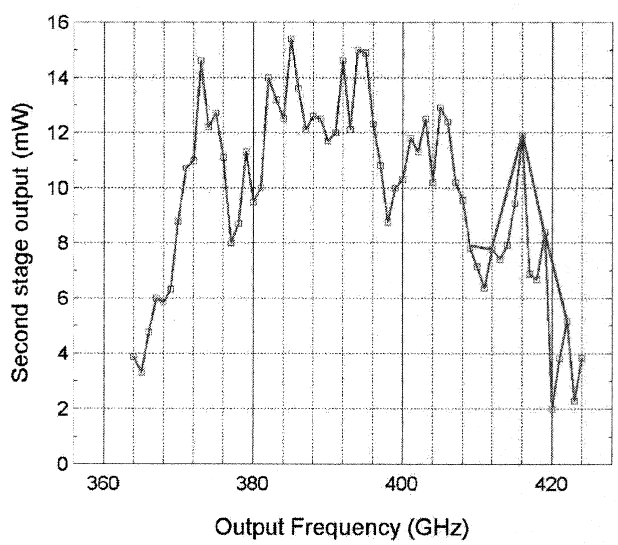


Figure 5. Output power of first two cascaded stages at 80 K. Input power to first stage is 140 mW below 408 GHz output. Above this frequency, only the upper curve has 140 mW input. No isolator is used between stages.

Third stage doubler (800 GHz)

The doubler for 800 GHz was designed at UMass with diodes fabricated at JPL. It is a balanced design as at lower frequencies, but just a pair of diodes is used, since the required power level is quite low. The diodes have a capacitance of 4.3 fF, which should be able to handle (as a pair) up to 10 mW input with a peak junction voltage below their 5.5 V breakdown. The previous stage works somewhat better than expected and its output exceeds this power by ~2 dB at some frequencies. The doubler chip is a very compact circuit on 12 μm thick GaAs, and uses beam leads for grounding the diodes and the bias bypass capacitor. The substrate is narrowed between the input and output waveguides to eliminate higher modes, which can cause a large difference in the coupling of the two diodes to the output waveguide. The circuit is simple to assemble except that diode chip is quite small, as can be seen in figure 6. Handling the chip is difficult because there is little GaAs that can be touched and the 1 μm thick beam leads are too fragile to pick up with tweezers. However, they can be picked up by simply touching a probe to them, and generally they stick. The diode is not attached to the block anywhere except at the bias terminal. This lead is connected to the bias circuit and the remaining beam leads are just clamped between the halves of the block. As with the other doublers the simple diode circuit is supplemented with waveguide steps to increase the bandwidth.

The output waveguide where the diode crosses is only 36 μm high, which is too small to cut with an end mill, so this waveguide was broached (scraped) with a tool having just the 36 μm width. This tool was ramped out of the block at a steep angle at the end of the cut to form the integral backshort. All other features were cut with end mills. All of the machining was done on an NC micromill [6].

A waveguide diagonal horn is integral to output of the doubler, since initial testing was to be of this as a final stage, and the waveguide seemed too small to flange reliably. This horn is an obstacle to using this as a driver for a following stage, but the horn may be eliminated for future use.

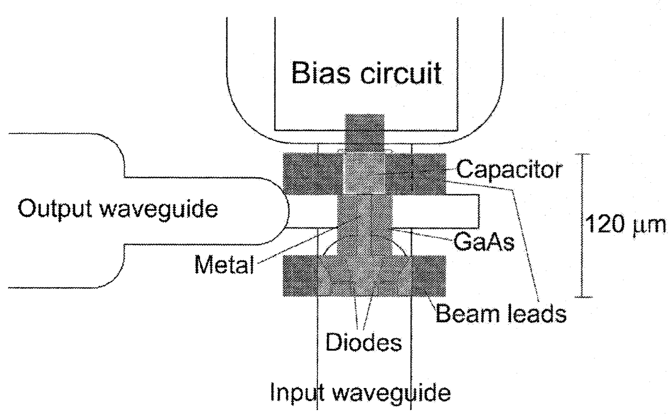


Figure 6. Cross section of 800 GHz doubler.

The output of these three cascaded stages is shown in figure 7, for room temperature and 80 K operation. There is more ripple than for the 400 GHz driver, and the ratio of maxima to minima is larger. In addition, this doubler, too, is tuned lower than designed, since it is intended to work from 780-860 GHz. The apparent tuning error is ~30 GHz, only a 3-4% shift relative to the design, but one that must be understood and corrected. The typical bias voltage is 1.5-2.5 V (reverse), with no systematic frequency dependence, and the bias current is very small.

The very large change in output power with cooling is mostly due to the change in input power, which may increase a factor of 2.4. The efficiency of this doubler is relatively temperature insensitive. The cold efficiency is about 11%, while at room temperature it is ~10%. The diode doping is 3×10^{17} which leads to minimal temperature dependence to the mobility. However, the efficiency rises with input power when it is underdriven, accounting for the very large increase in power at the higher frequencies at low temperature. It is notable that the maximum output power is ~20 times larger than that available at comparable frequencies using whisker contacted triplers, which were the best previously available multiplier technology.

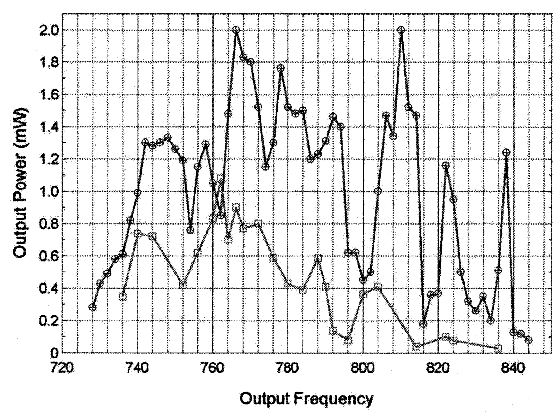
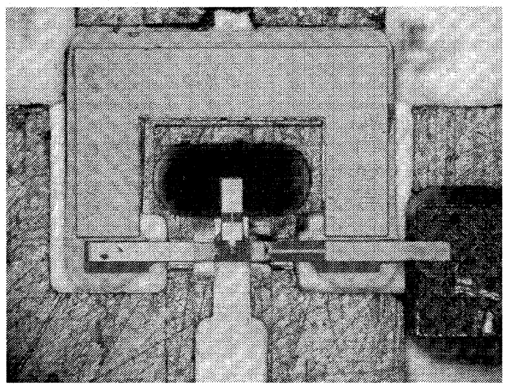


Figure 7. Output power of 3 cascaded stages at room temp (upper) and 80 K (lower). Input power for the cold data is 140 mW below 816 GHz. Input power at room temperature is 160 mW below 790 GHz. At higher frequencies input power may be significantly lower.

Fourth stage doubler (1.5 THz)

The 1.5 THz doubler uses a balanced design in a resistive mode. The circuits used in the lower frequency stages are not easily extended to this frequency because of the need to machine very low height output waveguide. However an alternate circuit geometry puts the diodes in series in the output waveguide, with a coupling probe to the full height input waveguide. The diodes may then be biased in series via an extension of the substrate and a SiN bias bypass capacitor. The circuit layout is shown in Figure 8. The overall diode construction uses a framed design with 50 μm thick frame and 3 μm substrate for active part of the circuit. This design has been described previously in preliminary tests with a laser pump [7].



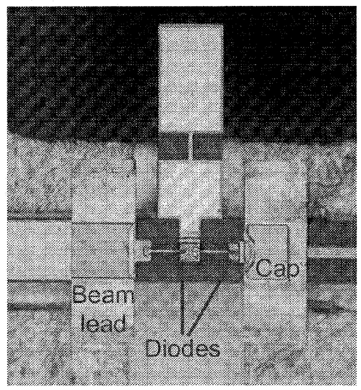


Figure 8. Overall view of the 1.5 THz doubler showing the frame and input waveguide, and detail showing just the electrically important part of the circuit.

The doubler is very easy to assemble, but the frame complicates the machining, because the input waveguide must plunge directly through the block. This waveguide does not need to be very long because a conical waveguide horn is integral to the input, and can be machined from the other side of the block. This block was designed for tests with a laser driver, before the complete chain was complete, so an input horn was desired. This horn has approximately the same dimensions as that on the 800 GHz doubler so coupling between them can be fairly good. although higher modes can also cause a large variation in coupling.

The complete four stage chain was tested at 60K over a wide band, and at room temperature over a more limited band. The chain as used at room temperature is shown in Figure 9. The setup for cold tests placed much of the chain at room temperature and just the final power amp stage and the four doublers at low temperature, as shown in Figure 10. In order to eliminate a lossy vacuum window on the output, the THz power sensor was placed inside the dewar, although it was maintained near room temperature through the use of an isolating section of stainless steel waveguide

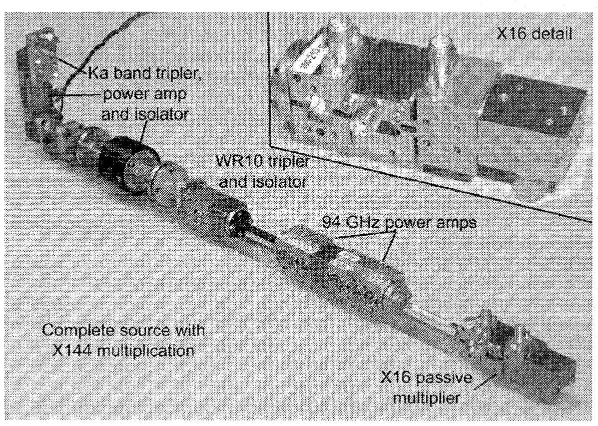


Figure 9. Complete source with x144 multiplication, using x9 stage followed by power amps and a x16 passive multiplier. The output is a small diagonal feed horn which points upward.

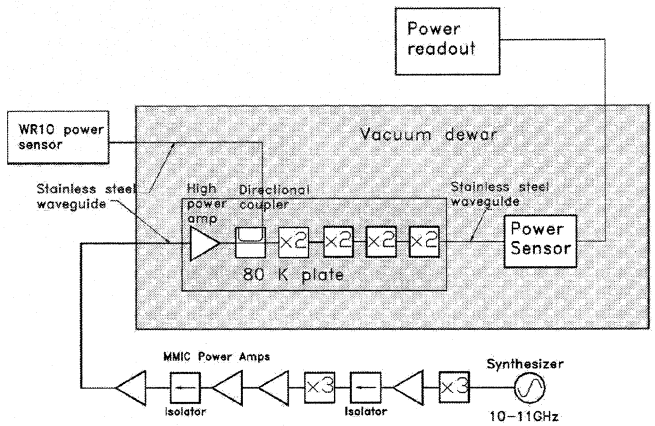


Figure 10. Setup for testing the complete X16 chain cold. Placing the power sensor in vacuum (at room temperature) eliminates the need for a window at 1.5 THz.

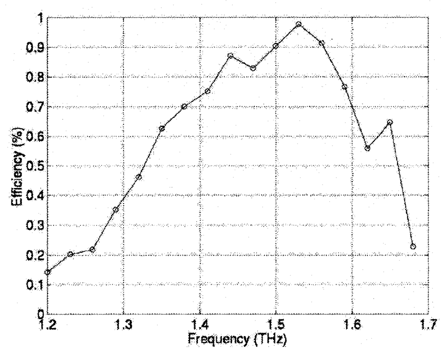


Figure 11. Predicted efficiency vs. frequency for the 1.5 THz doubler.

The predicted frequency response of the doubler is shown in Figure 11. The actual output power is shown in Figure 12, although this is convolved with a widely varying input power, making interpretation of the data difficult. One problem is the inherent variation in input power shown in Figure 7, but in addition, the horn-to-horn coupling adds a great deal of additional ripple due to mode conversion at some frequencies. It appears that this doubler does work at nearly the predicted frequency band, rolling off just 50 GHz lower than expected, but there is no data at low frequencies to show what happens. A few points were added using a different first stage doubler with lower tuning but this did not properly overlap the tuning of the first. This extended the range only slightly before the following stages began to roll off. Even with these problems we still can get >1 μW output power over 150 GHz, and the data sampling with 4 GHz spacing is equivalent to full coverage for the Herschel IF bandwidth of 4 GHz. Room temperature data is much more limited because of low input power, but still up to 10 μW can be obtained, making this a useful source for mixer testing. There is no good way to measure the efficiency either at room temperature or cold. It is impossible to know the true available power from the driver, or the interactions between two nonlinear devices. However, the cold efficiency, corrected for input mismatch, must be ~1-2%, given the peak driver stage output of 2 mW, and the maximum cold output peaks of 20-45 μW. Room temperature efficiency is not expected to be much different given the high diode doping of 5×10^{17}, and almost no temperature dependence to the mobility.

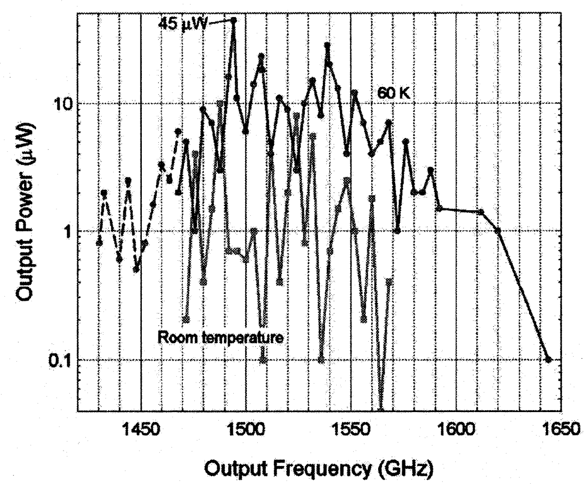


Figure 11. X16 output power with 160 mW into first stage. Upper data is at 60 K, lower data is at room temperature. Data on the dashed curve uses a different first stage doubler, but the same following stages.

HEB mixers are supposed to operate on extremely low LO power, and the Herschel specification is 1 μW for each mixer. There has been little data to support this, so this source was used to pump an HEB mixer at JPL. At the time of the test, the third stage doubler had not been optimized, so the source produced only 0.2 μW output, which pumped the mixer to within about a factor of two of the needed power. The IV curve of the mixer is shown in Figure 12 for this low power. No data was obtained with the higher power source in time for this paper, but there seems to be little doubt that with proper coupling the present power should easily drive the mixer at any frequency.

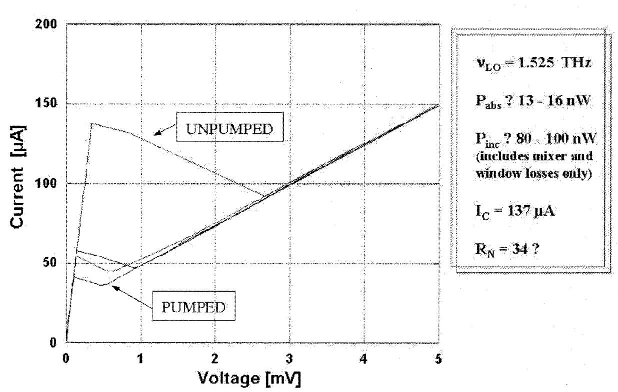


Figure 12. HEB mixer test at JPL with preliminary source with ~0.2 μW output.

Conclusions

A complete source has been built for 1.5 THz using a cascade of extremely high performance doublers. The output power of 45 μW is a record high for a solid state source at any nearby frequency. All of the stages work as well or better than expectations and the output power is sufficient to drive an HEB mixer over a wide band. All multipliers survive cooling to 60 K without problems and all work as well or better than at room temperature. The performance of this chain indicates that even higher frequency sources such as one at 1.9 THz as required for Herschel should be quite practical. The primary technical challenge at this point is getting the multipliers to work precisely at the needed frequency. All of the bands for Herschel are only 10-12% in fractional bandwidth, and at this time the tuning error for a given stage appears to be as much as 3-4%, although test data are not as complete as are needed for full diagnostic purposes.

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