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PROGRESS IN SIS DEVICE FABRICATION FOR HIFI MIXER BAND 2 AT KOSMA

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ABSTRACT

We present our progress in device fabrication of Nb–AlO_x–Nb junctions embedded into low-loss tuning circuits. These integrated tuning circuits include a NbTiN ground plane and aluminum or niobium as top conductor materials. The junctions are defined by electron beam lithography down to areas of 0.4 μm^2. Instead of a lift-off process we use Chemical Mechanical Polishing (CMP) of the SiO_2 dielectric insulation to contact the junction top electrode.

Dipstick I/V measurements of devices with R_NA products around 15 $\Omega\mu m^2$ show a significantly higher gap voltage as compared to previously UV lithography / lift-off defined devices using otherwise identical fabrication parameters.

I. INTRODUCTION

Our goal is to develop the HIFI Band 2 SIS mixer for the Herschel Space Observatory [1]. The performance goals for HIFI are a mixer fractional bandwidth of 22 %, while complying to the mixer noise temperature specs of 110 K – 130 K (DSB) in the allocated frequency band between 638 GHz and 802 GHz. This corresponds to roughly only seven times the quantum limit $h\nu/2k$. Standard all-Nb devices cannot provide this performance above the Nb gap frequency of $2\Delta/h \approx 700$ GHz, so a low-loss tuning circuit material above the Nb gap has to be used. Although all-normal-conductor material tuning electrodes consisting of Al yield good-performance devices above 800 GHz [2], circuit simulations show that it is necessary to use an even lower-loss, superconducting, material especially for the low end of the targeted frequency band [3].

Because the fabrication of the Nb–AlO_x–Nb material combination is well-established and yields highly reproducible and high-quality tunnel junctions and the fact that the top of our frequency band is well below their theoretical mixing limit $4\Delta/h \approx$ 1400 GHz, our device design and fabrication baseline is to embed Nb–AlO_x–Nb junctions into a integrated tuning circuit with a NbTiN base and Nb or Al top electrode.

As NbTiN is the current choice for superconducting material above the Nb gap frequency, NbTiN thin film deposition techniques have been established for our junction fabrication and already have been integrated into HIFI Band 2 mixer fabrication in the past [4].

In order to achieve the performance goal the reproducibility of sub-micrometer-sized junction areas is the most critical fabrication parameter. Past mixer results and subsequent analysis show that a photolithographic defined junction area is not reproducible enough for HIFI Band 2 device development as a relative area reproducibility

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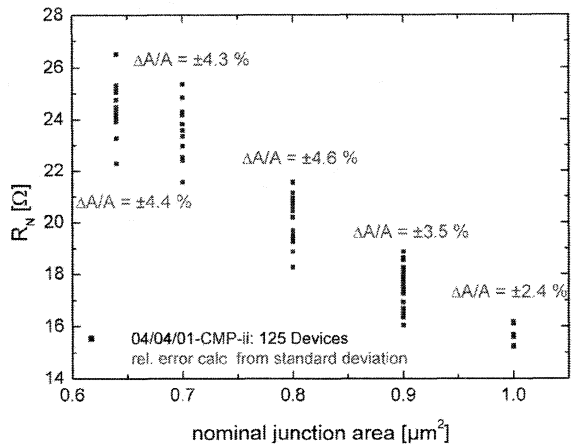

Fig. 1: Junction area reproducibility of simple Nb–AlO_x–Nb devices fabricated with our EBL / CMP process

$\Delta A/A < 10$ % (band center position) for junction areas of 0.5 μm^2 (RF matching) is required. Therefore we have integrated our electron beam lithography (EBL) / Chemical Mechanical Planarization (CMP) process scheme, which we developed in parallel for all-Nb devices, into junction fabrication for HIFI Band 2 mixer [5]. This process has proven its superior junction definition quality in the past yielding an area reproducibility complying to above design rule (Fig. 1).

We have decided to use EBL for junction definition while staying with standard photolithography for the likewise critical definition of the integrated top tuning electrode. We choose to do this because we encountered difficulties in achieving good RF performance of all-Nb mixers with the dual EBL and CMP process. We were able to trace the cause back to a resist related contamination problem during deposition of the integrated tuning top electrode. Good mixer results with photolithographic defined top tuning electrode reassured us that there is no inherent problem with our EBL / CMP process.

In this paper we present the current status of HIFI device fabrication at KOSMA and the advantages of the EBL / CMP process in comparison to our prior purely photolithographically defined batches.

II. Device Fabrication

Fabrication begins with the UV300 mask aligner definition of bilayer AZ7212 photoresist window structures on a 25 mm diameter and 285 μm thick INFRASIL fused quartz substrate. Through sputter-deposition of the metallization layer stack and subsequent lift-off these windows define the first half of the RF-blocking filter and waveguide-probe, the integrated tuning bottom electrode and the EBL alignment marks. The metallization consists of 350 nm NbTiN (tuning base electrode), 10 nm Au (diffusion barrier for the nitrogen and RIE etch stop, [6]), 100 nm Nb 1 (junction base electrode), 8 nm Al (for the AlO_x tunnel barrier) and 100 nm Nb 2 (junction top electrode) (Fig. 2). The Al layer is in-situ oxidized in the load-lock in a static pure oxygen atmosphere at 1.6 Pa using the Pa·s relationship [7] yielding a R_NA product of approximately 15 $\Omega\mu m^2$.

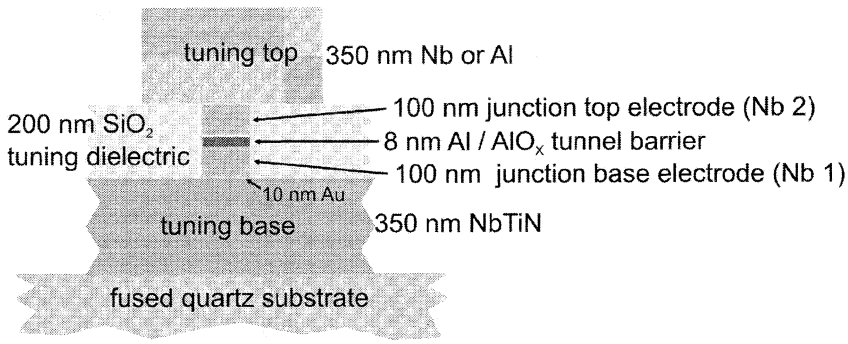

Fig. 2: Cross-section of HIFI Band 2 device layer stack

Then the junction area is defined via EBL in PMMA. Table 1 sums up the relevant process parameters. The use of an available 1 µm thick negative tone resist (MICRORESIST ma-N2410) would make a standard SNEP fabrication scheme possible but only works reproducible down to around 0.8 μm^2 junction area [8]. With a thin (positive tone) PMMA resist a self-aligned lift-off process for junction isolation is not possible.

Therefore we have integrated our EBL / CMP process into junction fabrication of our HIFI mixer. This processing scheme is based on the PARTS process [9] in which the junction isolation is not achieved by a self-aligned lift-off process (SNEP) but through planarization of a blanket layer of the dielectric material (Fig. 3). For pattern transfer during RIE, an etch mask is defined by sputter-deposition of 30 nm Al and 20 nm Au into the PMMA features and subsequent lift-off. The Au layer acts as a protection of the Al towards the alkaline developer during a subsequent photolithographic process. With this lithography step the area in which the Nb–AlO_x–Nb-layers are etched away is confined to the ground plane area of the tuning circuit.

The junction is then etched with several RIE steps. RIE of the Nb 2 and Nb 1 layers is performed with a mixture of CCl_2F_2 and NF_3 yielding an anisotropic etch behavior, while an Ar sputter etch is used to remove the AlO_x layer and the Au layer in a multi-cycle process [2],[4].

After removal of the remaining resist, 900 nm SiO_2 (tuning dielectric and junction isolation) is deposited onto the whole wafer with RF sputtering.

resist type	AR-P669.04 (PMMA 600k, 4%), ALLRESIST
resist thickness	220 nm
charge dissipation layer	6.5 nm Al sputter-deposited on PMMA
exposure dose	150 – 220 µC/cm^2 (proximity effect compensation)
e-beam current	14.0±0.2 pA
removal of Al layer	buffered phosphoric acid solution
development time	4 min AR600-56, ALLRESIST
stopper time	0.5 min AR600-70, ALLRESIST

Table 1: Electron Beam Lithography Parameters

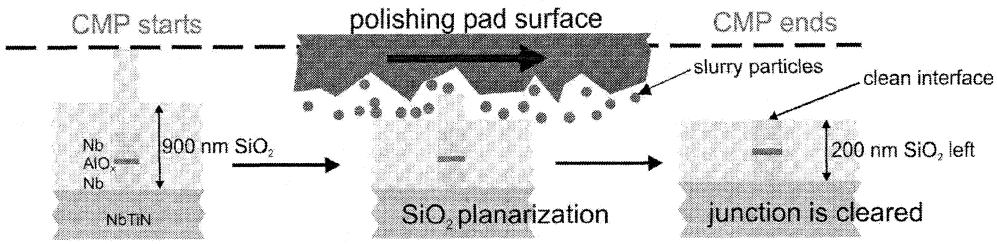

Fig. 3: Schematical explanation of the planarization process

The planarization efficiency during CMP is a function of feature size, with the generated topography of larger structures being planarized at a slower rate than smaller ones. This is due to deflection of the polishing pad and is in turn affected by the elasticity of the pad and the applied back pressure during polishing. Applied to our chip layouts this implicates that small features, such as the junction stack and waveguide probe, planarize faster than the large bond pad features at the other end of the RF-blocking filter structure. Dielectric thickness of the SiO_2 in the tuning circuit ground plane areas determines the end-point during polishing and thus terminates CMP before the contact area on the bond pad is cleared from the SiO_2. By defining additional holes in the dielectric layer during above photolithography contact problems are prevented.

During CMP the quartz wafer is glued onto a two inch silicon wafer with thin film wax for higher mechanical resilience during the polishing (Fig. 4, right). The CMP process has been transferred to a dedicated new polisher ([10], Fig. 4, left).

4 – 6 polishing steps are needed to complete the planarization and thinning of the dielectric each of typically 5 min duration. The remaining dielectric thickness must be 200±20 nm for the integrated tuning circuit to work as designed. End-point detection is realized by visually checking the color of the isolation dielectric under a microscope and profilometer measurements across the if structure relative to substrate level. The removal of the etch mask on top of the junction proves to be a very good additional indicator for clearance of the electrodes and can be performed without leaving any residue behind.

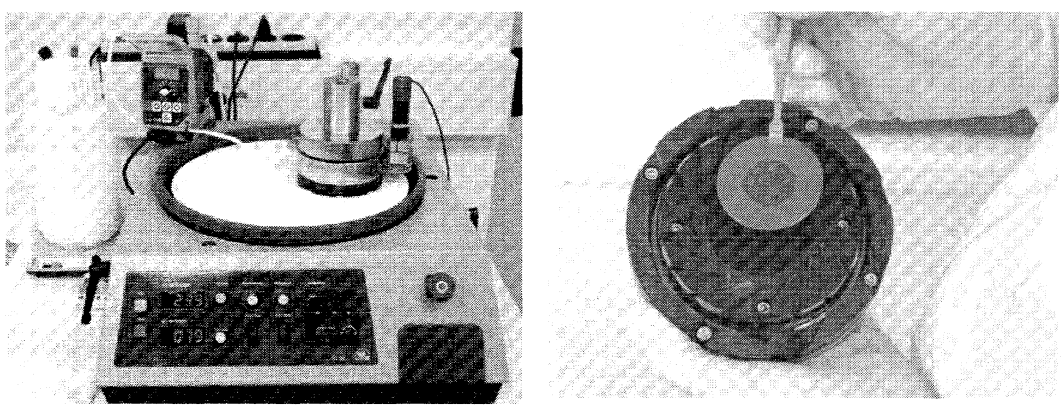

Fig. 4: CMP setup during processing (left photo) and quartz wafer glued onto a 2" silicon wafer prior to placement into the polishing head recess (right photo)

polishing pad	14" diam. IC-1000 / SUBA IV stack, RODEL CORP.
Slurry	ILD1200, diluted 1:4.3, pH = 10.5, RODEL CORP.
slurry feed	6 ml/min
jig rotation	22 rpm
pad rotation	20 rpm
relative velocity	0.37 m/sec
down force	26 N
wafer surface protrusion	approx. 100 µm, DF200 wafer backing, RODEL CORP.
typical bulk removal rate	30 nm/min

Table 2: Summary of important CMP processing parameters

The CMP process parameters have been adjusted to deliver local planarization of the junction area and best global uniformity of the tuning circuit dielectric thicknesses. After CMP the wafer surface is cleaned with a 2 % NH_4OH solution and PVA sponge. Table 2 sums up important CMP parameters.

Then follows the definition and sputtering of the integrated tuning top electrode, the missing half of the RF-blocking filter, the bond pad areas and alignment marks for dicing. This is done in two processing steps through UV lithography, sputter deposition of the metallization layers and subsequent lift-off. At first the Al-based integrated tuning top electrodes are defined with a 350 nm thick Al layer, supplemented by 70 nm Nb to eliminate series DC resistance. In the second step a 350 nm thick Nb layer, supplemented by 30 nm Au for bond adhesion, serves as the metallization layer for the Nb-based integrated tuning top electrodes, the other RF-blocking filters / waveguide probe halves, dicing marks and the bond pad areas of all devices.

To protect the integrated tuning top electrodes and the Al containing RF-blocking filters, a final UV lithography and lift-off step is needed for RF sputter-deposition of the 400 nm thick SiO_2 passivation layer.

III. DC I/V RESULTS

The inclusion of e-beam lithography and CMP into our HIFI mixer fabrication has a significant impact on device quality. An improvement of device quality is observed in two areas. First, junction area reproducibility has been significantly improved. Fig. 5 compares the junction area reproducibility of the first EBL / CMP scheme HIFI mixer batch with a previously defined UV300 / SNEP batch. The results are already close to those of past development runs with simple all-Nb devices (Fig. 1).

Second, the new process delivers junctions with systematically higher gap voltages than the old process. In Fig. 6 typical DC I/V curves of junctions from both fabrication schemes but otherwise identical fabrication parameters (e.g. layer stack, R_NA product, junction area) are compared. In this example the EBL / CMP processed device exhibits a gap voltage increase by over 0.2 mV (Fig. 6, left). In our interpretation the CMP leaves a very clean interface at the top of the junction electrode, thus enabling a better thermal contact of the junction to the integrated tuning top electrode and therefore better cooling of the tunnel barrier. We believe that our interpretation is also underlined by the fact that the gap voltage spread of a CMP produced batch is narrower when the junc-

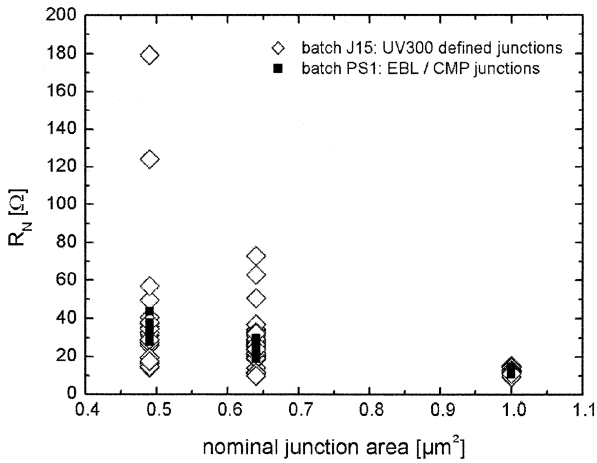

Fig. 5: Improvement in junction area reproducibility of a EBL / CMP fabricated batch in comparison to a past UV300 defined batch

tions of two differently processed batches are plotted as a histogram of their gap voltages (Fig. 6, right).

This underlines our past observation that it is very difficult to get a reproducibly clean junction top electrode interface after lift-off of the junction isolation during SNEP with embedded trilayer devices. With the UV300 / SNEP-based process we assisted the critical lift-off through a "short" chemical-mechanical polish on our prototype CMP setup.

Subgap current levels are not improved by the new process and are still at levels ($R_{sg}/R_N < 8$) significantly reducing mixer RF performance. As standard Nb–AlO_x–Nb devices of similar R_NA products routinely show R_{sg}/R_N ratios of 15 or better we conclude that this behavior is intrinsic to embedded trilayer devices of our junction fabrication. We have indication that the rough NbTiN base layer has an adverse affect on tunnel barrier leakage characteristics.

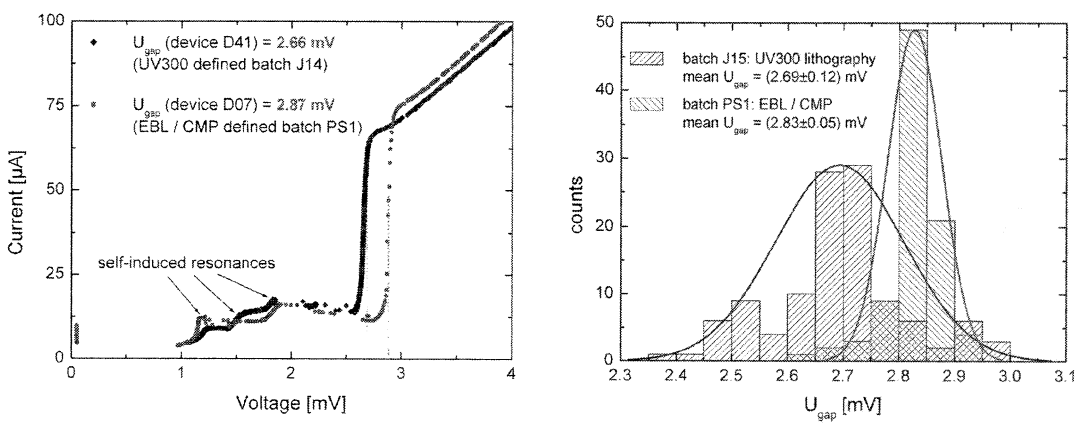

Fig. 6: Systematic increase and higher reproducibility of device gap voltage due to CMP. Comparison of two typical I/V curves (left) and histogram of gap voltage distribution (right) at 4.2 K

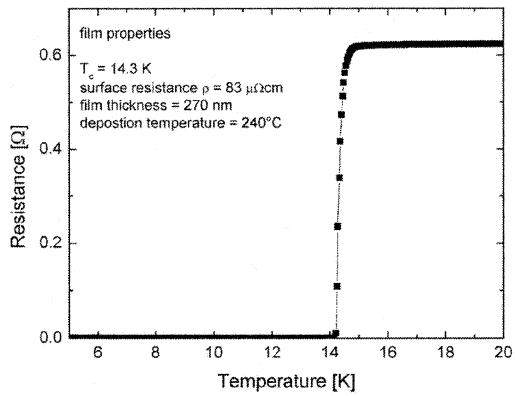

Fig. 7: R/T curve of a NbTiN thin film (van-der-Pauw structure), sputtered at an elevated substrate temperature of 240°C

NbTiN sputtered at an elevated substrate temperature is now available with our new sputtering machine for next fabrication runs. Van-der-Pauw measurements of NbTiN sputtered at 240°C show very promising results as they make low resistivity films for junction fabrication accessible without the penalty of high film stress (Fig. 7).

IV. Summary

We have made progress in device fabrication for HIFI Band 2 mixer by integrating EBL and CMP for junction definition into the processing scheme. Junction area reproducibility has been greatly improved for junction areas below 1 μm^2 and the gap voltage been systematically increased through our EBL / CMP process.

R_{sg}/R_N ratios still have to be improved to achieve required device performance. We are narrowing down the cause for our low R_{sg}/R_N ratios.

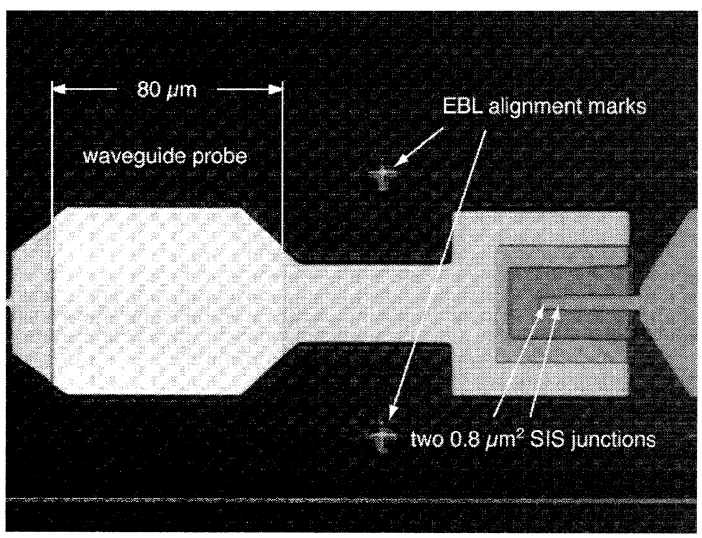

Fig. 8: Microscope photo of a recently fabricated EBL / CMP device for HIFI Band 2 mixer development (two junction integrated tuning circuit)

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