

A 1650-1900 GHz Tunable Source

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Abstract

A chain of multipliers has been built which for the first time produces an all solid state source up to 1.9 THz. The chain uses a tripler multiplying from near 300 GHz to 900 GHz and a doubler up to 1800 GHz. The 300 GHz source presently uses various multipliers and solid state drivers, with the goal of using a single cascaded pair of doublers driver by a power amplifier for the full band. All of the multipliers in this work use planar varactor or varistor diodes with a significant level of circuit integration. Output power exceeds 1 μ W at several points in the band and a peak of 3 μ W. The source is operated at a temperature of 90 K for best efficiency.

Introduction

The Herschel (FIRST) space mission requires LO sources with frequencies from 1.4 to 1.9 THz to operate HEB mixers in band 6. This band is broken up into two sub-bands, with the higher band of 1.7-1.9 THz being the subject of this work. The LO for these receivers is based on passive frequency multiplication from a initial band of 71-106 GHz where high power amplifiers are available. One way of multiplying to this band is to use a combination of three doublers and a tripler with a net multiplication of $\times 24$, with a starting frequency in the 71-79 GHz range. Another possibility is to use two triplers and one doubler ($\times 18$), and to start in the frequency range 94.5-105.5 GHz. The expected power level needed for these mixers is $\sim 1 \mu$ W, which is a fairly high power given the high frequency, and places fairly extreme requirements on the LO chain, given the present state of the technology. At 1.5 THz an HEB mixer has operated optimally from a 1 μ W solid state source [1], and this verifies the required power, although typical mixers at this time seem to use larger HEB devices (and more LO power) than the one used in this test.

In order to meet the requirements for flight qualification the source must use all-planar components with no mechanical tuning. At this time, planar diodes have shown excellent performance over moderate bandwidths and mechanical tuning is not really practical with most designs, so this requirement is not much of a limitation. Efficiencies actually exceed early expectations, and operating bandwidths do meet the goal. Diode

fabrication is quite consistent, and nearly all multiplier designs work very well, except that there are persistent errors in the exact frequency range covered relative to the design. Fairly complex circuits can be fabricated monolithically, on GaAs of any needed thickness and so the full set of tools are available to make the needed multiplier chains.

Within the range of multipliers that have been designed for this work there are many possible ways to realize either $\times 18$ or $\times 24$ net multiplication. In general if a chain uses a tripler it should be placed as the last stage because triplers are less suited to produce high output power than doublers. However, at the very high frequencies involved, a tripler circuit is harder to fabricate on GaAs, particularly if it is to be DC biased. In addition there are questions about the potential efficiency of such a high frequency tripler because of carrier velocity saturation which tends to reduce higher harmonics in the diode waveform. For these reasons this work is based on a doubler as the final stage, with a tripler as the driver. There is still a choice of initial stages, but two cascaded doublers have far higher output power potential than a single tripler, given that there is a good understanding of how to use series diode arrays in doublers but not in triplers. Thus this work is based on a $\times 2 \times 2 \times 3 \times 2$ chain.

Driver stages

While the plan is to use $\times 2 \times 2 \times 3 \times 2$, the first two doubler stages are not yet optimized and this work was primarily intended to test the feasibility of a tripler near 900 GHz driving a doubler. To provide full coverage, a variety of sources were used as drivers in the 280-320 GHz band. At the lowest frequencies a Gunn oscillator producing 50 mW from 140-146 GHz was used to drive a doubler. From 290-310 GHz a cascaded doubler- doubler was used, and at the highest frequencies a tripler was used. These drivers produced varying amounts of power and the final output varies considerably as a result, but it was possible to cover the full band.

All of the multipliers use planar diode arrays, and almost all of the devices used were developed for the Herschel work. The number of diodes used in the multipliers (and their size) depends on the expected power level. Both the doublers and triplers are very similar or identical to those described previously. All of the tests performed at ~ 90 K since Herschel will operate with a cold LO system at a temperature near 120 K.

The doubler used near 150 GHz was built some time ago using a UVa diode array [2. 3] and this device was intended to drive the chain at frequencies from 140-160 GHz, but the diode used was destroyed by overpower in early tests and no sufficiently similar replacement device was available. As a result the useful bandwidth was greatly reduced, and sufficient power was available only near midband. To avoid further loss of time the input power was limited to 150 mW which is probably well under the maximum that could be used. The typical output power was 45-50 mW in the midband. At frequencies below 146 GHz a Gunn oscillator was available producing 50 mW which exceeded the doubler output power, so this was used as a driver.

The planned second stage doubler uses a diode designed at UMass, and fabricated at JPL using 4 anode array. It is quite similar to a doubler described previously [2, 3] but with simpler construction. The diode array is connected to a beam lead capacitor with a 50 μm wide ribbon and these components are mounted to a waveguide block by soldering the diode in place. The construction is shown in Figure 1. While the block seemed to be properly constructed, there was a very large error in the operating frequency which tuned the block quite low in the band, and it was only marginally useful above 300 GHz. It is possible that the diode has excess capacitance, or that there is a design error in the block, but this is still unresolved. Despite this problem, there was still 10-15 mW output power from 275-300 GHz (at 90 K), which dropped rapidly above 300 GHz. This power was less than desired and certainly not enough for a flight multiplier chain, but sufficient for initial tests.

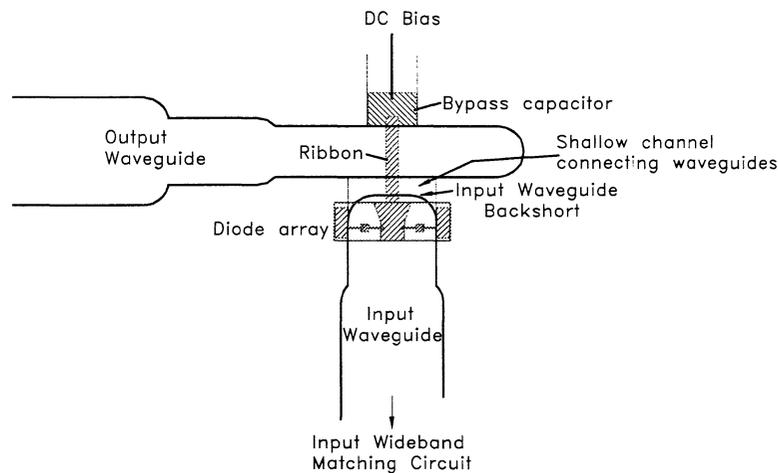


Figure 1. 280-320 GHz doubler using 4 diode array and beam lead capacitor for bias bypass.

As an alternative source for the frequencies above 300 GHz a tripler [4] was used which was built as prototype for later balanced triplers, including the 900 GHz stage in this work. This early design had limited bandwidth but good efficiency at the peak, which just happened to be from 300-320 GHz. The output power is estimated to be 8-9 mW at 90 K, which is considerably less than would be obtained from a doubler, but marginally adequate for this work. As a side note, this same tripler design is being used as the 320 GHz subharmonic LO on the EOS-MLS 640 GHz receiver.

900 GHz Tripler

The tripler was designed at UMass and the diode circuit was fabricated JPL. It is a balanced design very similar to the one mentioned above, and uses a pair of diodes. Provision is included within the chip for series biasing of the two diodes. A cross section

of the block and the device chip is shown in Figure 2. The block for the tripler was machined on a precision CNC micro-milling machine [5], with the very reduced height output waveguide made by broaching a slot with a 25 μm wide tool. Note that this waveguide steps up to near full height very close to the diode chip. The tripler is easy to assemble except that diode chip is very small and is only 12 μm thick. Thus the main problem is in picking up the chip, but with micro-manipulators this is fairly straightforward. The chip is simply glued into the block with the beam leads establishing the circuit ground, and the bias lead connected to an external bias circuit.

A prototype was built using a device that was 20 μm thick, rather than the design thickness of 12 μm . The tuning of these triplers is known to be sensitive to the thickness of the GaAs, and as expected this device tuned very low, relative to the design. However, it did operate at a frequency where a fairly powerful driver source was available, and so was useful in establishing the potential maximum output power that may be obtained. Tests were performed near a physical temperature of 90 K, which was convenient using LN₂, although actual operation in Herschel will be at 120-130 K. The peak output power was 1.0 mW near 810 GHz with ~18 mW input, which actually exceeded the expectation for this device. Bias conditions seemed moderate (2.3 V at 0.5 mA for the series pair) given the size and 4V (per diode) breakdown voltage for the device, but no long term testing was done to establish any safe operating limits.

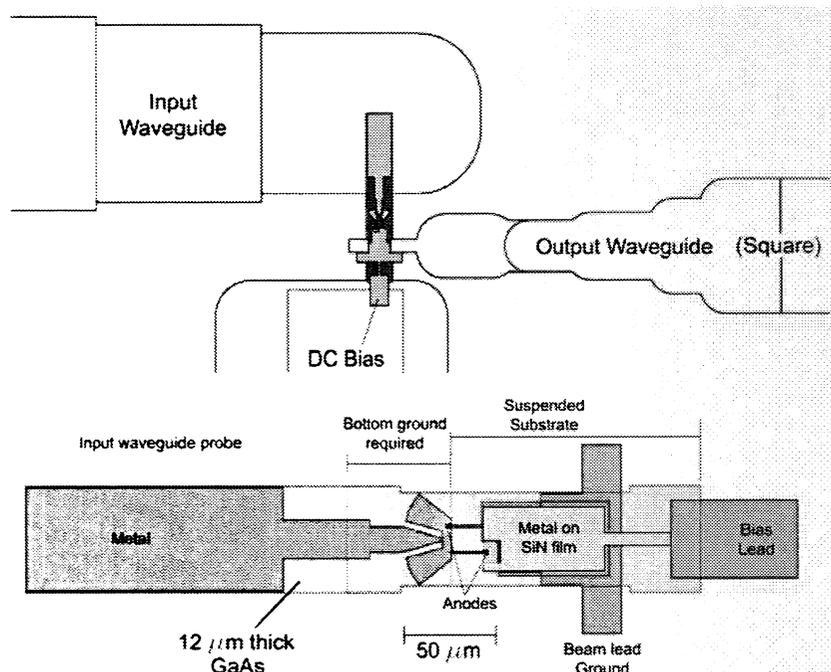


Figure 2. 900 GHz tripler cross section and the diode chip.

After these tests a second tripler was assembled with a 12 μm thick device and it appears to tune as expected, although there is not enough input power to properly pump it over the full band. Peak output power is lower, but this is largely because there is less input available, and only somewhat due to the higher frequency. A plot of the output power of both triplers over their respective bands is shown in Figure 3. Input power is not calibrated, but is typically 7-12 mW over the points tested. These tests were performed at a temperature near 90 K. Three drive sources were used, as described in the previous section.

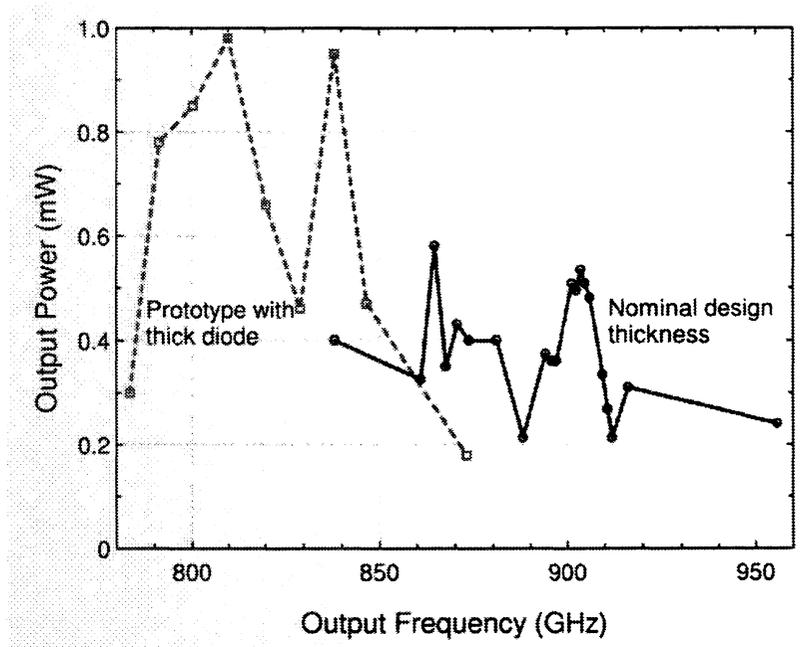


Figure 3. Output power from two triplers of the same design at 90 K with various drivers. The dashed curve is for a 20 μm thick device while the solid curve is for 12 μm thickness. Typical input power is 15-18 mW for points below 850 GHz and 7-12 mW above.

1.8 THz doubler

The doubler for 1.8 THz uses a balanced design in a resistive mode, with the diodes forward biased. The diodes are mounted in series in the output waveguide to simplify a layout with bias. The design is very much like that for 1.5 THz [6] except that the old design was on 3 μm thick GaAs with a 50 μm thick handling frame, while the new design has no frame, just 3 μm thick membrane for the circuit substrate with a 50 μm thick extension handle. The circuit has also been revised to improve the input match, and the overall bandwidth. The block was machined with the same CNC micromill as for the tripler, using end mills down to 50 μm diameter. The output waveguide transitions to square waveguide very close to the device chip, which is mainly required for optimal

impedance matching, but also aids the transition to a diagonal feed horn which is machined into the block. The input waveguide is internally $150 \times 300 \mu\text{m}$, but to reduce the loss of the input section, this was increased to a square $300 \mu\text{m}$ cross section at the flange. The same was done to the output waveguide for the 900 GHz tripler. While in principle this oversized cross section can work perfectly, there is some evidence in the test data that excitation of higher modes may be a problem.

The circuit is fairly easy to assemble, except that diode can not be positioned, or even touched, by hand, since the $3 \mu\text{m}$ thick GaAs is extremely fragile. The thicker “handle” region is strong enough to be useful for some purposes, but micro-manipulators are the preferred method of handling. Assembly simply requires positioning the chip properly and attaching the bias lead with conductive epoxy. The beam leads provide all of the remaining connections to the block, and the chip is fully suspended across the channel by its leads.

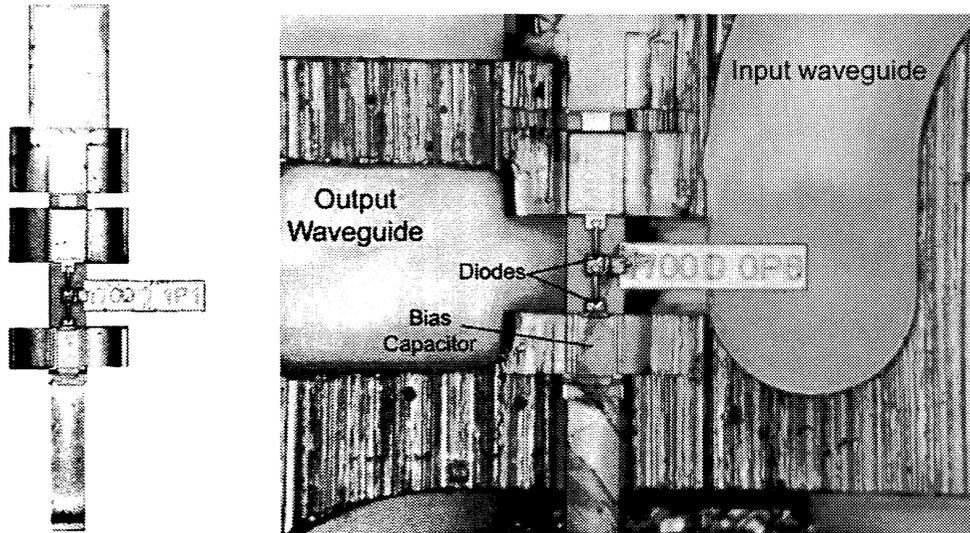


Figure 4. 1800 GHz doubler device and a detail of the complete block. The output waveguide at the left side of the photo is square and transitions to a diagonal horn.

All testing was done using the same 900 GHz tripler as a driver. The diodes were current biased at 0.2 mA, which appeared close to optimum for all input power levels. At this bias, V_{bias} is 1.8V with no drive to the doubler, at a physical temperature of 90 K. At the maximum input power this bias decreases by about 0.4 V. This bias change at constant current (ΔV_{bias}) is proportional to input power in the square law limit, which is quite broad for a biased detector. Up to the maximum input power, the output power varies as ΔV_{bias}^2 , equivalent to P_{in}^2 , which indicates that the doubler is very underdriven. This is expected since for the 1500 GHz doubler, an input power of 2 mW was required

to get the output into the regime where it is linear with input power. The plot in Figure 5 shows the output power and also a curve proportional to ΔV_{bias}^2 for the doubler over the range of frequencies tested. As can be seen, there appears to be a very close correspondence between these two quantities over the full band, and it is much easier to measure bias voltage than output power at the very low power levels involved, which approach the limit of sensitivity of the power meter [7] used.

Input power was not measured in any detail over the band, but the curve of Figure 3 (for the tripler output) may be used as an indication of the power available, since this was measured under the same conditions as in the doubler tests. Only the tripler with 12 μm thickness was used in these subsequent tests. As may be seen, the output power exceeds 1 μW for an input power of ~ 0.4 mW. This is fully consistent with the results for the 1500 GHz doubler. The highest power point of 3 μW also occurs for an apparent input power of 0.4 mW but, being at a band edge point for both devices, may result simply from a favorable interaction where the tripler delivers more power than into a matched load.

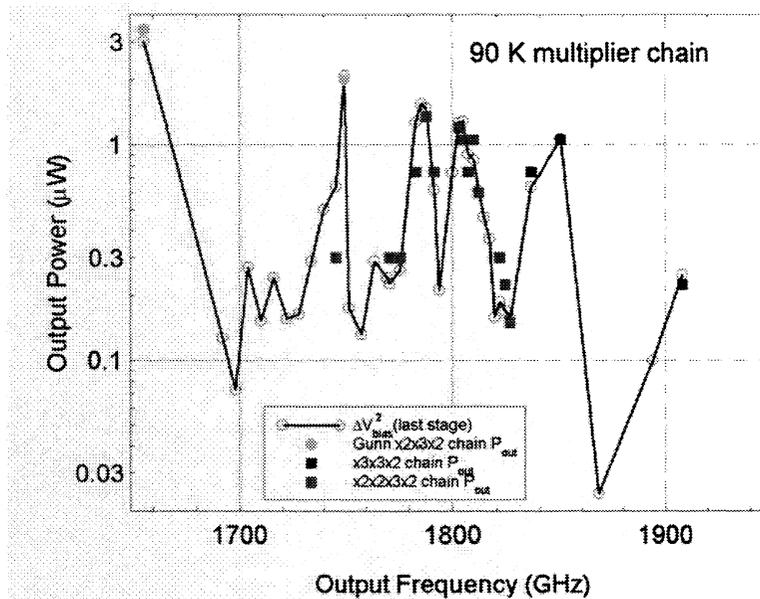


Figure 5. Output power from the 1800 GHz doubler, both measured (solid points) and estimated from the video response of the diodes (continuous line). Input power is as shown in Figure 3.

Figure 5 shows a general decrease in power at higher frequencies due to lower drive power, but the close correspondence between measured power and bias indicates that the output matching is quite flat. The input match shows no clear trend given the somewhat randomly spaced points and varying available power, but the power ripple is

higher than expected. It is possible that this results from a poor waveguide interface between the devices, either a poor flange joint, or significant mode conversion in the oversized waveguide. It is much higher than would be expected from the predicted VSWR of the two devices, since with a resistive doubler is actually fairly easy to get a good input match.

The properties of the various multipliers are summarized in Table 1. Efficiencies are well documented for the first two doubler stages but are only estimated for the last two stages. Efficiencies were not measured at room temperature for the higher stages, but it is expected that they operate similarly at room temperature because of the very high epilayer doping. The primary reason these tests were performed cold is to get the benefit of the increased power available near 300 GHz from the driver stages which use low doped diodes. Without this power the final stage would work too poorly to be even measurable.

Frequency	Number of diodes	Efficiency 90K	Epilayer doping
150 GHz	6	39%	1×10^{17}
300 GHz	4	28%	2×10^{17}
900 GHz	2	~5%	3×10^{17}
1800 GHz	2	~.2%	5×10^{17}

Table 1. Multiplier properties

While all details are not known, the overall $\times 24$ efficiency is a maximum of 7×10^{-6} . Because of the underdriven last stage, this would increase by a factor of ~ 3 at higher drive power, if the first two stages are operated in a power combined mode (two doublers in parallel with output combining). It is clear that the output power will not exceed $\sim 10 \mu\text{W}$ with the present limitations. With this method of operation there is potential for $\sim 1 \mu\text{W}$ output power above 2 THz with present technology, and in fact the required devices have been made as part of the same diode wafers used in this work.

Conclusions

A complete solid state source has been built for 1.8 THz using a net $\times 24$ multiplication, driven by a power amplifier. While tuning with good power is not continuous, there are a sufficient number of higher power points to indicate that a source with >200 GHz bandwidth and $>1 \mu\text{W}$ output is practical. It is likely that power combining will be needed for the first one or two stages in order to get sufficient power over the full band, but this is not inherently difficult, given the present state of planar technology. It appears that at least somewhat higher frequencies are feasible using the same approach.

Acknowledgement

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