Beam Lead Fabrication for Submillimeter-wave Circuits Using Vacuum Planarization

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The assembly of superconducting millimeter and submillimeter-wave circuits becomes increasingly difficult as chip dimensions and design tolerances shrink with increased operating frequency. Currently, RF ground connections are made by soldering, wire bonding or with conductive wire gaskets[1,2]. To facilitate assembly and throughput, we are developing a beam lead process for quartz chips. Such processes already exist for silicon and gallium arsenide wafers[3-5]. However, niobium circuits on quartz substrates present unique difficulties. SIS junctions introduce additional thermal and chemical constraints to process development. For quartz, wet etches are isotropic and dry etches with high etch rates require large ion energies. We have developed a new, top-side approach to beam lead fabrication suitable for whole wafer processing.

Introduction

We have developed a new, top-side approach to beam lead fabrication suitable for whole wafer processing. The new process, reported for the first time in this paper, differs from our original approach in which a sacrificial epoxy resin is planarized within the trenches using a sodium chloride optical flat[6]. The new process still uses a sacrificial epoxy to fill the trenches, but the method of epoxy planarization is much improved.

Process

After the mixer circuits are completed, trenches are cut along the perimeter of the chips using a standard wafer dicing saw. The trenches are diced only partly through the wafer, to a depth slightly greater than the desired chip thickness. Multiple passes with the dicing saw are used to achieve the desired trench width. Trenches are, on average, 143μm wide with a standard deviation of 12μm.

Planarization is accomplished by filling the diced trenches with a sacrificial epoxy. This is done by isolating the trench volume from the surface of the wafer and then injecting the epoxy into the trench volume. To isolate the trench volume from the wafer surface, a relatively smooth piece of silicone rubber is placed atop the wafer. The silicone is naturally attracted to the wafer surface by Van der Waals forces, creating a seal at the wafer-silicone interface. Once sealed, the wafer is placed in a metal support jig with the backside of the wafer facing up. Because the trenches run to the edge of the wafer, there is a unique opportunity to "inject" the epoxy into this unsealed region. This is accomplished by first placing the jig under vacuum along with an attached reservoir of epoxy. After the air is removed, the vacuum chamber is tilted in such a way that the epoxy runs from the reservoir, into the jig and over the wafer. The epoxy is allowed to

flow over the wafer until the perimeter of the wafer is thoroughly coated. When the vacuum is released, air pressure forces the epoxy into the trenches. The excess epoxy on the backside is then cleaned off. Next, the wafer and jig are oven-baked to cure the epoxy. After curing, the silicone rubber is gently pealed away, revealing a clean quartz surface and epoxy-filled trenches. Because the silicone rubber seals the surface very tightly and uniformly, every trench fills in the same manner resulting in consistent epoxy planarization across the wafer. The open quartz surfaces are completely devoid of any residual epoxy.

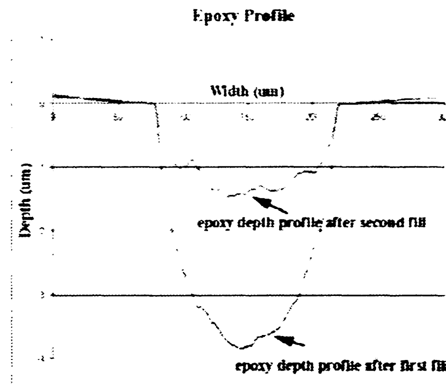

Figure 1 Trench depth is improved by performing the vacuum planarization process twice. After one fill, the maximum depth of the epoxy is, on average, 3.83μm. After a second fill, this is improved to 1.58μm.

The vacuum planarization process produces excellent results. The level of the epoxy does dip below the level of the quartz, but this dipping is slight compared to the depth of the trench. After planarizing once, we find an average dip in the epoxy of 3.83μm, with a standard deviation of 630nm. To further improve planarization, the epoxy is etched back by 30μm using an oxygen plasma. The process is then repeated once again, resulting in an average epoxy dip of only 1.58μm below the quartz, with a standard deviation of 470nm, as seen in Figure 1.

After the epoxy is fully cured, 15nm of titanium and 50nm of gold are sputter deposited over the wafer using DC magnetron sputtering. The titanium serves as an adhesion layer for the gold atop the quartz and epoxy surfaces. The gold serves as a plating seed layer, providing electrical continuity across the wafer during the plating step.

The beam lead patterns are defined using an ultra-thick resist, and are designed to straddle the quartz-epoxy boundary. Thick (10μm) gold beam leads are plated atop the seed layer within the resist patterns. After plating, the resist is stripped with acetone. The gold seed layer and titanium are removed using wet chemical etchants. The wafer is then mounted, beam lead side down, to a silicon carrier wafer. With the wafer mounted face-down, the quartz is lapped to the desired chip thickness, usually around 100μm or less. Since the trenches are deeper than the final chip thickness, the lapping process separates the chips from one another. The sacrificial epoxy is then removed from between the chips using an oxygen plasma. The mounting wax is then dissolved using TCE. At this point, the

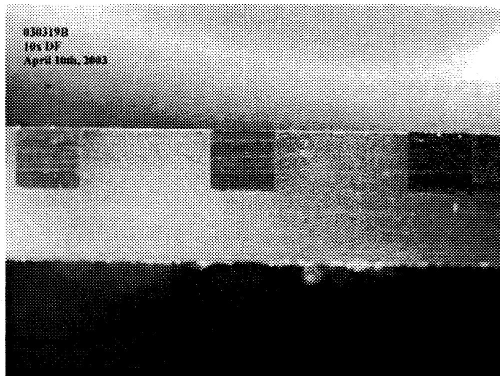

Figure 2 Epoxy-filled trenches are shown in the above cross-section of a quartz chip. The wafer thickness is 250μm. The cross-section was made using a wafer dicing saw.

chips are completed. The beam leads extend 40μm beyond the chip perimeter, and are rigid enough to support the chip when gripped with fine tweezers.

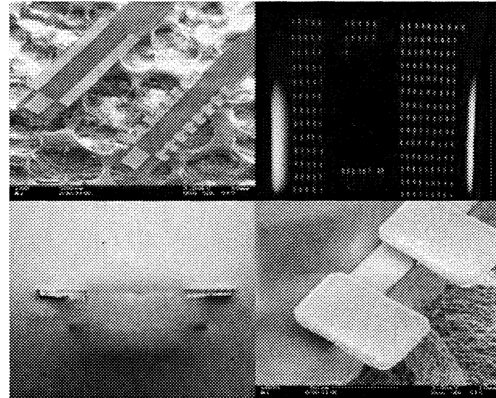

Figure 3 A composite picture of quartz chips with gold beam leads. In the upper left is an SEM image of two beam lead chips. A close-up SEM image is shown in the lower right. In the upper right is a completed batch of chips. In the lower left is an end-on picture of gold beam leads extending off of a quartz chip.

Conclusion

This process was developed specifically for quartz, but its implementation is independent of the substrate. The technology is easily transferable to other substrates such as silicon or gallium arsenide. Moreover, this fabrication process is also suitable for substrates for which beam lead processes have yet to be developed, such as sapphire and glass. We have found a device yield of greater than 60%, which is much improved with respect to the process of [6]. However, the device yield is not limited by the planarization process; beam lead failures are attributed to seed layer adhesion and plating issues.

Submillimeter-wave circuits with beam lead RF ground connections greatly simplify the assembly of receivers. Beam leads make it possible to quickly test receivers, and allow for replacement of nonfunctioning chips without having to deal with conductive adhesives, wire bonding or soldering. In turn, the ability to assemble large arrays of submillimeter devices is enhanced, since the burden of fabricating a large, functional array of devices on a single chip is eliminated. Instead, individual beam lead chips may be placed into micro-machined waveguides and then tested. Non-functioning devices may then be removed and replaced. The size of the array is then no longer limited by the yield statistics of the device fabrication process.

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