# Ultra-Thin Silicon Chips for Submillimeter-Wave Applications

R.B. Bass,[1] J.C. Schultz,[1] A.W. Lichtenberger,[1] R.M. Weikle[1]
S.-K. Pan,[2] E. Bryerton,[2] C.K. Walker,[3] Jacob Kooi[4]

1 - University of Virginia, Charlottesville, Virginia
2 - National Radio Astronomy Observatory Charlottesville, Virginia
3 - University of Arizona, Tucson, Arizona
4 - California Institute of Technology, Pasadena, California

We present a process for fabricating ultra-thin silicon chips for submillimeter-wave mixing applications using SOI (Silicon On Insulator) wafers. Such chips allow the profile of the mixer substrate to be minimized within the microstrip channel, thereby simplifying RF design considerations and minimizing machining constraints. The chips feature gold beam leads, RF filter structures, and hot-electron bolometers as the non-linear element.

We designed a prototype receiver to demonstrate the feasibility of the ultra-thin silicon chip technology. The receiver has a center frequency of 585GHz and accommodates both diffusion-cooled and phonon-cooled hot-electron bolometer mixers fabricated atop an ultra-thin silicon chip. The chip fits within the microstrip channel of a split-block horn antenna. Protruding from the sides and ends of the silicon chip are thick gold beam leads, which provide electrical and thermal contact between the chip and the waveguide block. In addition, the beam leads provide mechanical support to the chip, allowing the chip to be suspended within the middle of the microstrip channel between the two block halves.

Ultra-thin silicon chips with beam leads will facilitate the construction of large format spectroscopic imaging arrays. Such arrays would contain an assembly of individual chips, each featuring a single nonlinear mixing element. The chips could be added, removed of replaced without disturbing the rest of the elements within the array. There are myriad potentials for such systems; examples include atmospheric research, astrophysics, and security systems.

## 1 Introduction

The bulk of our work at the University of Virginia has centered on the development of niobium-based SIS mixers fabricated atop quartz substrates. These are single-element receivers, which rely on waveguides to couple RF radiation from a feedhorn antenna to a mixer chip [1,2]. Single-element waveguide receivers are standard for SIS- and HEB-based receivers, with the exception of a few arrayed waveguide receivers consisting of SIS mixers [3,4].

Our research group, in cooperation with researchers at the University of Arizona and the California Institute of Technology, has made progress towards integrating HEB mixers atop silicon nitride membranes as another approach for assembling receiver arrays [5]. Integrated arrays offer the benefits of rapid assembly and dense receiver integration since all of the mixers are fabricated atop a single chip. However, all of the devices on the array chip must have similar characteristics. In addition, the silicon nitride membranes must be extremely thin, around 1μm, at which point the membranes are extremely brittle and difficult to handle. Failure of any one of the mixing devices or membranes on a chip would lead to a loss in pixel density, jeopardizing receiver performance and possibly requiring the replacement of the entire mixer array chip.

These problems can be circumvented if each mixing element of an array is fabricated atop a single, smaller chip that could be placed within an array frame. By contacting these ultra-thin chips to the array frame via beam leads, the array can be quickly assembled with pre-tested devices, and later individually removed without disturbing other elements within the array frame [6]. In addition, ultra-thin silicon chips can be used in single-element metal waveguide receivers, greatly reducing the amount of dielectric in the waveguide channel while facilitating rapid prototyping and device replacement.

Ultra-thin chips with beam leads are a potentially powerful technology for THz mixers if several considerations can be met. First, the technology has to be compatible with SIS and HEB fabrication processes. Second, the chips need

to be 1μm to 10μm thick, and must be robust enough to survive receiver assembly and repeated thermal cycling down to cryogenic temperatures. And finally, because these chips are incredibly thin, they will have to be integrated with beam leads in order to mount them in THz mixer blocks or array frames.

Our fabrication process utilizes silicon-on-insulator (SOI) substrates integrated with gold beam leads to achieve ultra-thin silicon chips, and is a unique idea that we first implemented and published in 2003 [7]. Given our earlier work on beam leads for quartz-based millimeter-wave mixers, we realized that the solution to the requirements mentioned above lay in the integration of beam lead technology with SOI substrates [8,9]. Ultra-thin chips can be defined from the device layer of an SOI substrate while the handle layer of silicon provides mechanical rigidity during preceding processing steps.

## 2 Limitations of THz Receiver Assembly

THz circuits are extremely small and usually fabricated on very thin and fragile substrate materials such as silicon or quartz. As the operating frequency of circuits increases, the size of the circuit housing decreases. In addition, the dimensional tolerances of the circuit housing decreases, making the placement of the circuit both more difficult and more critical. All of these problems make replicating state-of-the-art submillimeter-wave devices extremely difficult. To overcome these difficulties, the circuit mount should be designed so that it is as simple as possible to assemble and non-critical to the function of the circuit. Also, the assembly procedures must be as clear and reliable as possible.

There are several critical design issues that need to be considered when developing both the circuit housing and the assembly procedures for THz receivers. First, improper mounting techniques may mechanically damage chips and circuits. A small displacement of the chip in the receiver block may result in excessive loss, degradation of device sensitivity, or unwanted resonance. A good receiver block design should provide a robust mechanical interface for the fragile circuit. The housing must be simple to fabricate and non-critical to the circuit placement. It should also be easy to assemble, disassemble and reproduce. Second, while mounting submillimeter-wave circuits, any wiring lead or contact becomes a circuit element. An incorrectly sized or misplaced lead may de-tune the circuit or excite unwanted resonance. A small extra length of ground lead may result in decibels of loss. Improper electrical contacts increase circuit loss, degrade device sensitivity and reduce reliability. Third, with HEB's device failure is typically a result of electro-static discharge (ESD). ESD most likely happens during the assembly process when the circuit is exposed to other objects that are on a different electrical potential. To avoid ESD, a suitable assembly environment and a proper mounting procedure need to be established and strictly followed.

This work attempts to address these issues by integrating hot-electron bolometer mixer circuits with new beam lead and ultra-thin chip technologies. Implementing these circuits on ultra-thin chips greatly simplifies the RF design process by limiting the amount of dielectric material within the microstrip channel of the waveguide. The beam leads provide electrical, thermal and mechanical contact between the circuit and the waveguide. Furthermore, a beam lead design reduces the complexity of the microstrip channel structure, and eases the process for making contact between the chip and the mixer block.

## 3 Submillimeter-wave Circuit Mounting Techniques

There are several ways to mount millimeter and submillimeter-wave circuits into receiver blocks. Conductive adhesive provides electrical contact and thermal heat sinking to some power device packages. After the adhesive is set, however, it is difficult to remove the circuit from the package without incurring damage. Also, applying the appropriate amount of adhesive at the intended places is not a simple task. Other microwave products commonly employ wire bonding and soldering. However, as the operating frequency of circuits increases, the electrical traces of the circuit shrink. Some of the circuit traces of millimeter and submillimeter-wave circuits are so small (less than 25μm) that it is very difficult to make a reliable bond to the circuit. Also, as the frequency increases, the required bond wire length becomes shorter and more critical. This makes attaching the leads to the circuit very difficult. In general, wire bonding and soldering are used to assemble millimeter and submillimeter-wave circuits, but they are not without their share of difficulties.

Conductive adhesive, wire bonding, and soldering all attach leads permanently to the circuit. None are ideal for prototyping tasks where frequent changing of circuits is needed. Several other mounting techniques offer easy

circuit replacement. SIS mixer chips often incorporate micro-spring contacts, which are formed by pressing a narrow (0.125mm in diameter) gold-plated beryllium-copper wire against the circuit contact pad [10,11]. However, micro-spring contacts are usually not as robust as those formed by wire bonding and soldering. Also, the initial fine adjustment of the micro-spring wire is very time-consuming. But since it is very easy to replace a circuit chip in a micro-spring contact package, this method is particularly useful in prototyping low-power dissipation devices.

Another popular mounting technique makes contact between the block and the circuit through conductive wire gasket contacts. This technique offers easy chip replacement capability and provides excellent mechanical, electric and thermal contact to the circuit. For example, our SIS mixer circuits are clamped between the left and right halves of a receiver block in a suspended-substrate stripline configuration. The RF and DC ground leads connect between the substrate and block through gold crush wires (the conductive gaskets). The wires sit atop shoulders that are milled along the lengths of the microstrip channel. The substrate sits atop these wires, with the wires contacting metal pads on the substrate. The wires compress between the block and the metal pads when the two halves of the block are brought into contact. Since the connections are made solely by compressing gold wires, the depth from the top surface of the lower half-block to the shoulder of the substrate channel becomes very critical. This technique has been applied successfully in packaging SIS mixers for many years at NRAO [12,13]. However, due to the difficulties in machining the shoulders along the microstrip channel with the precision required for high frequency applications, it may not be practical to use this technique in submillimeter-wave circuits.

A preferable method for packaging submillimeter-wave circuits is the beam lead technique. The beam lead technique was developed in the 1960's by Marty Lepselter at Bell Labs as a simple and reliable way for connecting integrated circuits to printed circuit boards [14]. In this approach, thick (1μm to 10μm) metal beam leads are formed directly on the circuit during the circuit fabrication process, becoming an integral part of the circuit. The metal lead patterns extend beyond the perimeter of the circuit. The beam lead circuits are usually packaged in a split-block housing. Using the beam lead as a handle, the circuit is picked up and placed into the substrate channel with the extended beam beads positioned along the perimeter of the channel. As a result, the chip is suspended within the middle of the substrate channel. When the two halves of the block are brought together, the beam leads are clamped between the two block-halves. The beam leads provide good thermal and electrical connection to the device, and a rigid physical support for the chip. The beam leads are crushed between the block halves, securing the chip in place within the microstrip channel. The contact force is between the beam leads and the block halves, and not on the chip as other contacting methods require. As a result, beam leads allow for the use of thinner, more fragile substrates that might otherwise break when clamped between two block halves.

**4 Design of the 585GHz Test Receiver**

The original basis of our design for the 585GHz HEB waveguide mixer block derives from a family of receivers designed by researchers at the Harvard-Smithsonian Center for Astrophysics for the Submillimeter Array (SMA). The basic SMA mixer block design consists of two halves; a feed horn half and a back short half. A quartz substrate containing an SIS junction and low pass filter structures is suspended in a microstrip channel between the two halves, parallel to the block split plane. The feed horn, located in the upper block half, is perpendicular to the split plane. A reduced height waveguide couples the RF and LO radiation from the feed horn to a bowtie antenna structure on the quartz chip. A backshort, located behind the bowtie antenna in the lower block half, terminates the reduced-height waveguide behind the antenna.

The first SMA receiver operates around a center frequency of 200GHz [15,16]. Additional SMA receivers, operating at 300GHz, 450GHz and 600GHz, are scaled versions of the 200GHz receiver [17-19]. Kawamura, et al., designed a similar receiver that operates around 800GHz. This receiver features a phonon-cooled hot-electron bolometer as the non-linear mixing element, and was used in the Heinrich Hertz Telescope atop Mt. Graham in Arizona [20]. Researchers at the Space Research Organization of the Netherlands and Delft University adopted this design as well, and now plan to use their design for bands 3 and 4 of the Heterodyne Instrument for the Far-Infrared (HIFI) on the Herschel Space Observatory [21].

We made several major structural changes when adopting the 585GHz design from the SMA design. First, we replaced the 50μm quartz substrate in the SMA design with an ultra-thin silicon substrate. Second, the quartz substrate in the SMA design sits atop shoulders milled along the sides of the microstrip channel. Since gold beam leads suspend the ultra-thin silicon substrate within the channel, the shoulders are unwarranted. As a result, the

microstrip channel of the 585GHz receiver has a truly rectangular cross-section. We also scaled the dimension of the SMA design by a ratio of 600/585 in order to accommodate the change in operating frequency. And finally, we rotated the orientation of the feed horn so that the length of the feedhorn runs parallel to the mating faces of the block halves. In the SMA designs, the long axis of the feed horn is perpendicular to the mating faces, which requires electroforming and a mandrel in order to define the feed horn. With the feed horn oriented parallel to the block mating faces, the feedhorn antennae becomes easier, and therefore less expensive, to machine.

## 5 Advantages of Ultra-thin Silicon Chips

Silicon offers several material advantages over quartz for THz substrate applications. First, the rupture modulus of silicon is greater than that of quartz; 135MPa versus 50MPa. As a result, silicon may be thinned more so than quartz before it becomes too brittle to handle. Another advantage of silicon is its higher thermal conductivity, 150W/mK versus 2W/mK for quartz. On the other hand, silicon has a dielectric loss tangent that is nearly 40 times larger. However, due to the much larger thermal conductivity of silicon over quartz, the heat generated within a silicon substrate due to RF propagation dissipates rapidly.

A second disadvantage that silicon has over quartz is its larger dielectric constant, 11.9 versus 3.8 for quartz at 10GHz. As a result, a beam of silicon looks electrically thicker to an RF signal than a quartz beam of equal physical thickness. The square root of the ratio of the two dielectric constants determines the difference in electrical thickness, which for silicon over quartz is a factor of 1.77.

Most importantly for ultra-thin silicon chips, silicon is far more resilient than quartz. Resilience is the ability of a material to absorb energy when deformed elastically. This energy does not contribute to deformation of the material. Rather, the energy is release upon unloading. While silicon and quartz both have similar Young's moduli (179GPa for silicon, 75GPA for quartz), the yield strength for silicon is significantly larger than that of quartz (7GPa versus 50MPa), resulting in a modulus of elasticity for silicon that is far greater than that of quartz, 450MPa versus 17kPa for quartz at room temperature [22]. Virwani et al have shown that Young's modulus for silicon remains unchanged between bulk measurements and measurements made from deflecting nano-scale beams [23].

The modulus of resilience represents the amount of energy a sample can absorb per unit volume before yielding. A 3μm thick silicon chip contains 16 times less volume than a 50μm quartz chip of equal width and length, but can absorb far more energy per unit volume. Ultra-thin silicon chips are therefore far less likely to rupture under applied loads during handling and receiver assembly .

We conducted numerous analytical RF studies on the feasibility of using our ultra-thin silicon chips in THz receiver applications for both single-chip receivers and array antenna structures [24]. The use of an ultra-thin silicon chip as the substrate for THz circuitry greatly simplifies the RF design process. In addition, since shoulders need not be milled within the microstrip channel to accommodate the chip, machining of the receiver block becomes much more straightforward.

## 6 Fabrication of Ultra-thin Silicon Chips with Beam Leads

The process for fabricating ultra-thin silicon chips with beam leads is discussed in three subsections: (i) beam lead fabrication, (ii) silicon thinning, and (iii) chip definition. In Figure 1, a process diagram outlines the fabrication steps. A batch of ultra-thin silicon chips is defined from a square piece SOI (silicon on insulator) wafer measuring 2cm on a side. A dozen such SOI squares are diced from a larger three-inch SOI wafer, which is supplied by Soitec, Inc. An SOI wafer consists of three layers: the thick handle silicon, followed by a buried oxide layer (BOX), and then the thin device silicon. The ultra-thin chips are ultimately defined from the device silicon layer.

<u>Beam Lead Definition</u> Gold beam leads are electroplated atop the device silicon layer. The beam lead thickness can be varied from wafer to wafer; we have fabricated beam leads ranging in thickness from 1.0μm to 10μm thick. The beam lead structures are defined using AZ4330 positive photoresist and an i-line contact mask aligner. The resist is 4μm thick, allowing for at least several a few hundred nanometers of spacing between the top of the beam leads and the top of the resist. Following resist patterning, the beam leads are plated using Techniq 25E plating solution.

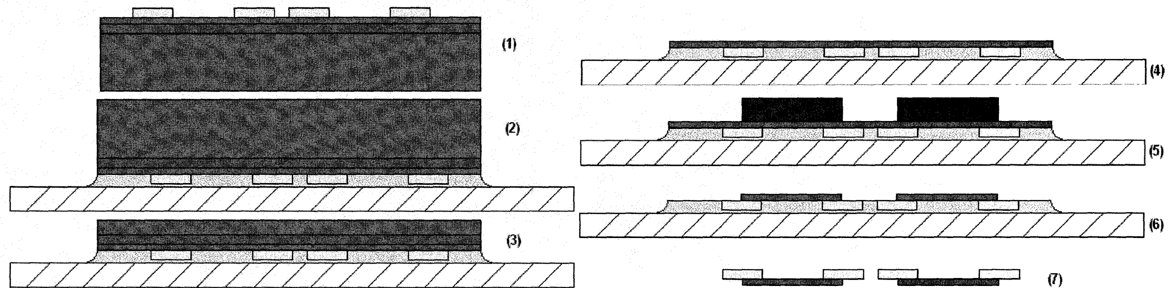


**Figure 1** The fabrication of ultra-thin silicon chips with gold beam leads is summarized in seven steps. In (1), beam leads are fabricated atop the device silicon layer of an SOI wafer. The wafer is then mounted, beam lead side down, on to a quartz carrier (2). The handle silicon and BOX layer are then removed using a combination of mechanical lapping (3) and wet etching (4). The exposed device silicon is then patterned with thick photo resist (5), which serves as an etch mask during a reactive ion etching (RIE) process. After the RIE defines the chip extents (6), the individual chips are separated from the quartz carrier (7).

Silicon Thinning After fabricating the beam leads, we remove the handle silicon from the backside of the wafer in a two-step process. First, we thin the bulk of the handle to 30μm by mechanical lapping. Second, we use a silicon wet etch process to remove the remaining 30μm of handle silicon.

Prior to thinning, we mount the silicon wafer, beam lead side down, atop a 250μm thick quartz carrier. The quartz carrier serves as a rigid support for the wafer, which loses most of its mechanical rigidity after the handle silicon has been removed. A clear mounting wax (Stronghold 7036) adheres the wafer to the carrier. The quartz carrier and clear mounting wax allow for a subsequent backside alignment process, which is necessary for aligning the chip extents with respect to the beam leads.

Next, the wafer/carrier pair is mounted atop a thick metal lapping block using the same clear wax. A mechanical pressure jig then planarizes the wafer and carrier with respect to the lapping block [25]. With the wafer, carrier and lapping block inside, the jig is heated to an internal temperature of 120C, which causes the wax to melt. Pressure is uniformly applied to the wafer via a silicon membrane within the jig for 20 minutes. The jig is then cooled to solidify the planarized wafer and carrier atop the lapping block. After cooling, the pressure is released and the wafer is ready for the first step of the thinning process.

A mechanical lapping process removes the majority of the handle silicon. Our lapping system consists of a Techprep Polishing Machine and a Multriprep Positioning Device, both made by Allied High Tech Products, Inc. A 30μm grit diamond lapping film reduces the handle silicon to within 30μm +/- 5μm of the BOX layer.

A wet etch solution removes the remaining handle silicon. The etchant consists of TMAH (tetramethyl ammonium hydroxide, $(CH_3)_4NOH$), diluted to 8% by weight in de-ionized water, and heated to 60C +/- 3C [26]. The BOX layer serves as an etch stop; the high selectivity of the TMAH etchant between silicon and silicon dioxide ensures that the BOX layer protects the underlying device silicon from the heated etchant.

The etch rate depends significantly upon temperature, and increases considerably with increasing etchant temperature [27,28]. However, the etchant is maintained at a temperature no higher than 60C because the clear mounting wax will soften and re-flow at temperatures beyond 70C. When the handle silicon is etched to within a few microns of the BOX layer, the membrane becomes extremely delicate. At this stage, the thin film may crack and peel if perturbed by flowing wax. At 60C, the wax does not free-flow, yet the etchant is heated sufficiently to maintain a reasonable etch rate.

Silicon Etching After removing the handle silicon, an etch mask is patterned on the backside of the wafer in preparation for reactive ion etching of the device silicon. The etch mask defines the individual chip extents, so it must withstand the high energy ion bombardment and chemical attack associated with the reactive ion etch of the device silicon. Etching of silicon with this chemistry is discussed in detail by Rangelow, et al [29].

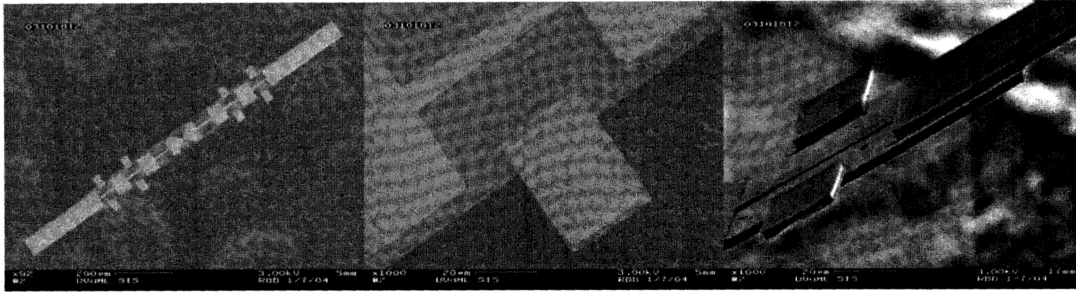

**Figure 2** The left-most micrograph shows a top-down view of an ultra-thin silicon chip with beam leads and integrated RF circuitry. The middle micrograph shows a close-up of a structural beam lead, while the right-most micrograph shows a 3μm thick silicon chip with 2μm thick gold beam leads of various lengths protruding from the perimeters. The longest beam lead extends 250nm beyond the edge of the silicon.

The BOX layer is removed by an HF-based wet etchant prior to photoresist patterning. In order to withstand the RIE conditions, a photoresist mask several microns thick is patterned on the exposed device silicon. For this work, we use 4μm AZ4330 photoresist, which can withstand the extended etch periods and energetic etch conditions associated with the Rangelow etch. These resists etch at a rate of around 80nm/min.

After etching, the individual chips are removed from the quartz carrier by rinsing in acetone, which dissolves the mounting wax. The chips separate from the carrier and collect on a piece of filter paper. Three SEM micrographs of completed chips with beam leads and RF circuitry are shown in Figure 2.

## 7 Conclusion

In order to determine the feasibility of using ultra-thin silicon chips in the microstrip channel of a THz receiver, we mounted several of these chips within our 585GHz mixer blocks, then cooled the blocks to 4.2K in a cryostat. All of the chips featured NbN p-HEBs as the non-linear mixing element, which allowed for current-voltage (I-V) and resistance-temperature (R-T) curves to be measured. These measurements established the presence of electrical continuity through the chips, as well as the non-linear response of the p-HEBs with respect to temperature and current, implying that the chips remain whole and in electrical contact with the block after assembly and cool-down. At the time of writing this paper, RF noise measurements were just beginning to e set up.

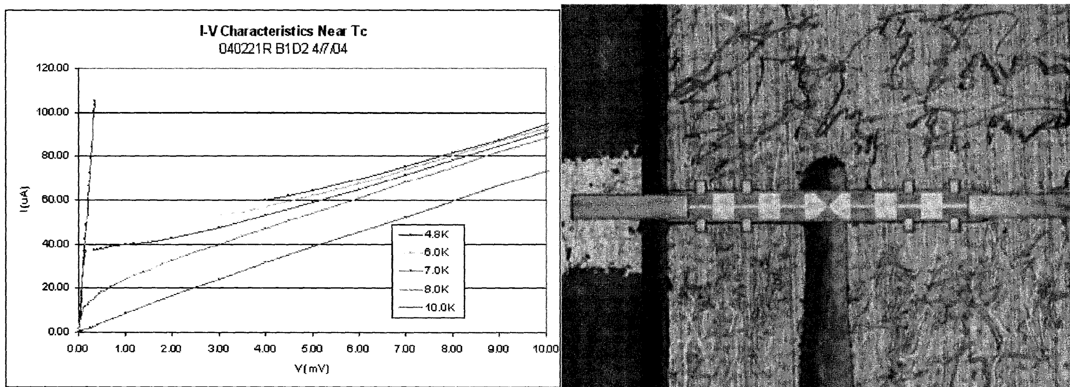


**Figure 3** (Left) Current-Voltage curves from a device mounted within the 585GHz HEB receiver block resemble the curves presented in Figure 1. The batch from which this device was drawn has average dimensions of 164nm long, 4.05μm wide and 4nm thick. The critical current at 4.8K is 105μA, giving a critical current density of $0.66x10^6 A/cm^2$. A 3Ω series resistance is introduced through the measurement connections and the IF filter structures on the ultra-thin silicon chip, as indicated by the steep I-V response observed while the bolometer is superconducting. (Right) An ultra-thin silicon chip rests atop the microstrip channel of our 585GHz test receiver. The beam leads contact the mounting face of the split-block receiver, suspending the chip within the middle of the waveguide channel.

Current-voltage curves from cryogenic testing of a NbN device mounted within a mixer block are shown in Figure 3. We measured I-V curves at several temperatures around the transition region of the R-T curve. The I-V curves presented in Figure 3 demonstrate a self-heating affect within the bolometer that causes a non-linear response for temperatures below $T_c$. In particular, the curves plotted at 4.8K, 6K and 7K all show that the device superconducts until the current within the device exceeds the critical current density. These three curves also demonstrate the self-heating affect where current flow, less than the value of the critical current, dissipates enough heat within the normal-state microbridge to maintain a local temperature above the critical temperature. These I-V measurements demonstrate our ability to fabricate hot-electron bolometers on ultra-thin silicon chips with beam leads, mount those chips within the microstrip channel of a metal waveguide block, and cool the entire assembly down to liquid helium temperatures.

We developed a process for fabricating ultra-thin silicon chips based on SOI substrates that has yielded robust detector chips as thin as 1.6μm. This process also permits the definition of non-rectangular chip geometries with control of final chip dimensions to better than +/-2um. The chips feature RF circuitry, including filter choke segments and bowtie antennae. We have demonstrated ultra-thin silicon chips as long as 2mm (1.6μm thick) and gold beam leads as long as 250μm (1μm thick).

Importantly, the beam leads allow ultra-thin silicon chips to be incorporated into the design of terahertz receivers. There exist no circuit contacting methods capable of providing robust electrical continuity to an ultra-thin silicon chip that would not damage the chip or secure it permanently to the receiver housing except beam leads. By using beam leads to secure ultra-thin silicon chips within a microstrip channel, the complexity of the microstrip channel is reduced from an RF design standpoint because most of the microstrip channel volume may be assumed to be vacuum. Current terahertz mixer designs must consider the effects of a thick dielectric substrate inside the microstrip channel when analyzing the propagation and mixing of signals within the receiver. When using ultra-thin silicon chips to position the submillimeter-wave circuitry within the microstrip channel, only 3μm or less of silicon need be considered instead of tens of microns or more of quartz. The machining of waveguide components is also greatly simplified when using ultra-thin silicon chips since complex structures need not be machined within the waveguide channel in order to support thick quartz chips, conductive wire gaskets, or other non-ideal structures that would require the microstrip channel shape to deviate from rectangular. Our ultra-thin silicon beam lead technology is also an excellent match with our existing laser micromachining capabilities at the University of Arizona. We are presently working on non-rectangular SOI chip array designs with asymmetric IF/ground mounts scalable to several THz.

**8 References**

[1] A. R. Kerr, S.-K. Pan, E. F. Lauria, A. W. Lichtenberger, J. Zhang, M. W. Pospieszalski, N. Horner, G. A. Ediss, J. E. Effland, R. L. Groves, *15th Inter. Symp. Space THz Tech.*, Northampton, MA, April 2004

[2] S.-K. Pan, A. R. Kerr, M. W. Pospieszalski, E. F. Lauria, W. K. Crady, N. Horner, Jr., S. Srikanth, E. Bryerton, K. Saini, S. M. X. Claude, C. C. Chin, P. Dindo, G. Rodrigues, D. Derdall, J. Z. Zhang, A. W. Lichtenberger, *15th Int. Symp. Space THz Tech.*, Northampton, MA, April 2004

[3] C.E. Groppi, C.K. Walker, D. Golish, A. Hedden, G. Narayanan, A.W. Lichtenberger, *Astronomical Telescopes and Instrumentation 2002: Topics in Astronomy: Information Technologies, MMW and Sub-MMW Detectors, Solar Astrophysics, Non-EM Astronomy, Exo-Planet Detection, and Astrobiology*, Waikoloa Village, HI, Aug. 2002

[4] C.K. Walker, C.E. Groppi, C.Y. Drouet d'Aubigny, C. Kulesa, A. Hedden, D. Golish, D.E. Prober, S. Yngvesson, J. W. Kooi, A. W. Lichtenberger, *Astronomical Telescopes and Instrumentation 2002: Topics in Astronomy: Information Technologies, MMW and Sub-MMW Detectors, Solar Astrophysics, Non-EM Astronomy, Exo-Planet Detection, and Astrobiology*, Waikoloa Village, HI, Aug. 2002

[5] A. Hedden, C. K. Walker, D. Golish, C. Drouet d'Aubigny, C. Groppi, C. Kulesa, D. Prober, J. W. Kooi, G. Narayanan, A. Lichtenberger, A. Datesman, *15th Inter. Symp. on Space THz Tech.*, Northampton, MA, April 2004

[6] A. Hedden, C. K. Walker, D. Golish, C. Drouet d'Aubigny, C. Groppi, C. Kulesa, D. Prober, J. W. Kooi, G. Narayanan, A. Lichtenberger, A. Datesman, *15th Inter. Symp. on Space THz Technology*, Northampton, MA, April 2004

[7] J.W. Kooi , C.D. d'Aubigny , R.B. Bass, C. Walker, A.W. Lichtenberger, "Broad Bandwidth Suspended Membrane Waveguide Transition for use in Silicon Micromachined Mixer blocks at THz Frequencies," *14th Inter. Symp. on Space THz Tech.*, Tucson, AZ, April 2003

[8] R.B. Bass, A.W. Lichtenberger, R. Weikle, J.W. Kooi, C.K. Walker, S.-K. Pan, *6th Euro. Conf. on App. Supercond.*, Sorrento, Italy, Sept. 14, 2003

[9] R.B. Bass, J.C. Schultz, A.W. Lichtenberger, C. Walker, J. Kooi, *14th International Symposium on Space THz Technology*, Tucson, AZ, April 2003

[10] Y. Taur and A. R. Kerr, *App. Phys. Lett.*, 32 **11**, 775-777, 1978

[11] C. E. Tong, R. Blundell, S. Paine, D. C. Papa, J. Kawamura, X. Zhang, J. Stern and H. G. LeDuc, *IEEE Trans. Micro. Theory and Tech.*, 44, 1548-1556, 1996

[12] A. R. Kerr, S.-K. Pan, S. Whiteley, M. Radparvar and S. Faris, *IEEE Inter. Micro. Symp. Digest*, 851-854, 1990

[13] A. R. Kerr, S.-K. Pan and A. W. Lichtenberger and D. M. Lea, *IEEE Micro. Guided Wave Lett.*, 2 **11**, 454-456, 1992

[14] M.P. Lepselter, *Bell Laboratories Record*, 299-304, Oct., 1966

[15] R. Blundell, C.-Y.E. Tong, D.C. Papa, R.L. Leombruno, X. Zhang, S. Paine, J.A. Stern, H.G. LeDuc, B. Bumble, *5th Inter. Symp. on Space Terahertz Tech.*, Ann Arbor, MI, 27-37, 1994

[16] R. Blundell, C.-Y.E. Tong, D.C. Papa, R.L. Leombruno, X. Zhang, S. Paine, J.A. Stern, H.G. LeDuc, B. Bumble, *IEEE Trans. Micro. Theory and Tech.*, 43 **4**, April 1995

[17] C.E. Tong, R. Blundell, S. Paine, D.C. Papa, J. Kawamura, X. Zhang, J.A. Stern, H.G. LeDuc, *IEEE Trans. on Micro. Theory and Techn.*, 44 **9**, Sept. 1996

[18] R. Blundell, C.-Y.E. Tong, J.W. Barrett, J. Kawamura, R.L. Leombruno, S. Paine, D.C. Papa, X. Zhang, J.A. Stern, H.G. LeDuc, B. Bumble, *6th Inter. Symp. on Space Terahertz Tech.*, Pasadena, CA, 123-133, March 1995

[19] C.-Y.E. Tong, R. Blundell, D.C. Papa, J.W. Barrett, S. Paine, X. Zhang, J.A. Stern, H.G. LeDuc, *6th Inter. Symp. on Space Terahertz Tech*, 295-304, Pasadena, CA, March 1995

[20] J. Kawamura, R. Blundell, C.-Y.E. Tong, D.C. Papa, T.R. Hunter, S. Paine, F. Patt, G. Gol'tsman, S.Cherednichenko, B. Voronov, E. Gershenzon, *IEEE Trans. Micro. Theory and Tech.*, 48 **4**, April 2000

[21] G. de Lange, B.D. Jackson, M. Eggens, H. Golstein., W.M. Laauwen, L. de Jong, S. Kikken, C. Pieters, H.. Smit, D. Van Nguyen, M. Kroug, T. Zijlstra, T.M. Klapwijk, *14th Inter. Symp. on Space Terahertz Tech.*, Tucson, AZ, April 2003

[22] K.E. Peterson, "Silicon as a Mechanical Material," *Proceedings of the IEE*E, pp. 420-457, 70 (5), 1982

[23] K.R. Virwani, A.P. Malshe, W.F. Schmidt, D.K. Sood, "Young's modulus measurements of silicon nanostructures using a scanning probe system: a non-destructive evaluation approach," *Smart Materials and Structures*, 12, pp. 1028-1032, December 2003

[24] J.W. Kooi, C.K. Walker, and J. Hesler, "A Broad Bandwidth Suspended Membrane Waveguide to Thinfilm Microstrip Transition", *9th Inter. Conf. on Terahertz Electronics*, Oct. 2001

[25] W.L. Bishop, D.M. Summers and A.W. Lichtenberger, "Precision Techniques for Whole Wafer Dicing and Thinning of Superconducting Mixer Circuits," *IEEE Transactions on Applied Superconductivity*, 11 (1), pp. 171-174, March 2001

[26] O. Tabata, R. Asahi, H. Funabashi, K. Shimaoka, S. Sugiyama, "Anisotropic Etching of Silicon in TMAH Solutions," *Sensors and Actuators A*, 34, pp. 51-57, 1992

[27] P.-H. Chen, H.-Y. Peng, C.-M. Hsieh, M.K. Chyu, "The Characteristic Behavior of TMAH Water Solution for Anisotropic Etching of Both Silicon Substrate and $SiO_2$ Layer," *Sensors and Actuators A*, 93, pp. 132-137, 2001

[28] I. Zubel, M. Kramkowska, "The Effect of Isopropyl Alcohol on Etching Rate and Roughness of (1 0 0) Si Surface Etched in KOH and TMAH Solutions," *Sensors and Actuators A*, 93, pp. 138-147, 2001

[29] I.W. Rangelow, P. Hudek, F. Shi, "Bulk Micromachining of Si by Lithography and Reactive Ion Etching (LIRIE)," *Vacuum*, 46, pp. 1361-1369, 1995