Design, Fabrication and Characterisation of High Power HBV Diodes

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***Abstract*— We present design and analysis of material structures and device geometries for heterostructure barrier varactor diodes (HBVs) for high-power frequency multipliers. The methods aim at finding optimum epitaxial layer structures with respect to diode power handling capability and efficiency. A distributed device geometry for further increasing the output power levels whilst maintaining acceptable device temperatures is also presented. Finally, an electro-thermal HBV model with the ability of incorporating temperature-dependent device parameters is used to simulate the introduced devices, followed by a design example of a 3×4-barrier high-power HBV diode.**

I. Introduction

Applications in the millimeter wavelength range have in the last decades increased, e.g. radio astronomy, high-speed wireless communications, medical and biological imaging and surveillance systems, but a major problem at these frequencies is the lack of power sources. One promising approach is to use a frequency multiplier [1] with high-power heterostructure barrier varactors (HBVs) [2], [3], as HBVs use a heterojunction as a blocking element and therefore several barriers can be grown epitaxially, to increase the breakdown voltage and thereby the power handling capacity. This property favors HBVs rather than Schottky diodes for high-power, high-order frequency multiplication [4], [5]. The vast majority of HBV multipliers this far have been tripler circuits and efficiencies of 12% at the output frequency of 250 GHz in InP-based system have been achieved [6], [7].

State-of-the-art high-frequency HBVs are fabricated using $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ on semi-insulating InP substrates [8]. This system offers higher electron velocities and mobilities compared to GaAs-based systems, which means lower series resistance and higher conversion efficiency. For higher input powers more barriers need to be stacked, resulting in a comparatively thick epitaxial layer. However, because of the strong correlation between HBV performance and material properties, the main difficulty is to maintain a high quality when growing thick epitaxial layers. Also, in high-power applications, a large amount of input power is dissipated as heat in the devices, resulting in high temperatures, causing high leakage currents and self-heating problems in HBVs [9]. The main disadvantage of using an InP lattice matched system in high-power applications is the poor thermal conductivity that causes a high temperature inside the mesa, leading to a lower efficiency [10]. Therefore the maximum allowable absorbed power per barrier is limited by the maximum acceptable temperature inside the mesa. One solution could be to fabricate HBVs on substrates having a higher thermal conductivity [11], or to apply a distributed topology structure that improves the heat transfer through the device patterned on an InP-based [12]. We here introduce parameters important for the diode performance for high-power applications, and present design methods for epitaxial layer structures, circuits, materials and geometries in order to reach high power handling capabilities and diode efficiencies. In order to assess and analyze the designs, we perform simulations using an electro-thermal model which updates the device temperature and temperature-dependent device parameters self-consistently [13]. Finally, we present a 3-barrier HBV material, Chalmers MBE995, designed for high output power level, with a wide and smooth I-V curve and a maximised elastance swing which would result in higher efficiency.

II. Device Model

A. Basic Principle

A general InP-based HBV layer structure is shown in Table I. The modulation and barrier layers consist of InGaAs and InAlAs, respectively. The layer sequence 2-5 can be repeated N times to create an N-barrier HBV. This structure with a pseudomorphic (3nm) AlAs layer in the center of the barrier has a high potential barrier, resulting in a very low leakage current [14].

The performance of a varactor device is associated with the dynamic cut-off frequency, f_c, which determines the conversion efficiency [15].

$$f_c = \frac{S_{max} - S_{min}}{2\pi R_s} \tag{1}$$

TABLE I
A TYPICAL ONE-BARRIER HBV LAYER STRUCTURE

Layer No.	Layer	Thickness [nm]	Doping level [cm^{-3}]
7	Contact	200	$\sim 10^{19}$
6	Modulation	400	6×10^{16}
5	Spacer	5	undoped
4	Barrier	20	undoped
3	Spacer	5	undoped
2	Modulation	400	6×10^{16}
1	Buffer	500	$\sim 10^{19}$
	Substrate		

where S_{max} and S_{min} are the maximum and minimum elastance, respectively, during a pump cycle and R_s is the series resistance.
For a typical HBV the parallel plate capacitor model can be used to estimate the elastance,

$$S = \frac{1}{C} = \frac{N}{A}\left(\frac{b}{\varepsilon_b} + \frac{2s}{\varepsilon_d} + \frac{w}{\varepsilon_b}\right) \tag{2}$$

Here N is the number of barriers, A is the cross sectional area, b, ε_b, s and ε_d are the thickness and permittivity of the barrier and spacer layer, respectively, and w is length of the depleted region.
The series resistance is voltage-dependent through the extension of the depleted region and also depends on the device geometry, material parameters and the temperature. For a planar HBV with two series-connected mesas, Figure 1, the series resistance can be estimated as

$$\begin{aligned} R_s(T) = {} & R_{mesa}(T) + R_{buffer}(T) + R_{cl}(T) \\ & + R_c + R_{finger} \end{aligned} \tag{3}$$

where R_{mesa} is the resistance of the layers inside the mesa, R_{buffer} is the spreading resistance in the buffer layer, R_{cl} is the resistance of the contact layers, R_c is the ohmic contact resistance, and R_{finger} is the resistance of the air bridges.
Any of these resistances can be calculated as

$$R = \frac{t}{A\sigma} \tag{4}$$

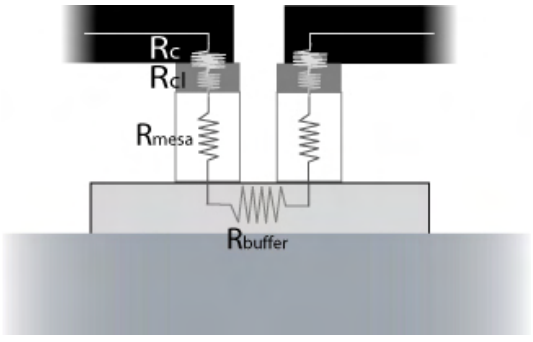


Fig. 1. Contributions to the series resistance of a planar HBV diode.

where t is the thickness and σ is the electrical conductivity of the layer. The electrical conductivity depends on the doping concentration and the electron mobility as

$$\sigma = q \cdot N_d \cdot \mu_e(N_d, T) \tag{5}$$

where $\mu_e(N_d, T)$ is the electron low-field mobility, calculated from the following empirical model [16]

$$\mu_e(N_d, T) = \mu_{min} + \frac{\mu_{max}(T_0)(\frac{T_0}{T})^{\theta_1} - \mu_{min}}{1 + \left(\frac{N_d}{N_{ref}(T_0)(\frac{T}{T_0})^{\theta_2}}\right)^{\lambda}}. \tag{6}$$

Here μ_{min}, μ_{max}, N_{ref}, λ, θ_1 and θ_2 are fitting parameters available for most common III-V materials, and $T_0 = 300K$.

B. Electro-Thermal Model

Simple analytical expressions can be used for initial estimations and investigations about thermal properties, but in order to properly design and analyze HBVs, especially for high-power applications, it is necessary to employ combined electrical and thermal simulations. Here we demonstrate the use of an electro-thermal model, implemented in Agilent Advanced Design System (ADS) [13].
The voltage across an HBV as a function of the charge Q stored in the device is calculated from the quasi-empirical Chalmers HBV model [17]

$$\begin{aligned} \frac{V(Q)}{N} = {} & \frac{bQ}{\varepsilon_b A} + 2\frac{sQ}{\varepsilon_d A} \\ & + \text{Sign}(Q) \cdot \left(\frac{Q^2}{2qN_d\varepsilon_d A^2} \right. \\ & \left. + \frac{4k_B T}{q}\left(1 - exp\left[- \frac{|Q|}{2L_D A q N_d} \right]\right)\right) \end{aligned} \tag{7}$$

where k_B is the Boltzmann constant, q is the elementary charge, and L_D is the intrinsic Debye length. The displacement current is

$$i(t) = \frac{\partial Q}{\partial t}. \tag{8}$$

For GaAs-based HBVs that exhibit relatively low effective barrier height, the conduction current is dominated by thermionic emission [9], [17], but for InP-based HBV devices, the current transport is rather dominated by electron tunnelling through the barrier.

By using an equivalent electro-thermal circuit, the device temperature T can be treated like any other control voltage [18]. Now, the electrical properties of an HBV can be modeled with harmonic balance simulations using the equivalent circuit in Figure 2 (left) together with (7), combined with appropriate expressions for the conduction current and the series resistance. The thermal resistance R_{th} is calculated by using 3-D finite element simulations. The thermal capacitance C_{th} models the thermal storage of the device, so that the thermal time constant is $\tau_{th} = R_{th} \cdot C_{th}$.

The thermal properties are modeled with the electro-thermal equivalent circuit displayed in Figure 2 (right). We have implemented the electro-thermal model in ADS by using an extra nonlinear port.

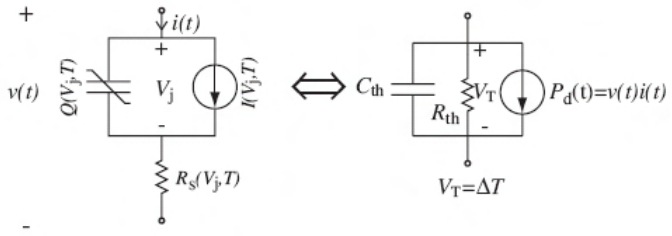


Fig. 2. Electrical equivalent (left) and electro-thermal equivalent circuit model (right) for harmonic balance simulations.

C. Thermal Resistance and Device Geometry

It is obvious that the power handling capacity of the conventional HBV is limited to the maximum allowable temperature inside the active part of the diode for a certain amount of input power [10]. We have calculated the temperature distribution for conventional planar HBVs using 3-D finite element simulations. We assume that 1200 mW is absorbed in the device. The total required number of barriers needed to be able to handle this power level is considered to be 12 [10], which, in a conventional planar HBV, are divided equally into two series-connected mesas, see Figure 3. Since the HBV is to be flip-chip mounted onto the embedding circuitry, only the contacting pads are assumed to be perfectly heat-sunk, and due to symmetry reasons only a quarter of the geometry is displayed.

As can be seen in Figure 3 the maximum rise temperature for this power level is $230°$C, higher than the acceptable level, which is approximately $150°$C.
The thermal resistance, R_{th}, is calculated by using 3-D finite element simulations and equal to the maximum rise temperature divided by the total dissipated power in the device, $R_{th} = 190\ K/W$.

III. Results

A. Distributed Geometry

In order to lower the temperature to an acceptable level, we propose the topology shown in Figure 4 [12]. This geometry consists of 16 mesas, 4 connected in parallel and 4 in series. This gives a thinner epitaxial thickness which is also advantageous from a material growth point of view, since it is difficult to realize a thick, high-quality material in this particular material system.

Figure 4 shows that the maximum temperature has decreased substantially, to $115°$C. This is mainly because of the heat source being distributed over a larger area. The distance between the fingers is larger for the inner pair. This is to avoid a higher temperature on these two fingers compared to the ones at the periphery. Also, in each finger, the two inner mesas are not connected directly, because of the gold pad extending down to the substrate to divert heat more efficiently for the innermost mesas. The distance between two nearest mesas is chosen as short as possible with respect to limitations in processing and parasitic capacitances, since a wider separation increases the series resistance in the structure, and thereby lowers the diode conversion efficiency.
By using 3-D finite element, the thermal resistance is calculated $R_{th} = 100\ K/W$ for this kind of distributed geometry, which is lower than in the case of conventional planar HBV.

B. Epilayer Structure Optimization

The performance of an HBV device depends on the dynamic cut-off frequency, which is the main figure of merit for pure varactor multipliers. Another parameter which influences the device performance is the conduction current, especially in GaAs-based systems. A Poisson/Schrödinger calculation of the current density for a single-barrier InP-based HBV as a function of the barrier thickness shows that the barrier thickness which gives the lowest conduction current by including a thin central AlAs layer inside the barrier is around $20nm$, this thickness for GaAs-based HBV is about $15nm$ [14].

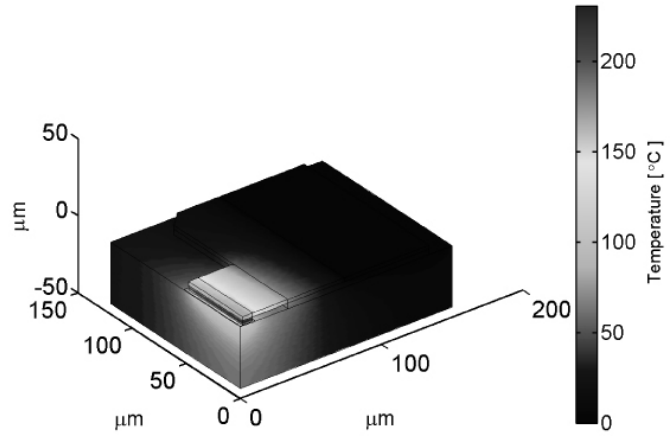


Fig. 3. Temperature distribution for a conventional planar HBV, InGaAs on InP substrate.

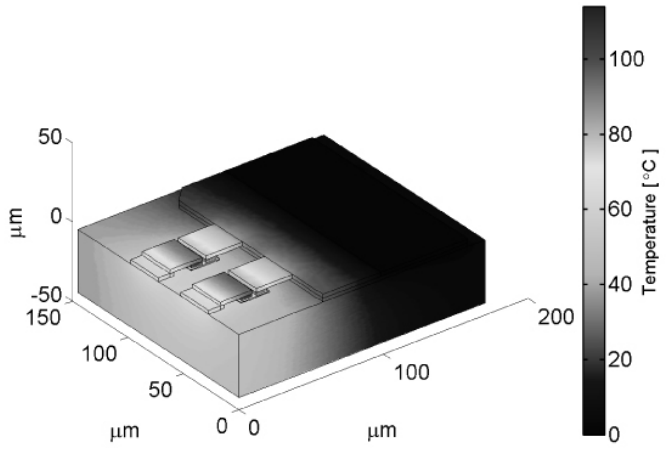


Fig. 4. Temperature distribution for the novel InGaAs on InP HBV, consisting of 16 mesas.

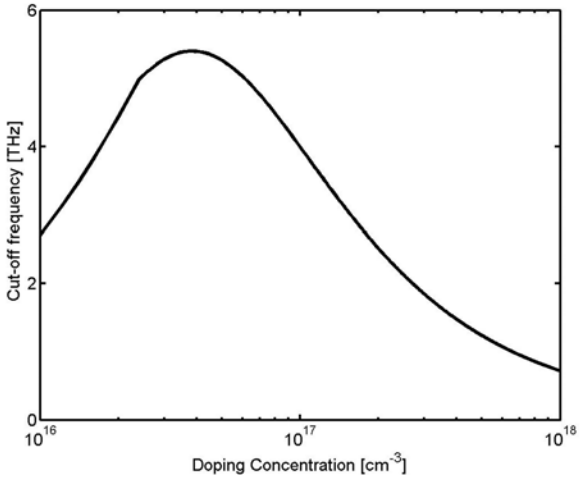


Fig. 5. Cut-off frequency for a 3-barrier planar HBV versus doping concentration.

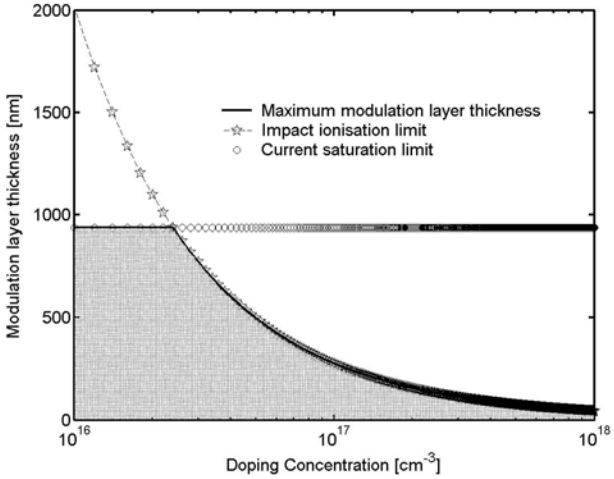


Fig. 6. Maximum modulation layer thickness versus doping for both impact ionization and current saturation conditions.

From (1) it can be seen that for optimizing the efficiency, one should maximize the elastance swing, $S_{max} - S_{min}$, and minimize the series resistance, R_s.

The maximum elastance, S_{max}, is directly proportional to the modulation layer thickness. However, a thicker layer leads to a higher series resistance which results in a lower efficiency. For high-power applications the thickness of the modulation layer is determined by considering impact ionization at high electric fields, while still making sure that it is thinner than current saturation thickness limit [19].

For impact ionization, the maximum modulation layer thickness can be calculated as

$$w_{max} = \frac{\varepsilon_d E_{d,max}}{qN_d} \tag{9}$$

where $E_{d,max}$ is the maximum electric field in the modulation layer at the voltage where breakdown occurs and can be described as

$$E_{d,max} = \frac{a}{1 - b\log\left(\frac{N_d}{N_{d,ref}}\right)} \tag{10}$$

where $a = 3{\times}10^7$, $b = 0.28$ and $N_{d,ref} = 1.5{\times}10^{16} cm^{-3}$ are the fitting parameters for Chalmers MBE InP based materials. Current saturation limits the thickness according to

$$w_{max} \approx \frac{v_{max}}{8 f_p} \tag{11}$$

where v_{max} is the saturated electron velocity [19], [20].

From (1), (2) and (9) we observe a necessary trade-off between doping concentration and thickness of the modulation layer, in order to achieve an optimum cut-off frequency and thereby the highest efficiency. Figure 5 shows how f_c and thereby η vary with doping concentration for a certain number of barriers, in this case a 3-barrier planar HBV with four series-connected mesas distributed in four fingers and a total diode cross sectional area of $700 \mu m^2$, Figure 4.

The modulation layer thickness has been calculated according to (9) for each value of doping concentration so that impact ionization occurs before current saturation. Figure 6 shows the modulation layer thickness versus doping concentration for a 3-barrier material.

The series resistance of the active part of the diode also varies with the doping, where R_{buffer} and R_{mesa} constitute the main contributions to the total resistance, respectively, especially for structures with thin buffers. According to (3), the total resistance can be calculated for a given area and doping concentration value with the respective maximum modulation layer thicknesses.

The device breakdown voltage depends on the doping level and the related maximum modulation thickness, and can be described as

$$V_{BD,max} = N\varepsilon_d E_d \left(\frac{b}{\varepsilon_b} + \frac{2s}{\varepsilon_d} + \frac{w_{max}}{2\varepsilon_d} \right). \tag{12}$$

The breakdown voltage and thereby the power handling capacity can also be increased by increasing the number of barriers, limited by the maximum allowed temperature inside the mesas [10].

C. Design Examples

We now use the presented optimization methods and then the electro-thermal model to further demonstrate the design of high-power HBV diodes. The material structure is optimized for a 100 GHz frequency tripler. We assume the distributed geometry, Figure 4, with 3-barrier mesas and a total cross sectional device area of $A = 700 \mu m^2$. Plot of the cut-off frequency versus the doping concentration obtained from the models presented shows that $N_d = 7{\times}10^{16} cm^{-3}$ gives the highest cut-off frequency. This corresponds to a modulation layer thickness of $370nm$, which is thinner than the current saturation limit, and a total breakdown voltage of $90\ Volt$.

This InP-based material, Chalmers MBE995, has been grown, with a slight difference in doping, $N_d = 1{\times}10^{17}\ cm^{-3}$. To verify the quality, a test diode consisting of one mesa has been

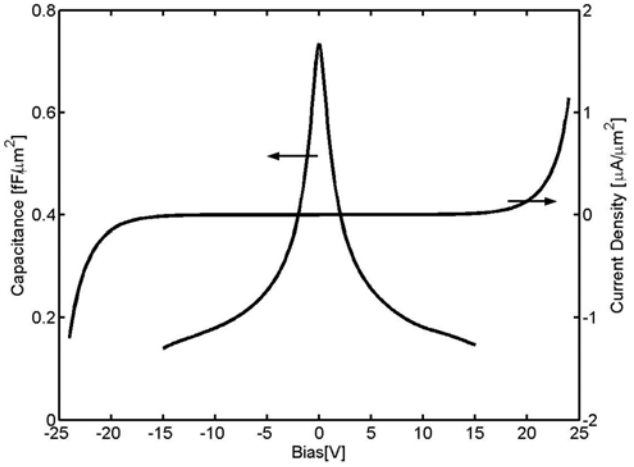


Fig. 7. C-V and I-V for a high power designed material, Chalmers MBE995.

fabricated by using this material, Figure 7 shows C-V and I-V measurements for this 3-barrier diode. This device has a breakdown voltage of $24\ Volt$, and an excellent C_{max}/C_{min} ratio of 5.2.
SEM image of the high power diode with distributed geometry, Figure 4, is shown in Figure 8.
For this material, we have used the electro-thermal model [13]to estimate the diode efficiency and the maximum temperature inside the device for a certain input power level for a pump frequency of 33 GHz.

The series resistance is calculated with (3) with considering four series-connected mesas distributed in four fingers, Figure 4, and assuming $R_c{\cdot}A = 100\mu m^2$ per mesa. The room temperature value is 4Ω and the increase in the series resistance due to self-heating is approximately 14%.

The conversion efficiency excluding circuit losses with and without effect of junction temperature is shown in Figure 9a and the corresponding junction temperature is displayed in Figure 9b. Approximately $2W$ of input power can be handled by this device without reaching the breakdown voltage per barrier or an unacceptable device temperature.

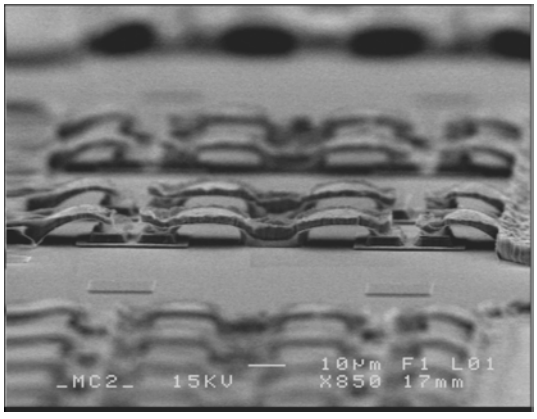
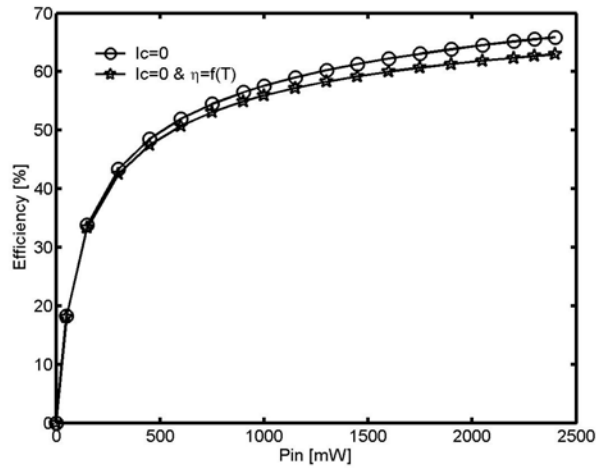
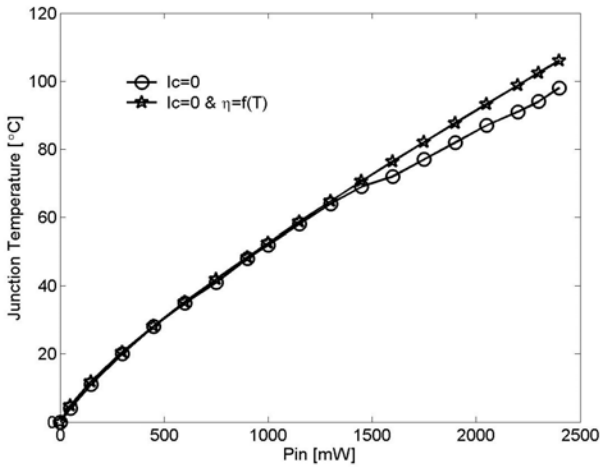


Fig. 8. SEM image of high power HBV diodes.



(a)



(b)

Fig. 9. Simulated diode efficiency (a) and the corresponding junction temperature (b) for a 12-barrier high-power HBV, Chalmers MBE995, with an area of $A = 700\mu m^2$ distributed in four fingers.

IV. Conclusions

To be able to handle high input power levels with HBV diode multipliers for millimeter and submillimeter wavelength applications, we have presented a device model, a material structure optimization method, and a temperature-dependent electro-thermal model. To further decrease the maximum temperature rise in the device we have also presented a distributed geometry for which thermal calculations show that the maximum temperature is drastically decreased compared to the conventional planar HBV. Finally, using the presented models, a high-power InP-based material has been designed and fabricated. The measured DC characteristics are excellent. The electro-thermal model has been employed to simulate the diode performance of the fabricated material and to further demonstrate the design method.

V. Acknowledgment

This work has been supported by the European Space Agency through the project HBV Devices and MMICs, the Swedish Defence Research Agency, FOI, through the Nano Technology program, the EU INTERACTION program and SSF-HSEP.

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