Progress towards an integrated 380 GHz planar Schottky diode heterodyne receiver on single substrate

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Abstract— : **We report on the design, build and characterisation of an integrated submillimetre wave receiver featuring a 380 GHz sub-harmonic mixer and a 190 GHz frequency doubler on a single quartz based microstrip circuit. The integrated circuit uses two separate planar Schottky diode components to perform the doubling and 2nd harmonic mixing. Measurement results give best double sideband mixer noise temperatures of 1625 K at 372 GHz, and a corresponding mixer conversion loss of 8 dB. The measured instantaneous RF bandwidth extends from 368 GHz to 392 GHz, in good agreement with simulations. This work represents the first demonstration of a single substrate integrated mixer/multiplier at submillimetre wavelengths.**

***Index Terms*— Submillimetre wave receiver, integrated mixer/multiplier, planar Schottky diodes.**

I. Introduction

Submillimetre receiver arrays are expected to enhance the capabilities of future airborne and space-borne atmospheric limb sounding instruments. For example, Schottky diode based heterodyne array instruments will not only allow observations with greater sensitivity than single pixel sounders, but will also provide vertically and horizontally resolved information on global distributions of key species in the Earth's upper troposphere and lower stratosphere (e.g., the STEAM-R concept [1]). One way of avoiding difficulties associated with local oscillator (LO) generation and injection in an array of receivers is to integrate the mixer and LO provision within each pixel; in principle this will allow reduced size, mass and power consumption, and an easily extendable array concept. Here we investigate the integration of a subharmonic mixer with a frequency doubler based on planar Schottky diodes, since this is the method generally used to provide the local oscillator signal in a sub-millimetre receiver.

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Due to the efficient and mature modelling techniques for planar Schottky diode devices at submillimetre wavelengths, coupled with the monotonic increase in available computing power, mixer and multiplier circuits which were previously designed and packaged independently are now being incorporated in a single housing [2]. However, no mixer/multiplier device integrated on a single circuit carrier has been reported so far in the submillimetre wave domain. We report here for the first time the development of an integrated 380 GHz sub-harmonic mixer/doubler using a single quartz substrate.

II. 380 GHz integrated mixer/multiplier design architecture

The 380 GHz integrated mixer/doubler design concept features a balanced doubler stage and a sub-harmonic mixer stage in a single circuit, as illustrated in Fig.1. The integrated circuit performs the second harmonic mixing between the output LO signal of the doubler stage and the RF input signal of the mixer stage. The main advantage of using a balanced diode configuration is the possibility of decoupling the input matching circuit for the fundamental frequency, circa 95 GHz, and the RF input matching circuit without additional filtering elements, as shown in Fig.1. This is due to the natural input and output mode separation of a balanced configuration, further detailed in [3]. The reduced dimensions of the microstrip channel help to prevent the third and fifth harmonics, generated by the doubler diodes in a parasitic TE mode, from propagating towards the mixer diodes. The fourth harmonic, generated in a quasi-TEM mode, is strongly rejected by the RF low-pass filter as it falls into the RF frequency band. In the selected approach, each series pair of the balanced doubler diodes can be biased independently from the sides of the input waveguide, rather than from the central microstrip line usually used in balanced doubler architectures [4]. A bond wire is used to provide both a DC ground for the doubler diodes and an IF ground for the sub-harmonic mixer diodes via the central microstrip line. Its length is set as a quarter wavelength at the LO frequency in order to affect minimally its propagation. The bond wire does not significantly disturb the RF matching circuit since the RF signal is already attenuated strongly by the low pass filter at this point.

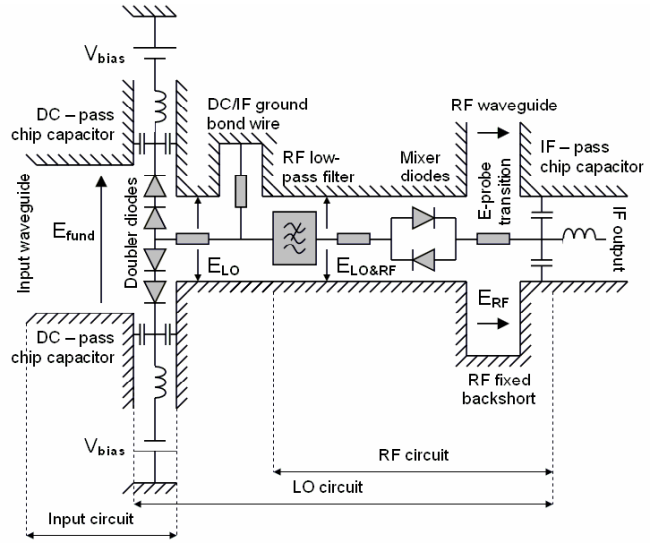


Fig.1. Schematic diagram of the integrated receiver. RF input is from 370 to 390 GHz, whereas the fundamental input frequency is about 95 GHz.

The design methodology uses a combination of linear/non-linear circuit simulations (Agilent ADS [5]) to optimize and compute the performances of the circuit, and 3D EM simulations (Ansoft HFSS [6]) to model accurately the diodes and waveguide structures.

As a first step, the electrical models for the doubler and mixer diodes are linearised around their optimum operating point. The electrical parameters of the doubler's VDI SB6T4-R1 varactor diodes [7] are a series resistance of $R_s = 5\ \Omega$, saturation current I_{sat} = 146 pA, a zero voltage capacitance C_{jo} = 42 fF, an ideality factor $\eta = 1.2$, a built-in potential $V_{bi} = 0.83$ V and an anode diameter $d = 6\ \mu m$. An additional linear capacitance corresponding to approximately 4% of C_{jo} is introduced in parallel to the non-linear plate capacitance of the junction to include the edge effect [8]. Considering an available input power of 9 mW at 95 GHz and a bias voltage of -3 V per diode, an ideal input embedding impedance of Z_{in} = 8.5 + j.68, and an output embedding impedance of Z_{out} = 13 + j.34 at a frequency of 190 GHz is found for a single barrier.

For the subharmonic mixer, the electrical parameters of VDI's SC1T9-D20 diodes used are a series resistance R_s = 10 Ω, a zero voltage junction capacitance of C_{jo}= 2.5 fF, saturation current I_{sat} = 30 fA, ideality factor η=1.25 and built-in potential V_{bi} = 0.73 V. Considering an optimum LO power level of 1.5 mW, a set of non-linear simulations gives an ideal embedding impedances of approximately Z_{RF} = 47+j.46 at RF frequencies and Z_{LO} = 63+j.121 at LO frequencies. The IF load impedance is set to 100 Ω.

In a second step, each part of the circuit is modelled electromagnetically with HFSS, and imported in ADS for further optimisation. In order to retrieve the S-parameters at the level of each Schottky barrier in the doubler and mixer devices, micro-coaxial probe ports are introduced [9]. A simple low-pass filter is required to prevent the RF signal from leaking into the doubler stage and to transmit the LO signal to the mixer stage. Single layer chip capacitors (model Tcap® from DLI [10]) with minimum dimensions of 254 µm x 254 µm x 76 µm are used to present a shunt resonance at fundamental and LO frequencies for the doubler stage, allowing independent DC bias to be applied to each branch. On the mixer stage, a similar chip capacitor is reduced in size using a dicing saw in order to present a shunt resonance at LO and RF frequencies, allowing the transmission of the IF signal to the output.

The circuit is optimized for best coupling of the fundamental signal to the doubler diodes, the LO signal from the output of the doubler stage to the mixer stage, and the RF signal to the mixer diodes. As an example, the total coupling efficiency between the doubler and the mixer diodes is presented in Fig. 2. It is obtained by summing the individual coupling efficiencies between each of the doubler diodes and mixer diodes, and is estimated to be between 60 % and 70%, from 186 GHz to 196 GHz. The simulated RF input return losses of mixer circuit stage are given in Fig.3, showing a predicted RF bandwidth extending at least from 370 GHz to 390 GHz.

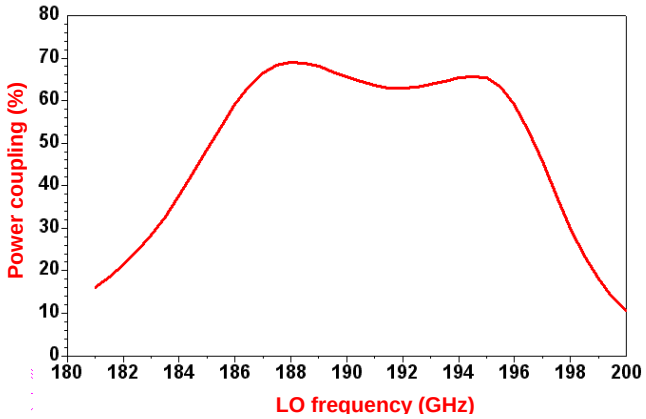


Fig.2. Predicted coupling efficiency between the doubler and the mixer stages at LO frequencies.

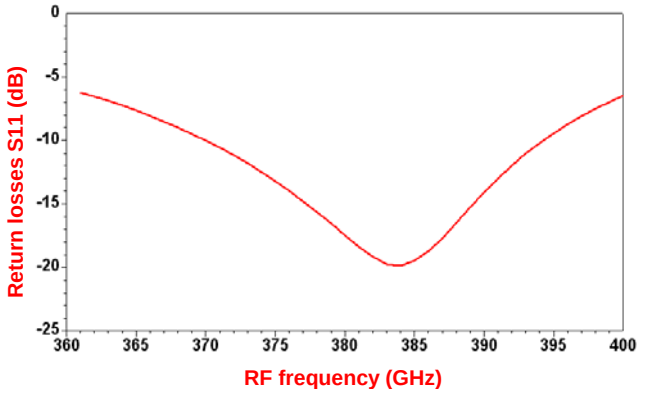


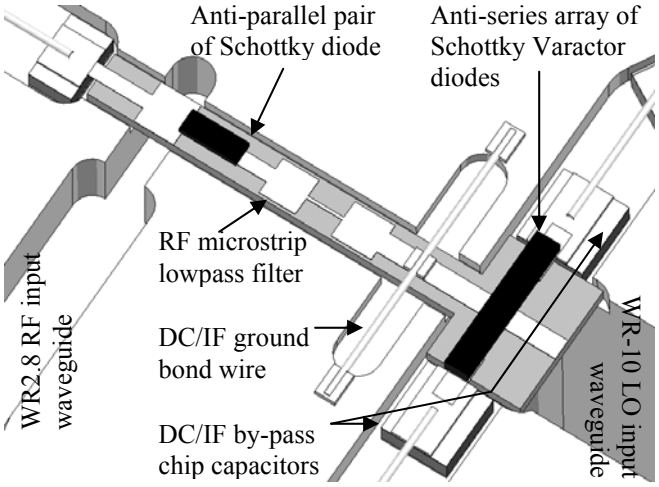
Fig.3. Predicted waveguide return losses in as a function of RF, assuming 60 mW of input power at the fundamental frequency.

III. 380 GHz INTEGRATED MIXER/MULTIPLIER FABRICATION

The integrated circuit includes an anti-parallel pair of planar Schottky diodes (ref. SC1T9-D20 from VDI) for the 380 GHz sub-harmonic mixing part, and an anti-series array of 4 planar Schottky Varactor diodes (ref. SB6T4-R1 from VDI) for the multiplier part. The latter component has originally six Schottky devices. However, one diode at each extremities is removed to produce the configuration shown in Fig. 4, which

reduces the amount of input power required. Both mixing and multiplying diodes components are flip-chip mounted onto a single quartz based microstrip circuit. The quartz substrate is cut into the required "T" shape using a precision dicing saw. This geometry is needed to accommodate the different dimensions of the two Schottky devices and to prevent higher order modes, as described above, from propagating inside the circuit.

Then, the quartz based circuit is mounted inside the lower half of the split-block and connected via beamleads to the three ceramic chip capacitors, as shown in Fig.4. Gold bond wires are then contacted to the circuit using a conductive silver-epoxy glue as a final step of the mounting procedure.



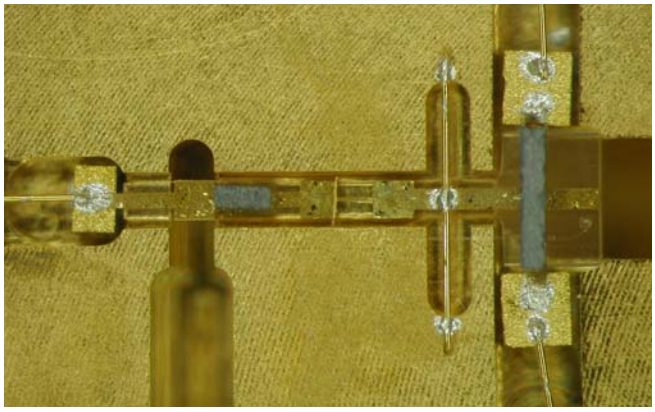


Fig.4. Top: labelled schematic of the integrated design and, bottom, a photograph of the circuit after mounting into the lower half of the split metal block

The assembled 380 GHz block shown in Fig.5 includes two SMA DC bias ports, a K-type IF output connector (right hand side), a WR-10 input flange for the fundamental input signal (not visible, on the left-hand side), and an integrated diagonal RF horn antenna [11] with aperture visible on the front of the block. The IF microstrip-to-K connector transition is designed to present low insertion losses from DC up to 40 GHz.

Fig.5. Photograph of the final integrated mixer/multiplier assembled block.

IV. Test of the integrated 380 GHz receiver

For testing, the 380 GHz integrated mixer/multiplier is driven by a BWO whose output power is controlled by a separate rotary vane attenuator. In order to maximize the matching at the fundamental frequency, an E/H tuner is inserted after variable attenuator. Both DC bias lines to the doubler stage are connected to a stabilized low noise DC power supply. The IF signal is amplified by a low noise amplifier chain, with a noise figure of 1.4 dB, which included a filter with a pass band between 2.5 GHz and 3.5 GHz. The output power of the amplifier chain is measured using an HP 8481D diode power sensor.

Test results presented in Fig.6, show the double side band (DSB) receiver noise temperature, DSB mixer noise temperature and DSB mixer conversion losses as functions of four times the fundamental signal frequency. The best DSB receiver noise temperature obtained is 2330 K at an RF frequency centred at 372 GHz, corresponding to a DSB mixer noise temperature of 1625 K and DSB mixer conversion losses of 8 dB. The measured conversion losses are between 1.2 dB and 2.5 dB above the predicted ones. The 3 dB conversion losses bandwidth extends from a RF centre frequency from 368 GHz to 392 GHz, apart from degradation in performances around 380 GHz, due to a lack of LO power delivered to the mixer stage. This could arise from a drop of power from the BWO at the fundamental frequency as it has been observed by a measurement of the output power of the BWO at this frequency, and/or a resonance in the LO matching circuit at 190 GHz.

Despite the possibility to bias independently each branch of the doubler diodes array, it is noticed that the performances are optimum when both branches are biased with the same voltage, with equal resulting DC currents, giving an indication that the power coupled to the diodes is well distributed between both branches.

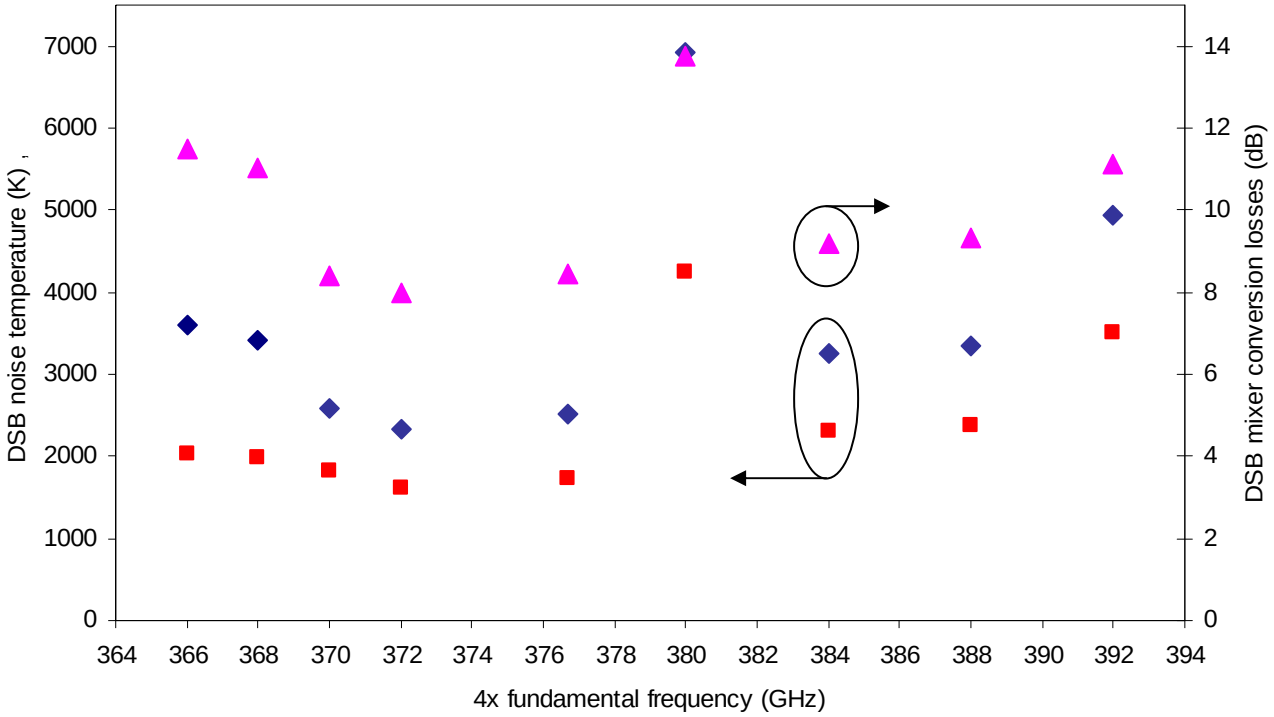


Fig.6. Measured double sideband performance of the 380 GHz integrated mixer/multiplier as functions of the RF frequency. The IF band extends from 2.5 to 3.5 GHz. The bottom red squares show the DSB mixer noise temperature, the middle blue diamonds show the DSB receiver noise temperature and the top pink triangles show the DSB mixer conversion losses.

I. Conclusion

The first operation of an integrated sub-millimetre wave receiver featuring a doubler and a sub-harmonic mixer stage on a single substrate is reported. Over nearly all of the designed RF bandwidth, conversion losses between 8 and 10 dB and DSB noise temperatures between 1625 and 3000 K were measured. These agree relatively well with the simulation. An observed degradation in performance at 380 GHz is attributed to a loss in LO power delivered to the mixer stage. The device demonstrates that it is possible to couple efficiently the output signal of a doubler stage to a sub-harmonic mixer circuit when both are mounted on the same microstrip quartz-based circuit.

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