A Novel THz SIS Mixer with a NbTiN-Ground plane and SIS Micro-Trilayers Directly Grown on a Quartz Substrate

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Abstract— **A new structure and fabrication process for multi-material THz-SIS mixers is proposed. In this design, both the micrometer-sized SIS trilayers (MTLs: micro-trilayers) and the ground plane are deposited directly onto the substrate. This structure is expected to possess a number of unique features, e.g., (1) the quality of the SIS junction is not affected by the physical nature of the ground plane film; (2) the heat can escape directly from the junction into the substrate. The influence of the MTL-structure on the junction quality and circuit characteristics have been investigated. Numerical calculation suggests that the extra rf loss around the junction can be kept small if the offset between the junction and the ground plane is less than 1μm. MTL-SIS mixers have been fabricated using Nb/Al-AlO$_x$(or AlN$_x$)/Nb SIS junctions and NbTiN/Al microstriplines. The leakage current of the SIS junction can be made as small as that of the best all-Nb devices. The MTL-SIS structure will be useful in thedevelopment of future THz SIS mixers.**

I. INTRODUCTION

Heterodyne receivers with superconductor-insulator-superconductor (SIS) quasiparticle mixers offer quantum-noise limited sensitivity at frequencies from 0.1THz to ~1THz[1]. SIS mixer devices usually include an integrated circuit to tune out the large capacitance of the SIS junction(s). It is common to make these transmission lines with superconductorssuch as Nb. One of the critical parameters that characterize the interaction between a superconductor and high frequency electromagnetic radiation is the gap frequency ($f_{\mathrm{gap}}=2\Delta/h$), which is the minimum frequency at which a photon canexcite quasiparticles. Below f_{gap}, a superconducting strip line can be treatedas a lossless metal sheet with nearly zero surface resistance[2]. However, above f_{gap}, the resistivity of a superconductive transmission line increases drastically, and the rf loss severely degrades the sensitivity of the receiver[3]. On the other hand, the SIS junction itself can operate in the quantum regime and offer high sensitivity up to a frequency of $2f_{\mathrm{gap}}$[4], [5]. For example, the f_{gap} of niobium (Nb) is ~0.7 THz, which is the largest among element superconductors. Nb is not only a good material for planar transmission lines below 0.7THz, but has also been regarded as the best material for the electrodes of SIS junctions, in combination with high quality tunnel barriers made of aluminum oxide (AlO$_x$). At 0.7THz $<f<$ 1.4THz, Nb SIS junctions can be used incombinationwith transmission lines made of compound superconductors with f_{gap}larger than Nb (e.g., NbN[6]-[7], NbTiN[8],[9],NbCN[10],[11], Nb$_3$Al[12]) or normal metals with low resistivity (e.g., Al, Au[13], [14]). For example, SIS mixers with Nb/AlO$_x$/Nb (or Nb/AlN/NbTiN) SIS junctions and NbTiN/SiO/Al microstriplines have shown good performance at f~1THz[8], [15]. At $f>$ 1.4THz, where the conversion loss of SIS junctions made of Nb increases sharply, epitaxially grown NbN/AlN/NbN SIS junctions are considered as a promising alternative [6]. In the same way as Nb, NbN can be used for an SIS junction up to $2f_{\mathrm{gap}}\sim$ 2.8THz, but its use for transmission lines is limited to $\leq f_{\mathrm{gap}}$ ~1.4THz. Therefore, at 1.4THz $\leq f \leq$ 2.8THz, the transmission line must be made of normal metals like Al or Au. Examples of material candidates for SIS junctions and transmission lines are illustrated in Fig. 1.

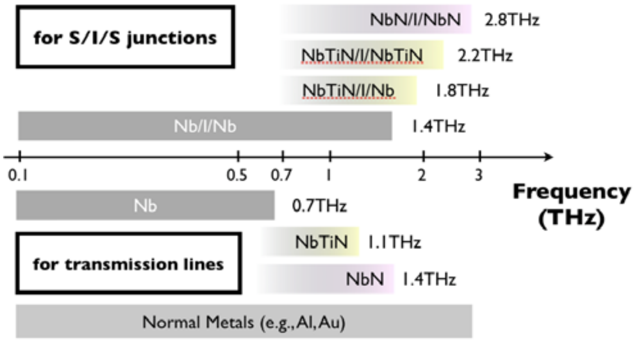

Fig. 1 Approximate frequency upper limits of various superconductors as materials for electrodes of SIS junctions or transmission lines.

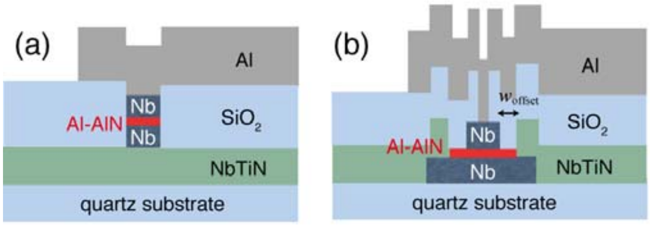

Fig. 2 Cross sectional diagrams of SIS mixers with (a) a conventional "stacked up" structure and (b) a micro-trilayer structure.

Thus, SIS mixers at super-terahertz frequencies are often multi-material, in sense that the electrodes of the SIS junction, and the transmission line, are made of different materials. Usually, these devices are fabricated by stacking an S/I/S trilayer on top of the ground plane of the transmission line, as shown in Fig. 2(a). In such a configuration, the requirements for the properties of the ground plane film tend to be quite tight, if both good quality SIS junctions and a low-loss transmission line are to be realized:

- Thin films of compound superconductors such as NbTiN often possess strong stress, which can damage the tunnel barrier of the SIS junction that lies on top, when the stress is released during the fabrication process [16]-[17].
- The films of compound superconductors can have rough surfaces[18]. This can affect the growth of films grown on top, for example the bottom electrode of the SIS junction and also the tunnel barrier, causing degradation in the nonlinearity of the current-voltage ($I(V)$) characteristics[19].
- The epitaxial growth of the superconducting electrodes of the SIS junction can have several advantages, such as an increased f_{gap} and less defects in the tunnel barrier[7],[15]. In order to grow a film epitaxially, the underlying layer must also be crystalline with a matched lattice constant.

Aside from these difficulties, there is also a potential problem of heat trapping in an SIS junction placed on a superconductor with a larger f_{gap} than its electrodes[20]-[21]. Nevertheless, multi-material SIS mixers with "stacked-up" structures have demonstrated state-of-the-art performance above 1THz.

In this study, we propose an alternative structure and fabrication process for multi-material SIS mixers. Because this fabrication process includes a stage where islands of S/I/S trilayers with diameters as small as a few micrometers are formed, we refer to this new process/structure as the "micro-trilayer" (MTL). In the MTL design, both the μm-sized SIS trilayers AND the ground plane are deposited directly onto the substrate, or, possibly with a buffer layer in between. A cross sectional diagram of the MTL SIS junction is presented in Fig. 2(b). We expect this structure to possess a number of unique features:

- The quality of the SIS junction is not affected by the physical nature (e.g., stress, roughness or lattice constant) of the ground plane film.
- The Joule heat produced in the SIS junction can escape directly from the bottom electrode into the substrate.

On the other hand, there are also possible drawbacks:

- There is an area around the SIS junction where the base electrode of is not covered by the ground plane. We call this the "*offset*" region (see Fig. 2(b)). For rf currents at THz frequencies, this region behaves like a normal conductor and therefore adds to input losses of the mixer.
- The structure around the SIS junction becomes three dimensional and complex, which could add unpredicted reactance to the circuit.

We have studied the properties of the MTL structure in terms of the quality of the SIS junctions and the characteristics of the tuning circuit, by means of numerical simulation and experiment.

II. SIMULATION

The effect of the additional resistance at the offsetarea around the SIS junction was studied by numerical simulation using a commercial software package*Microwave Office*®. We assumed a configuration in which two Nb/Al-AlO$_x$/Nb SIS junctions are embedded in a microstrip line tuner, which consists of a NbTiN ground plane and an Al top wire with SiO$_2$as an insulating layer. The offset structure was included by replacing part of the NbTiN ground plane around the junction with Nb. A schematic of the geometry is presented in Fig. 3, in which the height of the Nb islands is much exaggerated.The legends of Fig. 4 summarize the material and geometrical parameters used for the simulation.

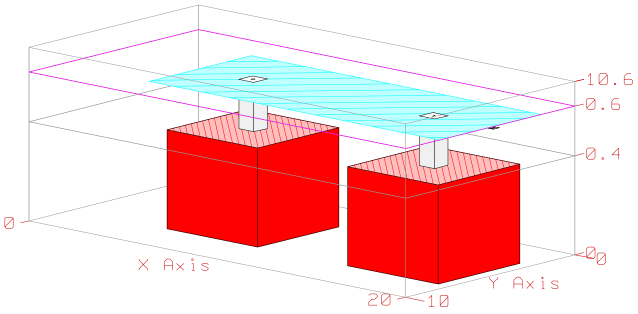

Fig. 3 Configuration of the electromagnetic-model of the twin SIS tuning circuit with Nb-MTL junctions. The blue layer represents the Al top wire. The two red flat islands are the Nb micro-trilayers surrounded by the NbTiN ground plane. The x, y and z axes are in units of μm.

According to the results, the offsetarea may introduce noticeable rf-loss. Fig. 4 presents the combined effect of rf-loss, which includes both the tuning circuit and the offset area. This graph illustrates the influence of the offsetwidth (w_{offset}) and the $R_{\mathrm{N}}A$ product of the SIS junctions (normal resistance multiplied by the area). The important result is that by decreasing w_{offset} from 2 μm to 0.6 μm we may save up to 1.2 dB of coupling loss for the 0.8-μm SIS junctions. Trying to minimize the three following parameters: $w_{\mathrm{offset}} = 2 \rightarrow 0.6$ μm, $R_{\mathrm{N}}A=32 \rightarrow 21$ Ω μm^2, $d_{\mathrm{SIS}} = 1 \rightarrow 0.8$ μm, one can save up to 2.7 dB of the mixer gain. Note that the solid curve at the top presents the imaginary situation of epitaxial NbN junctions instead of Nb ones. Note also that the offset of 0.2 μm has a negligible effect on rf-loss.

III. FABRICATION

SIS mixers with Nb/Al-AlO$_x$ (or AlN) /Nb SIS junctions and NbTiN/SiO$_2$/Al tuning circuits have been fabricated using the MTL technique. The geometry of the tuning circuit is the same as the current design for the ALMA (Atacama Large Millimeter and Submillimeter Array) band 10 SIS mixer[9], except for the MTL structure around the junctions. No modification/optimization of the circuit design has been done, for the primary purpose of the experiment was to quickly demonstrate that the MTL process can reliably produce good quality SIS junctions in combination with a NbTiN ground plane.

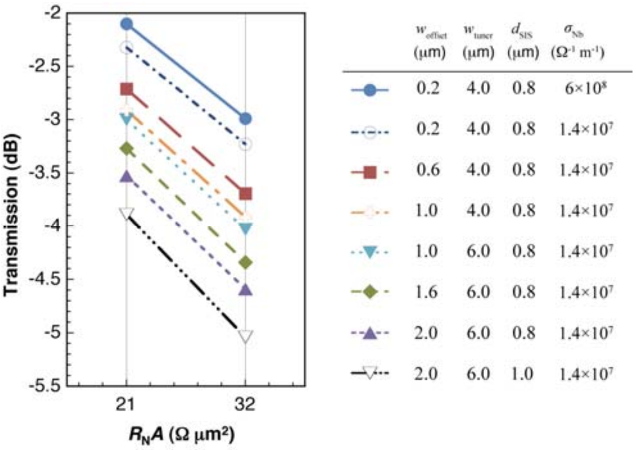

Fig. 4 Loss in the resonant tuning circuit with twin MTL SIS junctions shown in Fig. 3. w_{offset}, w_{tuner}, d_{SIS}, $\sigma_{\mathrm{Nb}}$are the width of the offset, the width of the Al top wire, the diameter of the SIS junction and the conductivity of Nb, respectively.

Fabrication of the MTL structure requires a horizontal alignment accuracy on the order of 100nm, which is difficult by means of conventional contact mask aligners. Therefore, we used an i-line stepper (Canon FPA-3000 i5+) with an alignment accuracy better than 40nm. In addition, we adopted an ICP-etching machine with dc biasing for good anisotropy. This combination enabled us to fabricate the MTL structure with good reproducibility.

The S/I/S trilayer consists of a 200nm-thick Nb base-electrode layer, a 10nm-thick Al layer, with its surface either oxidized or nitridized to form a tunnel barrier, and a 100nm-thick Nb top-electrode layer. To form the AlO$_x$ barrier, the Al film was exposed to an oxygen atmosphere, while the AlN barrier was created by nitridizingthe surface of the Al film in a capacitively coupled nitrogen plasma. The ground plane was made of 230-nm thick NbTiN, which was dc-sputtered in a plasma of Ar+12%N$_2$. The typical resistivity of the NbTiN films at room temperature was $\rho_{300\mathrm{K}}$ = 110μΩ cm and the transition temperature was T_{c} = 14K.

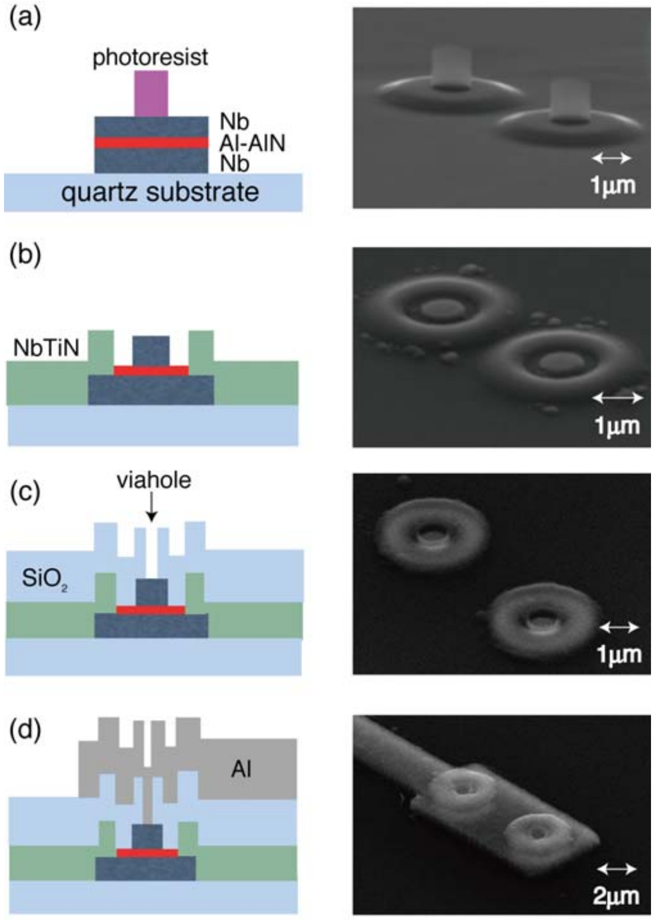

Fig. 5 Cross sectional diagrams (left) and SEM micrographs (right) of the SIS junctions at various stages of the fabrication process.

Cross sectional diagrams and SEM micrographs are presented in Fig. 5 to summarize the fabrication process. The process began by depositing the trilayer through a liftoff mask. The diameters of these circular trilayers were remarkably small; only 3-5µm. After lifting off the photoresist, a columnar photoresist with a diameter of 0.8-2.0µm was patterned in the center of the trilayer, and the junction was isolated by ICP etching. Next, another columnar liftoff mask with a diameter larger than the junction by ~1µm was patterned so that it covers the top-Nb electrode, and then the NbTiN ground plane was deposited. When the photoresist is removed, the top electrode appears again with the offsetaround it. Note that it is possible to anodize the rims of the SIS junctions at this point—though this will also anodize the surface of the top electrode, the oxide can be removed afterwards when the via-hole is etched. Next, a layer of SiO_2 was deposited all over the wafer. This layer has a thickness of 300nm and serves as the insulator of the microstrip line. Finally, a via-hole with a diameter smaller than the junction (0.6-1.0µm) was etched and the Al top-wire with a thickness of 540nm was deposited. The resistivity of the Al film at 4K was 0.21µΩ cm, which corresponds to an electron mean free path of 390nm, limited by the thickness of the film[22].

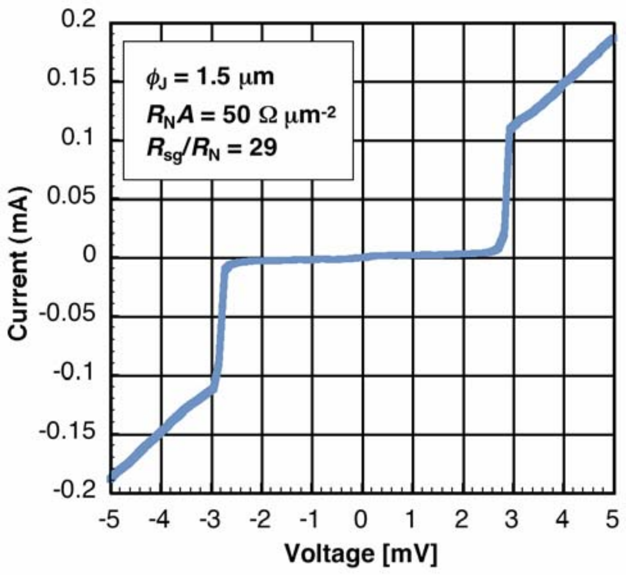

Fig. 6 DC I(V) curve of a Nb/Al-AlN/Nb SIS junction combined with a NbTiN ground plane using the micro trilayer technique.

The process described above is merely one example of the several possible sequences for creating the MTL structure. For example, one could begin the process by sputtering the ground plane instead of the trilayer, though this will result in the Nb base electrode overlapping *on top of* the ground plane, and not beneath. One advantage of the abovementioned sequence was that the surface of the NbTiN film is never exposed to a plasma after it is deposited. In contrast, in the conventional process where the trilayer is deposited on top of the NbTiN ground plane, the surface of the NbTiN ground plane will be exposed to the plasma when the trilayer around the junction is removed, which can make the surface of the NbTiN film considerably rough.

IV. DC CHARACTERISTICS

The dc $I(V)$ characteristics of the abovementioned SIS mixers were measured at 4.2K by a four-point method. An example of an $I(V)$ curve of a Nb/Al-AlN/Nb SIS junction is presented in Fig. 6. This junction has an $R_N A$ product of 50 Ω µm^2, which corresponds to a critical current density of J_c = 4kA cm^{-2}. The ratio of the R_N to the sub-gap resistance measured at 2mV (R_{sg}) was R_{sg}/R_N ~30. This is approaching the theoretical limit of the sub-gap current of Nb at 4.2K ($R_{sg}/R_N \leq 40$) [23], indicating that the AlN barrier was formed with no problem, even though the trilayer was extremely small. Similarly, we have also obtained AlO_x barrier SIS junctions with good quality using the MTL process (e.g., $R_N A$=16 Ω µm^2, R_{sg}/R_N = 15).

While the MTL structure does not seem to affect the sub-gap current, we found that the gap voltage of the $I(V)$ curve decreases when the diameter of the *Nb base electrode* was smaller than 10µm, as shown in Fig. 7. This could be because the quality of the µm-sized Nb film is affected by contamination from the sidewalls of the

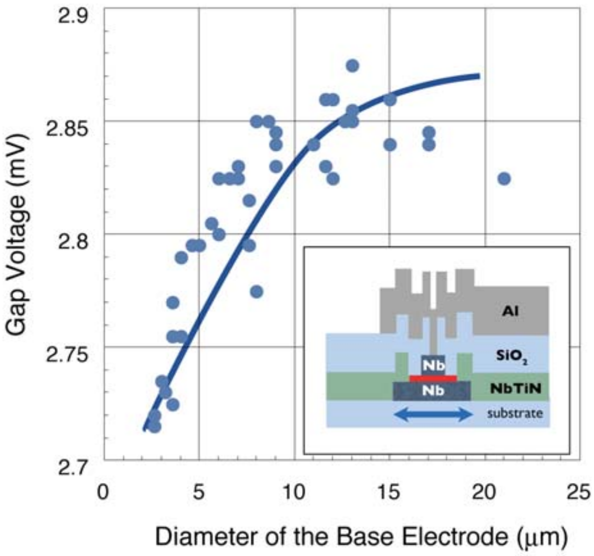

Fig. 7 The decrease in gap voltage in accordance to the diameter of the Nb base electrode (shown by the arrow in the inset). Each point represents a different SIS junction on the same wafer. The solid curve is shown as a guide-to-the-eye.

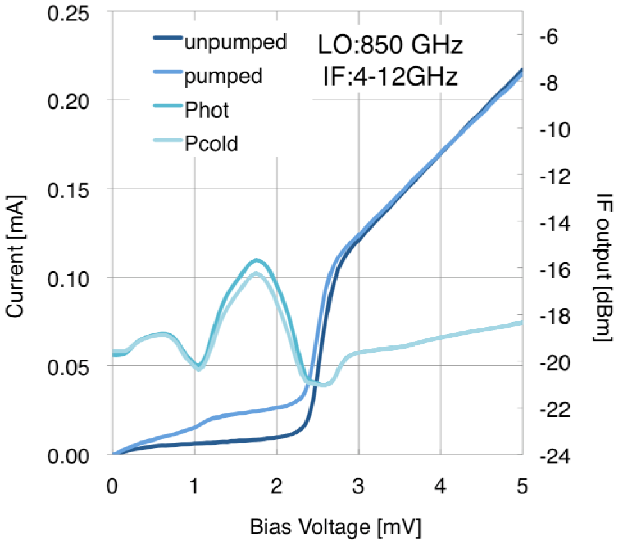

Fig. 8 RF characteristics of a MTL SIS junction at 850 GHz.

photoresist during the deposition of Nb. Another mechanism that could cause a decrease in the gap voltage is Joule heating around the junction. However, we do not think this is the case, because no back-bending was observed in the $I(V)$ curves with suppressed gap voltages.

V. RF MEASUREMENT

We have installed one of the SIS mixer devices in a waveguide-type receiver to measure the noise temperature by the standard Y-factor method. So far we have only measured one chip, and furthermore, both the mixer chip and the measurement setup were not optimum, so this is merely a preliminary result. The $I(V)$ curve of the SIS mixer in the receiver with/without LO input is presented in Fig. 8. The reduced gap voltage and the large sub-gap current is a result of the temperature of the mixer being considerably higher than 4K. The local oscillator frequency was $f_{\rm LO}$ = 850GHz. The integrated IF output from 4 to 12 GHz is also plotted. The calculated noise temperature was 1100K at this frequency, and was typically 1500-2000K throughout $f_{\rm LO}$ = 820-920GHz. This noise temperature is considerably higher compared to the noise temperature measured for SIS mixers with the same material but with the conventional "stacked up" structure (Uzawa*et al.*, this conference).

VI. DISCUSSION AND FUTURE POSSIBILITIES

We have seen that introducing the MTL structure results in a trade-off between the improvement of the junction quality and the increase of rf-loss in the tuning circuit. As predicted from our simulation, a good way to reduce the rf-loss is to reduce the$R_{\rm N}A$ ofthe SIS junction. AlN barrier SIS junctions are useful for this purpose, for$R_{\rm N}A<10\ \Omega\ \mu m^2$ can be achived with excellent non-linearity[7],[24]-[26].

The MTL structure should be especially useful in pushing the frequency limit of SIS junctions to the super-THz range, where HEB mixers are currently the choice when sensitivity is top priority. For example, if an epitaxial NbN/AlN/NbN SIS junction is used in combination with a microstrip line made of superconductors with higher T_c (e.g., MgB_2)or a normal metal with low resistivity (e.g., Al or Au),the theoretical cutoff frequency can beas high as 2.5THz. However, NbN does not usually grow epitaxially on these materials, so it would be difficult to fabricate such a device using the conventional "stacked up" structure. If the micro-trilayer structure is adopted, the NbN/AlN/NbN trilayer and the microstrip line can be grown independently on a substrate suitable for the epitaxial growth of NbN, such as MgO. Such SIS mixers have the possibility of achieving good sensitivity at super-terahertz frequencies.

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