Design of Superconducting Terahertz Digicam

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Abstract— **Imaging array design for 650 GHz SIS photon detector array, which we call superconducting terahertz digital camera, is discussed. Focal plane optics and cryogenic readout electronics are two major topics for the array developments. Lens arrays are discussed to make high optical efficiency and compact focal plane assembly. Cryogenic readout electronics were designed and fabricated based on GaAs-JFET technologies. These designs are similar to CMOS digital camera, but operate at cryogenic temperature, and we can make use all the advantage of the digital camera technologies for the superconducting terahertz digicam.**

I. INTRODUCTION

Development of large format imaging array in terahertz frequencies are crucial for future space terahertz community for imaging large field of view with high dynamic range. Variety of imaging array techniques are employed in this field: transition edge sensor bolometers, kinetic inductance detectors, hot/cold electron bolometers and superconducting tunnel junction detectors [1].

We have been working on superconducting direct detectors with niobium tunnel junctions, the SIS photon detectors. The detectors have high dynamic range and fast response, and operate at higher temperature than bolometric detectors. But, there are some issues before we can apply the detector technology to future instrumentations. One is how to realize large format array with efficient focal plane optics and cryogenic readout electronics, others are how to improve sensitivity and wavelength coverage for low background space-born instrumentations.

In this paper we describe the design of focal plane optics for large format imaging array and integrated readout electronics for the superconductive imaging submillimeter-wave camera for 650 GHz observation.

II. IMAGING ARRAY DESIGN

Our imaging array is based on submillimeter-wave SIS photon detectors which are a kind of tunnel junction detectors with their photo response due to the photon assisted tunnelling process [2]. Because the tunnel junction detectors are relatively high impedance detectors they can be readout using semiconductor readout circuits. Our plan is to implement two imaging array technologies of CMOS digital camera to our superconducting imaging arrays; lens array and semiconductor integrated circuits. Schematic diagram of the imaging array is shown in figure 1, which is similar to cryogenic infrared imaging array with CMOS integrating amplifier and multiplexer bonded to the detector array. Two major differences to the infrared arrays are that the input radiation is coupled to antenna behind each lens, and that the readout circuits operate at less than 1 K. Key parameters of the camera are listed in table I, which will be addressed into detail in the following sections; the detector, focal plane optics and readout electronics.
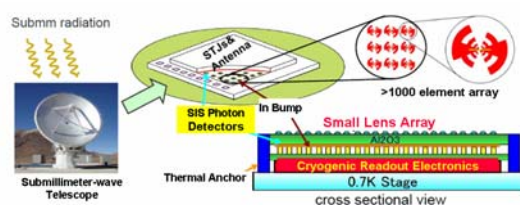

Fig.1. Schematic diagram of the superconducting terahertz digicam [3].

TABLE VII
KEY PARAMETERS OF THE DIGICAM

Detectors	SIS photon detectors at 650 GHz
Focal Plane Optics	Hexagonal lens array with 1.0 Fλ spacing 1027 pixels φ37 mm FPA at F2.0 focus
Readout Electronics	GaAs-JFET CTIA at < 1.0 K Multiplexed Readout
	Low noise < 1 µV/√Hz @ 1H
	Low power dissipation < 10 µW/ch

A. SIS Photon Detectors

The SIS photon detectors are antenna coupled superconducting tunnel junction direct detectors based on photon assisted tunnelling process. Their operational frequency is below the superconducting energy gap, which is same as the SIS mixer. Since the SIS photon detectors are quantum detectors, their response is much faster and their dynamic range is higher that bolometric detectors. The detector performance is limited by the leakage current of the tunnel junctions. Sensitivity and noise of SIS photon detector is expressed by the following equations [4]:

$$S = \eta \cdot \frac{e}{h\nu} \quad [\text{A/W}]$$

$$N = \sqrt{2eI_0} \quad [\text{A}/\sqrt{\text{Hz}}]$$

$$NEP = N/S = \frac{h\nu}{\eta} \cdot \sqrt{\frac{2I_0}{e}} \quad [\text{W}/\sqrt{\text{Hz}}]$$

where η is quantum efficiency, ν is frequency and I_0 is the leakage current. Current performance of submillimeter-wave SIS photon detector is limited by leakage current of about 100 pA and quantum efficiency of about 20%, which result in NEP of about 10^{-16} W/Hz$^{0.5}$ at 650GHz. Our goal is realize leakage current of less than 10 fA and NEP of less than 10^{-19} W/Hz$^{0.5}$ for future space-born instrumentations.

Figure 2 shows the 36-element array of SIS photon detectors fabricated in RIKEN that operates at 650 GHz with 10% bandwidth [5]. One detector element consists of log-periodic antenna and a series of 6-element distributed parallel junctions, totally 12 tunnel junctions on one detector element which forms matching circuits for 650 GHz input radiation.
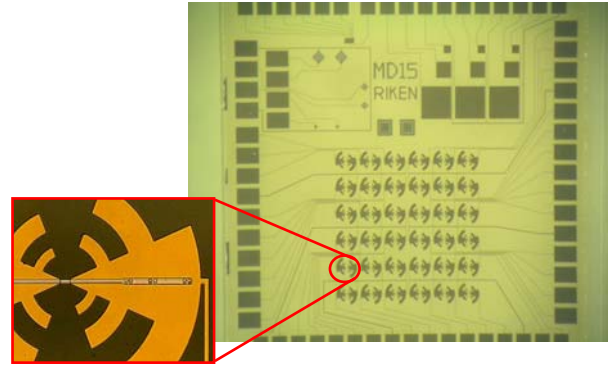

Fig.2. 36-element 650 GHz SIS photon detectors on 5mm x 5mm sapphire substrate [5].

Table II summarizes the performance of SIS photon detectors [6]. It is characterized as large voltage response detector with short time constant and large dynamic range. When the detector temperature is higher than 0.7 K, their performance is limited by the thermally excited quasi-particle current, but have good performance even at 4.2 K compared to bolometers operating at the same temperature [2]. If their leakage current further decreased down to 0.5 K following the BCS theory, leakage current of 10 fA would give NEP of 10^{-19} W/Hz$^{0.5}$.

TABLE VIII
PERFORMANCE OF SIS PHOTON DETECTORS AT 650 GHZ

NEP	10^{-16} W/Hz$^{0.5}$
Temperature	< 0.7 K
Voltage Response	10^9
Time Constant	<< 10^{-3} second
Dynamic Range	> 10^7
Limit of NEP	Leakage current

Before implementing multiplexed readout circuit for SIS photon detectors, we have confirmed operation of a detector with an integrating amplifier [7]. For this experiment we used conventional operational amplifier at room temperature to make resistive or capacitive trans-impedance amplifier (TIA or CTIA). Figure 3 shows the I-V characteristics measured with TIA and output signal from CTIA under background illumination from 300 K and 77 K blackbody, respectively. From the experiment we have found that stable operation of SIS photon detector is realized when feedback amplifier gain is more than 2000.
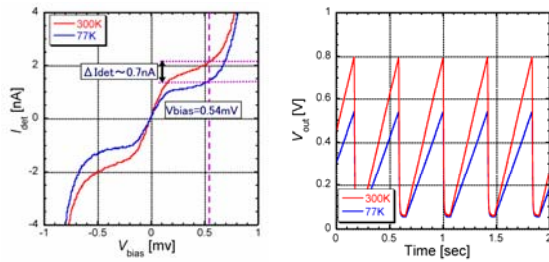
Fig. 3. (left) I-V characteristics of an SIS photon detector under radiation input from 300 K and 77 K blackbody source. (right) Signal output from integrating amplifier under the same radiation conditions [7].

B. Focal Plane Optics Design

High efficiency and compact focal plane optics is important for the large format array design. First we discuss briefly on the figure of merit of focal plane optics and then show possible design to install a large format array of SIS photon detectors in a compact cryostat.

There are two obvious approaches for focal plane optics design, one is optical design approach and another is microwave approach. Thin film absorber is commonly used for bolometric detectors and often used in a small cavity or with multi-mode waveguides connected to a conical horn or a Winston cone. This could be a combination of microwave horn technologies and optical thin film technologies, which has been used extensively for semiconductor bolometers. Filled array with thin film absorber is another approach often used for TES bolometers such as SCUBA-2 [8] and ones made in NASA GSFC [9]. In this design, pixel spacing of half beam width or Nyquist sampling is adopted. The filled array is like CCD, for which incoming radiation from any angle of incidence is absorbed. Other approaches use thin film antennas with lens or without lens. In this approach, distributed antenna array [10] or quasi-optical technology [11] is adopted, where Gaussian beam mode analysis is often used to achieve high beam-mode coupling to telescope optics.

To compare the different focal plane optics design, the following figures of merits are discussed: 1) focal plane coverage, 2) number of pixels, 3) beam efficiency, 4) size of focal plane. Table III lists some of the parameters to show the characteristics of different focal plane optics design.

The focal plane coverage means the efficiency of focal plane usage or the ratio of detected radiation and total radiation from telescope aperture within field of view of the array. Horn array results in small coverage because the horn aperture size limits the spacing between pixels. Other planar structure can cover most of the focal plane area in principle. The number of

pixels is the required number of detectors to cover the focal plane normalized by focal plane area divided by half power beam area. For the horn array number of pixels is limited by the focal plane coverage. For filled array, Nyquist sampling is preferred and four times larger number of pixels is required than the full sampling arrays. Beam efficiency means the coupling efficiency of one detector element to telescope optics. Horn arrays have high beam efficiency, but filled array have low efficiency due to large side lobe which should be terminated by cold stop inside a cryostat. Size of arrays is also dependent on re-imaging optics. Horn array tend to have longer focal length and the array size becomes larger. On the other hand, filled arrays prefer small sizes for better optical coupling and smaller absorber volume. The distributed antenna and lens arrays with full beam sampling design could achieve high focal plane coverage with smaller number of pixels compared to the filled array design.

TABLE IX
COMPARISON OF FOCAL PLANE OPTICS DESIGN

	Horn array	Filled array	Antenna array	Lens array
Focal plane coverage	20-30%	~100 %	80-100%	80-100%
Number of pixels	0.2-0.3	4	0.8-1	0.8-1
Beam efficiency	high	low	medium	medium
Size of array	large	small	medium	medium

From the above consideration, distributed antenna array or lens array seems to be a good compromise for optical performance and number of pixels required. In this paper we propose to use lens array for the imaging array. The lens array is designed using Al_2O_3 ceramic lens with low absorption coefficient and large index of refraction. We are going to use planar antennas at focus of each lens. In front of the lens, incoming beams are overlapped at -3dB at lens edges and each lenses focus the beams onto planar antennas at the backside of the lens array. Figure 4 shows the ZEMAX calculation of beams inside the 0.4-K cryostat for ASTE. Fore-optics and the cryostat is the same as in reference [4]. Aberration within the 7 arcmin field-of-view is within the Airy radius. The lens diameter and thickness are both 1 mm. Lenses are placed in a hexagonal pattern to make the distance between beams as small as possible. With this configuration the array would cover the

6.8 arcmin field-of-view with 1027 detectors, which correspond to the physical size of 37 mm in diameter at F2 focal plane of 10-m diameter telescope.
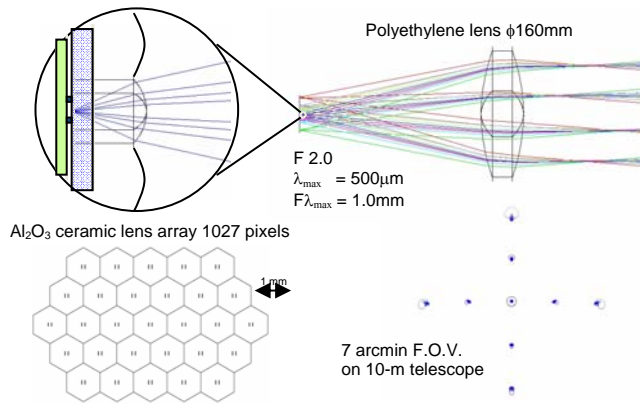
Fig.4. (top) Focal plane optics design with lens array at focal plane. SIS photon detectors are at the backside of sapphire substrate with planar antenna such as double-slot antennas. (bottom) Front view of the hexagonal lens array and spot diagram calculation within a field of view of 7 arcminues on 10-m diameter telescope.

III. CRYOGENIC READOUT ELECTRONICS

The cryogenic readout electronics is based on junction field effect transistor of gallium arsenide semiconductors (GaAs-JFETs). First we explain the property of SONY GaAs-JFETs and then describe the design and recent measurement results of cryogenic readout electronics both analogue and digital circuits for the superconducting terahertz digicam.

A. GaAs-JFETs

GaAs-JFETs have good I-V and noise characteristics at cryogenic temperature [12]. We have been working on SONY GaAs-JFETs at cryogenic temperature below 4.2 K that show identical performance even down to 0.3 K [13]. Figure 5 shows I-V characteristics and noise spectrum of a depletion-type GaAs-JFET.
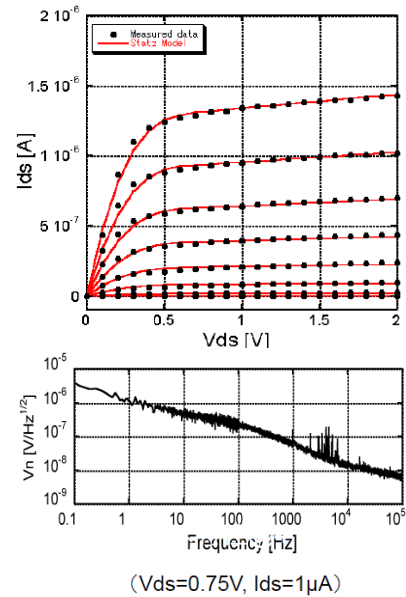
Fig.5. I-V characteristics and noise performance of SONY GaAs-JFET (W/L=5/50um) at 4.2K. A Statz model well fits to the I-V characteristics [7].

The I-V curve show a good fit to a standard Statz model, which makes the design of circuits very flexible and low power dissipation circuits can be designed relatively easily. They show no hysteretic or kink behavior like silicon MOSFETs. Unlike GaAs-MESFETs, the gate leakage current of p-n junction of GaAs-JFET is extremely low and also have low noise performance [14]. The SONY GaAs-JFETs show gate leakage current of an order of 10^{-19} A, and low voltage noise of less than 1 $\mu V/Hz^{0.5}$ at 1Hz were measured. We can design integrated circuits both with depletion and enhancement type JFETs on the same wafer, so we can control DC offset of amplifier and normal state of switching circuits. The flexible circuit design also serves to lower the power dissipation.

B. Design of CTIA amplifiers

The analogue electronics for the imaging array is based on ac-coupled capacitive trans-impedance amplifier (AC-CTIA). We decided to use AC-CTIA because of the following reasons: 1) SIS photon detectors are low current and high impedance device, 2) SIS photon detectors require low and constant bias voltage of about 1 mV, 3) output signal should be multiplexed. Figure 6 shows the schematic diagram of the readout electronics. It is composed of AC-CTIAs, sample-and-holds, a multiplexer and shift registers.
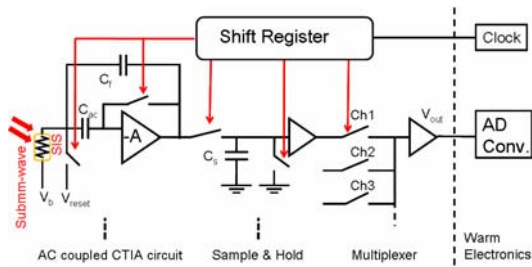
Fig.6. Schematic diagram of the cryogenic readout electronics [3].

Bias voltage of SIS photon detector is kept constant at V_b by the feedback amplifier and quasi-particle current is integrated on feedback capacitor (C_f). Because of relatively large offset voltage of GaAs-JFET and small voltage bias to the detector of about 1 mV, the amplifier is ac-coupled (C_{ac}) to cancel the offset voltage. The AC-CTIA amplifier is followed by a sample-and-hold circuit and a multiplexer that is addressed by a shift register. Full explanation of the analogue integrated circuits are given by Nagata et al. [15].

We have designed high gain amplifier circuits and fabrication of test circuits is made using a standard GaAs-JFET process by SONY. Figure 7 shows one of the test circuits; a cascode active-load amplifier with differential input and output source follower. The measured gain of the amplifier was 170, power dissipation was 4 μW, input referred noise 8 $\mu V_{rms}/Hz^{0.5}$ at 1Hz, and output voltage swing 0.8 V_{p-p}. Since input stage FETs are enhancement type in this circuit, the noise tend to be larger than the depletion type FETs.
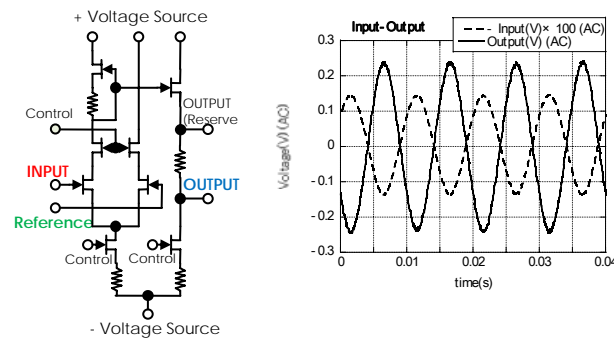

Fig.7. Demonstration of GaAs-JFET single stage amplifier with gain of about 200.

Circuit design of one of the ac-coupled CTIA amplifiers is shown in figure 8. FETA is an enhancement type JFETs and the other FETs are depletion types. The gate sizes of these FETs are W(μm)/L(μm)=5/5, 5/10, 5/50 5/100 for both FETA and B, FETC, FETD, and FETE. CTIAs with other combinations of the GaAs-JFETs are also designed and fabricated. The resistance of Ra, Rb, Rc, and Rd are 2 MΩ, 1 MΩ, 200 kΩ, and 300 kΩ, respectively. Capacitance for C_{ac}

and C_f are 20 pF and 10 pF. A resistor, R, and capacitor, C, series placed in parallel with FETD is a phase compensation circuit. The resistance R is 30 kΩ, and the capacitance C is selectable from 2 pF to 20 pF because we have only upper limit values of stray capacitances for the GaAs-JFETs (gate-drain, drain-source, and gate source capacitance).
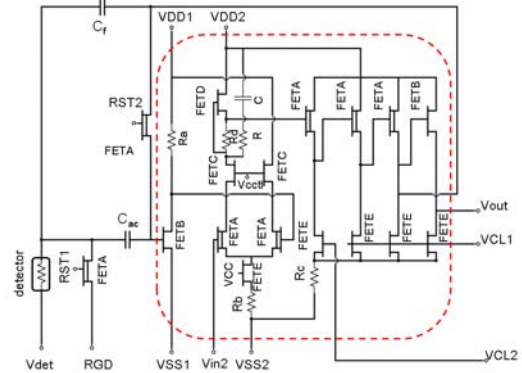

Fig.8. Circuit diagram of AC-CTIA circuits. The area covered by the dashed line is high gain amplifier with gain of more than 2000, that is composed of two stage amplifiers with output level shift source followers. FETAs are enhancement-type and others are depletion-type [15].

PSPICE simulations have shown that open loop gain is more than 2000, the gain bandwidth product of the amplifier is around 250 kHz, voltage swing is 0.5 V, and power consumption is 1.4 μW.

C. Design of Digital Circuits

To decrease the number of readout cables, we designed multiplexer circuit made of sample-and-hold and a multiplexer that are addressed by shift registers operating at the same detector temperature. GaAs-JFETs have good switching performance at low current region, which is advantageous for various switching elements in readout electronics. Accompanied with low gate capacitance of GaAs-JFETs, we can operate GaAs-JFET circuit much faster than silicon MOSFET circuits.

The digital circuit is based on direct-coupled FET logic (DCFL). Since we can use depletion and enhancement type FETs on the same wafers, we used depletion-type FETs (DFET) as current sources and enhancement-type (EFET) as switches to make various logic circuits with low power dissipation. We designed with the DCFL logic level of 0 V (low) and 1 V (high) and source current of 0.12 μA. Figure 9 shows the switching characteristics of the NAND and NOR gates. From the figure, we estimated the voltage margin for our DCFL circuits are more than 0.3 V. This voltage margin is large enough

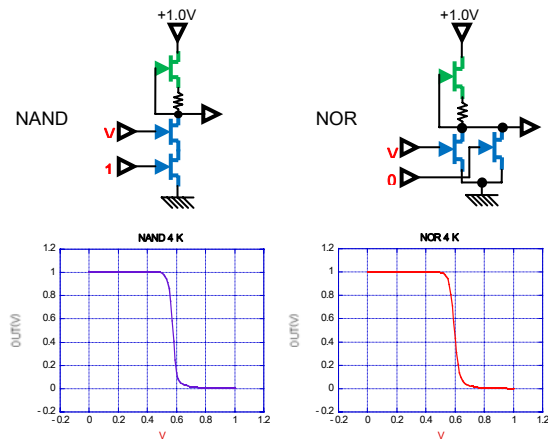compared to the variation in threshold voltage of GaAs-JFETs.

Fig.9. (top) NAND and NOR gates of GaAs-JFET DCFL circuits. DFET as current source and two EFETs for switch for both NAND and NOR gates. (bottom) Input and output voltages of NAND and NOR gates at 4 K. Voltage margin for logic gates are larger than 0.3 V [3].

Figure 10 shows a circuit of a master-slave type flip-flop using NAND gates. Combination of NAND gates is advantageous for low power operation of the circuit. Using 4 flip-flop circuits, we have designed a 4-channel shift register, which can be used to address 4 detector pixels in series.

We have confirmed basic operation of analogue and digital circuits and designed all the cryogenic readout components using n-type GaAs-JFETs only. Based on these experiments and simulations, we now have designed and fabricated 4-channel AC-CTIA amplifiers, 8 channel sample-and-hold circuits and 2 sets of 4 channel shift registers on each chips for evaluation. We are going to measure operation of shift registers, measure their speed and combine with sample-and-hold and multiplexers to make a readout circuits for the imaging array.
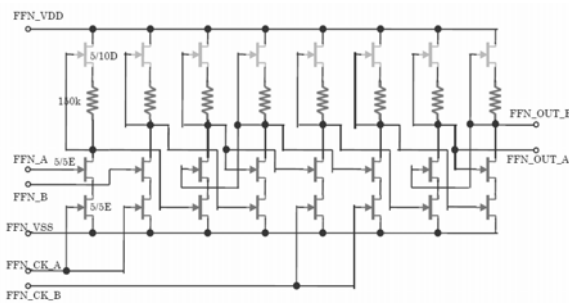

Fig.10. Circuit diagram for a master-slave type flip-flop circuit with NAND gates. Series connection of this flip-flop circuit is used for a shift register. [3]

Although details of clock timing and addressing scheme are not decided yet, we can use similar schemes to CMOS camera or infrared imaging arrays as shown in figure 11, where much larger arrays have been operational and we can use all the developed technologies of the readout electronics.
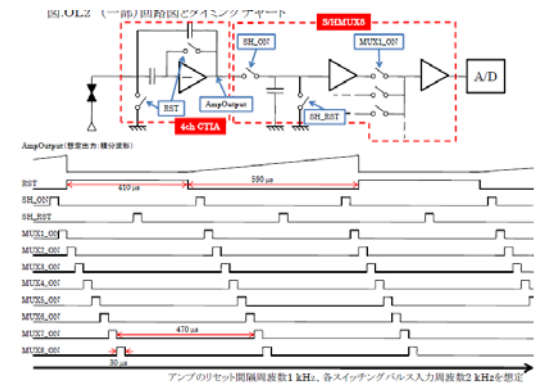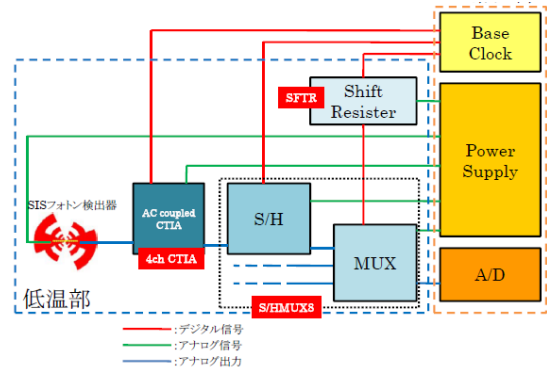

Fig.11. (top) Block diagram of readout electronics of the imaging array. This readout scheme is much like CMOS optical imager except that all analogue and digital electronics operate at cryogenic temperature at less than 1 K. Interface to the room temperature electronics are clock, power supply and a signal line to an A/D converter. (bottom) Timing diagram for 8 channel readout circuit.
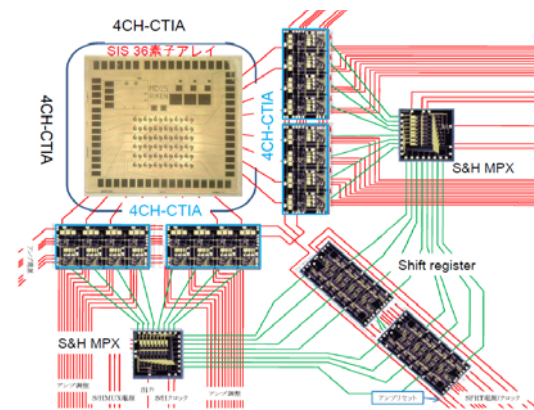
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Fig.12. Configuration of SIS photon detectors and readout electronics when all the test circuits are combined together. Size of the each test chips are either 1.9 mm square or 1.9 mm by 3.8 mm, with total size of less than 20 mm square [15].

Figure 12 shows possible configuration of hybrid readout circuit when all test chips are connected together to make 16-channel cryogenic readout electronics. We still have large number of power

supply lines for tuning each amplifier, but most lines can be in common

CONCLUSIONS

In this paper we discussed two major topics to realize large format arrays of submillimeter-wave SIS photon detectors; focal plane optics and cryogenic readout electronics.

Focal plane optics is important to define the size of the system (number of pixel, pixel separation, cryogenic optics and beam quality), so trade-off between different technologies is important. Compact lens array is discussed in this paper to make efficient focal plane sampling with smaller number of detectors, which is sensible when number of detector and field of view are limited.

Our readout electronics is based on integrating amplifiers with semiconductor device that is identical to infrared imaging arrays, and implementation of readout circuits are straight forward up to 1-k pixel arrays. For larger format arrays and for space-born applications, further development to decrease power consumption of readout electronics or low thermal conductivity interconnect between detector and readout electronics becomes important. When pair-breaking detector in far-infrared region is demonstrated, application fields of superconducting direct detectors will grow including far-infrared space-born instrumentations and various application fields of terahertz technologies.

ACKNOWLEDGMENT

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