Cryogenic Phase Locking Loop System for Flux-Flow Oscillator

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Abstract— Recently a cryogenic phase detector (CPD) based on a superconductor-insulator-superconductor junction has been proposed and preliminary tested. The CPD is initially intended for phase locking of a Flux-Flow Oscillator (FFO) in a Superconducting Integrated Receiver (SIR). A model to describe coupling between the CPD and the FFO has been developed and experimentally verified. We present a design of the Cryogenic Phase Locking Loop (CPLL) system implemented for the SIR and discuss the results of the CPLL experimental tests. The effective bandwidth of the CPLL system exceeds 25 MHz at the reference oscillator frequency of 400 MHz. The CPLL bandwidth considerably surpasses that of the room-temperature PLL system, for which it is limited to 12 MHz by inevitable delays in the long cables and semiconductor devices. The novel CPLL system can phase-lock more than 50% of the emitted by FFO power even if the free-running FFO linewidth is about 10 MHz. This fraction of phase-locked power is twice as much as the result of the conventional room-temperature PLL. Such an improvement allows to reduce the FFO phase noise and extend the SIR operation range.

I. Introduction

A Cryogenic Phase Locking Loop system (CPLL) described in this report is primarily designed for phase stabilization of a Local Oscillator (LO) of a Superconducting Integrated Receiver (SIR) [1], [2]. The SIR circuit comprises on a single chip (size of 4 mm by 4 mm) a planar antenna integrated with an SIS (superconductor – insulator - superconductor) mixer, a superconducting flux flow oscillator (FFO) acting as a LO in the frequency range 400 - 700 GHz and the second SIS harmonic mixer (HM) to phase-lock the FFO.

The shape of the FFO radiation spectral line was found to be Lorentian [3], [4] at the frequencies up to 750 GHz. It indicates that the free-running ("natural") FFO linewidth is determined by the wideband noise, i.e. thermal fluctuations and the shot noise. It differs from many traditional microwave oscillators (for example, backward-wave and Gunn oscillators) where the "natural" linewidth is rather small and is broadened mainly by external fluctuations. For stabilization of the FFO frequency a specially designed wide-band phase locking loop (PLL) has been developed [4]. The effective bandwidth (BW) of the existing room temperature PLL (RT PLL) is about 10 - 12 MHz, while the FFO linewidth may exceed 10 MHz. The so-called "spectral ratio" (SR) is the ratio between the phase-locked and the totally emitted by oscillator power. The RT PLL provides SR value around 50% for the 5 MHz wide FFO radiation line. For the Terahertz Limb Sounder (TELIS) balloon project intended to measure a variety of stratosphere trace gases [5] the SR value better than 50% was desired.

The wider PLL BW is the more power of the FFO can be phase-locked (resulting in higher SR). The BW is determined by the group delay τ in the PLL loop. In our experiments the dependence of the SR on the length of the PLL cables was found to be linear in the wide range of parameters. [6]. The existing RT PLL has τ about 15 ns, which contains 5 ns contribution from the PLL filtering part and semiconductor electronics and 10 ns from the 2 m long cables connecting the RT PLL electronics with the HM and the FFO. The minimal length of the cabling is restricted by the geometric size of a cryostat and can not be essentially reduced without increasing the heat flux into the cryogen space. From the other hand the traditional PLL can not be placed directly into the cryogenic volume inside the cryostat, as it is a semiconductor-based device designed for room temperature.

There are several motives to extend the BW of the PLL systems for FFO phase-locking to values much higher than present 10 MHz. The FFO linewidth exceeds 10 MHz at the voltages above the one third of the FFO gap voltage, where the Josephson self-coupling effect drastically modifies FFO IVCs increasing differential resistance and internal damping [7], [8]. In case of such a wide line an essential part of the emitted FFO power can not be phase-locked with the RT PLL and contributes directly into the receiver phase noise.

An FFO based NbN or NbTiN films is the most attractive for future SIR applications at the frequencies around 1 THz. The linewidth of this type of the FFO can considerably exceed 10 MHz due to higher surface losses. In this situation the PLL has to have the bandwidth as large as 30 MHz (to reach the SR value desirable for most radio-astronomy projects), which can not be provided by the RT PLL.

Using an SIR for interferometry applications requires an LO with high phase stability. For example, for ALMA project (interferometer in Chile with the up to 15 km base line) the LO rms phase noise should be considerably less than 75 fs (the value of rms atmospheric fluctuation in location of the interferometer) [9]. The rms phase noise and SR of the phase-locked LO are related by:

$$\tau = \frac{1}{\omega_{LO}} \sqrt{\frac{100\% - SR}{SR}},$$

where ω_{LO} is the operation frequency of typical value about 600 GHz. From this dependence (see Fig. 1) one can estimate that the SR > 95 % is required for ALMA applications. To provide such a large SR value for the FFO with linewidth of 2 MHz the PLL should have BW about 50 MHz.

To improve spectral characteristics of the FFO and to overcome the limitation of RT PLL we propose the Cryogenic Phase Locking Loop system (CPLL). The key element of the CPLL is a cryogenic phase detector (CPD) [6] based on a well-developed tunnel SIS junction. The CPD can be placed very close to the FFO to minimize the loop length, since both devices operate at the same temperature; all other elements of the loop can be placed inside a cryostat as well. Negligible delay in the CPD and small time delays in the short loop lead to ultra wide BW.

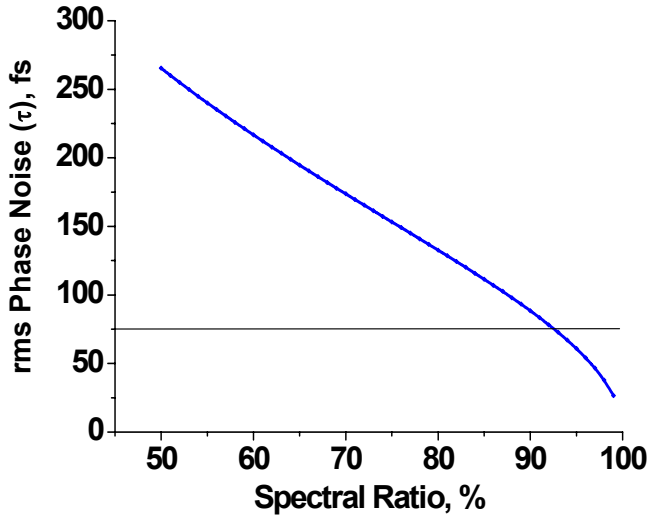

Fig. 1. Dependence of the rms phase noise value vs SR at ω_{LO} = 600 GHz.

A. *Cryogenic Phase Detector*

SIS junction is a well known mixer element due to its nonlinear properties; see [10] for example. Any mixer can operate as a phase detector, so a micron size Nb-AlOx-Nb tunnel junction with R_nS product (the product of the area and the normal state resistance) about 30 $\Omega^*\mu^2$ was chosen to be a cryogenic phase detector (CPD) for the CPLL.

B. *I-V curves of the CPD*

First successful results of the CPD implementation were presented very recently in [6]. A principle of the CPD operation can be demonstrated by IVCs of the SIS tunnel junction. A typical autonomous IVC of the SIS junction is shown in Fig. 2 (curve 1); curve 2 corresponds to the IVC of the SIS pumped by a microwave signal. Although the frequency of the synthesizer is a few GHz, and rather low compare to the smearing of the superconducting gap, the shape of the CPD IV-curve pumped by the synthesizer looks very much like a result of irradiation by a high frequency signal rather than a low frequency one. Moreover, this shape is qualitatively the same at the synthesizer frequency in range 0.4 – 10 GHz. Apparently, a certain number of higher order harmonics of the applied signal are excited in the SIS junction due to its non-linearity; these harmonics effectively pump the tunnel junction.

Curves 3 and 4 are measured in situation when the two microwave signals are fed to the junction in phase and with 180 degree shift correspondingly. The phase response, which is the difference between curve 3 and curve 4 is also presented in Fig. 2. A very important point here is that the phase response is almost independent on the CPD bias voltage above 1 mV. Looking forward we can say that the best bias voltage for CPD operation is in region 2...2.5 mV.

It was shown [6] that dependence of the phase response versus the phase difference between the two signals can be sinusoidal for the CPD under proper experimental circumstances (see inset in Fig. 2).

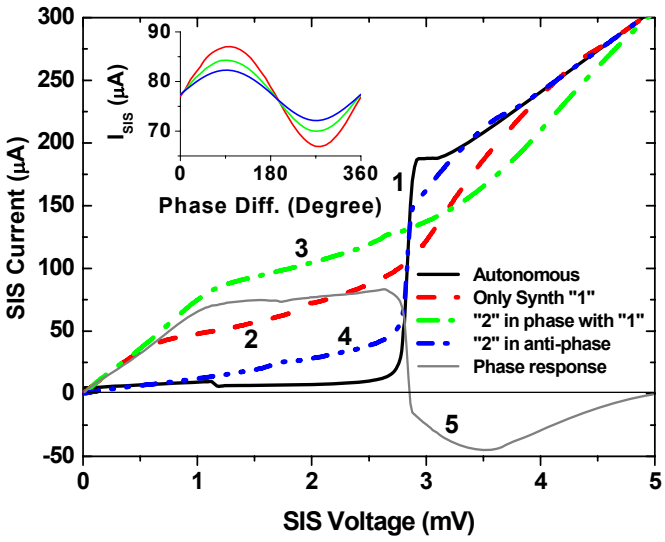

Fig. 2. IVCs of the SIS junction measured at different settings of the microwave signals (frequency 5 GHz): curve "1" – autonomous; "2" – pumped by one microwave signal; "3"- pumped by two microwave signals in phase; "4" – pumped by 2 microwave signal in anti-phase; PSynth1 = 0.3 μW, PSynt2 = 0.1 μW; "5" – phase response of the CPD – difference between curves "3" (in phase) and "4" (anti-phase). Inset shows a sinusoidal dependence of the SIS current on the phase difference between the signals.

C. CPD – FFO coupling

The phase response shown in Fig. 2 was measured at DC by voltage biased source. However, the CPD of the CPLL is supposed to be connected to the FFO control line channel (CL FFO) to tune the FFO frequency [8]. The frequency of the FFO is controlled by the two currents and the one, producing the magnetic field at the FFO ends (the so-called control line current I_{CL}) is employed as a FFO-CPD interface. The simplified equivalent diagram shown in Fig. 3 effectively describes this connection at frequencies of interest 0 – 100 MHz. The current source generates current I_0 and a part of it I split to the CPD. The CPD voltage V_0 can be expressed in terms of load R and current I from simple formula:

$$I_0 = I + V_0 / R .$$

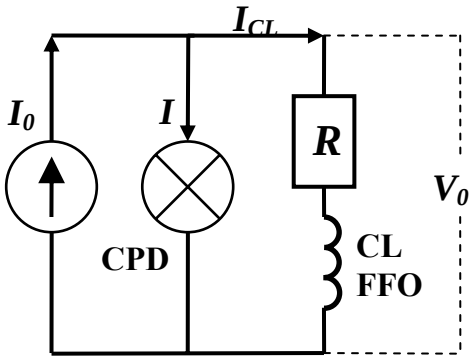

Fig.3 Simplified equivalent diagram of the CPD - FFO coupling. Connection that provides constant FFO CL current is not shown.

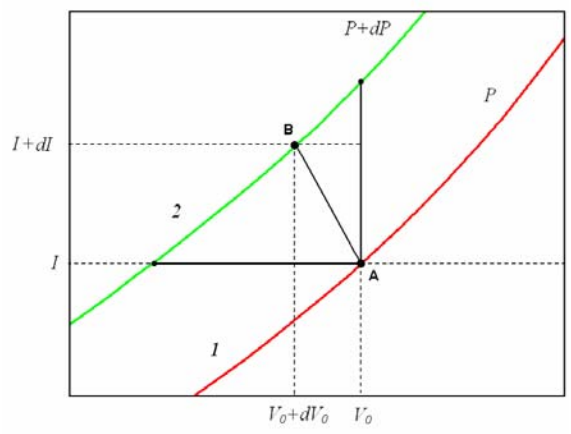

Fig. 4. Demonstration of the CPD operation with load R. Two IVCs of the CPD pumped at slightly diriment powers are presented.

Let's consider the microwave power P applied to the CPD and introduce it's variation dP to estimate the coupling between the FFO and the CPD. The current of the pumped junction depends on the power P (see Fig. 4 curves 1 and 2). The CPD biasing point goes along the load line $(1/R)$ from point A to point B at changing of the microwave power. The variation of the CPD voltage dV_0 is given by the relation:

$$dV_0 = -\frac{r_d R}{r_d + R}\frac{\partial I}{\partial P}dP ,$$

where r_d is a CPD differential resistance, $\partial I/\partial P$ is a partial derivative (can be calculated from the dependence $I(P)$ measured at the fixed CPD voltage). The contribution to the current I_{CL} from the CPD is the ratio dV_0/R. From these considerations the variation of the FFO frequency df_{FFO} is equal to:

$$df_{\mathrm{FFO}} = kdV_{\mathrm{FFO}} = k\frac{dV_0}{R}Rd_{\mathrm{CL\,FFO}} = -kRd_{\mathrm{CL\,FFO}}\frac{r_d}{r_d + R}\frac{\partial I}{\partial P}dP$$

Here $k = 483.6$ MHz/μV is the Josephson constant and $Rd_{\mathrm{CL\,FFO}}$ is the FFO differential resistance by I_{CL} (typically, about 0.02 Ω).

In case of the two microwave input signals of the power $P1$ and $P2$ with the phase difference φ the expression $\partial I/\partial P*dP$ should be replaced with $\partial I/\partial P*(P_1P_2)^{1/2}*d\varphi$ (here $P = (\sqrt{P_1} + \sqrt{P_2})^2$). So, for the two coherent signals:

$$df_{\mathrm{FFO}} = kdV_{\mathrm{FFO}} = -kRd_{\mathrm{CL\_FFO}}\frac{r_d}{r_d + R}\frac{\partial I}{\partial P}\sqrt{P_1P_2}d\varphi \quad (1)$$

This formula gives the efficiency of the CPD - FFO coupling and has been experimentally verified with a good accuracy [11]. An important result is the value of df_{FFO} is found to be linearly proportional to the derivative $\partial I/\partial P$. The CPD parameters r_d and $\partial I/\partial P$ can be preliminary measured to choose the best sample for the CPD operation. Detailed analysis of this formula is presented in the next chapter, where the CPLL optimization is considered.

Frequency parameters of the CPD are also an important issue briefly studied in [6]. The results of additional experiments demonstrate that the CPD is applicable for the FFO phase locking [11]. The operation frequency of the CPLL can be ranged from 200 MHz to 20 GHz and the response amplitude remains flat at least up to 750 MHz, that considerable exceeds 100 MHz required for the CPLL.

D. Cryogenic Phase Locking Loop System

Experimental Details

A block diagram of the CPLL is shown in Fig. 5. The FFO radiation of the frequency around 600 GHz is down converted by the harmonic mixer (HM) to the frequency 400 MHz and amplified by the two HEMT-amplifiers HEMT #1 and HEMT #2. This signal is compared by the CPD with the external reference signal and the resulting output error signal is proportional to the phase difference φ and fed to the FFO via the channel of the I_{CL} current. Some part of the microwave power after HEMT #1 is spitted to the spectrum analyzer by the directional coupler and can be also used as the input of the RT PLL and Frequency Detector, FD (the RT PLL and FD can operate together with the CPLL). It makes possible to stabilize the FFO frequency by the RT system mounted outside the cryostat.

The HEMT #2 varies the overall loop gain, it also is used to prevent a leak of the reference signal to the HM and spectrum analyzer. The total gain of the amplifiers is about 30 dB. The loop gain can be also controlled by the CPD gain factor, which depends on the CPD biasing voltage and the power of the reference signal.

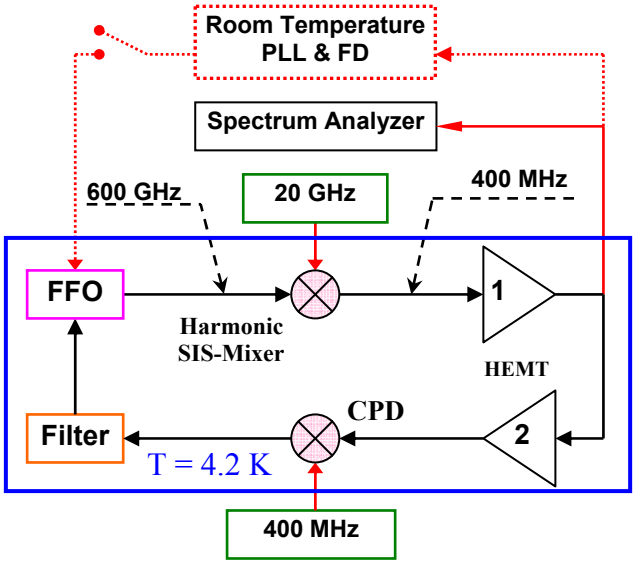

Fig. 5. Block diagram of CPLL for FFO.

The filter (see Fig. 5) blocks the signals around 400 MHz. There is very important requirement on the group delay introduced by the fitter - this delay should be as small as possible. So there are two main parameters of the filter: the group delay and a reflective characteristic (or transparency) at operation frequency. For better filter reflection a bigger value of reactive elements or higher number of them is necessary, but it leads to an increasing of the delay, so for these two parameters a trade off should be found. Two types of filters can be used: a low pass filter and a rejecter or a band-stop filter (the bandwidth of the stop-band should be no less than PLL BW to avoid a distortion of signal going to CPD from HEMT #2). The band-stop filter has smaller group delay than the low pass filter with the same reflective characteristic in the required frequency range, so a band-stop filter with a transparency -20 dB and the group delay 2 ns have been chosen for the presented CPLL. For the CPD output signal (frequencies up to 100 MHz) filter is transparent and only a resistance R (Fig. 3) is placed between the CPD and the FFO. It should be mentioned that such a filter will have significantly smaller delay for the CPLL with higher operation frequencies.

For optimization of the CPLL with the fixed loop length the effective CPD - FFO coupling and the minimal group delay in the filter of the loop must be achieved. The parameters for tuning are the load R and differential resistance r_d of the CPD (by varying the area of the SIS junction S). We assume that the R_nS product and filter parameters are fixed. Analyze is based on formula (1) and gives the following results:

1) value of R should be smaller then r_d (optimal value is R *of* about $0.2r_d$);

2) the larger area S the better is the CPD - FFO coupling. At realization of these conditions some problems can be foreseen: a) large required power of the microwave signal for the CPD pumping (larger SIS needs more power, while small r_d causes a bad coupling of the CPD with 50 Ohm source of microwave signal), b) larger power of the microwave signals will require a modification of the filter for better reflection, that leads to increasing of the group delay, c) increasing of the filter group delay because of its input and output impedances (r_d and R) decreasing. Taking into account all these conditions the CPLL have been realized with area of the CPD S ≈ 1 um^2 (r_d ~ 50 Ohm) and R = 10 Ohm.

The results presented for the CPD are obtained with suppressed critical current (CC) of the SIS junction. There is no significant influence of the CC on phase response, but for the CPD implementation in real CPLL system the CC can results in instability of the FFO line, high noise level and excitations in the loop. The way to minimize CC influence is to work at the CPD voltages about 2.5 mV (almost near the gap voltage). However, it is better to suppress the CC.

E. Experimental Results

The presented realization of CPLL has the length of the loop about 1 m (group delay 5 ns). The delay in filter is 2 ns. So the total group delay is 7 ns (compare to 15 ns for the RT PLL). This reduction of the loop delay results in increasing of the BW from 12 MHz to 25 MHz (see Fig. 6). For the FFO linewidth of 2 MHz this CPLL is able to phase-lock 91% against 82% for the RT PLL. For the FFO linewidth as large as 10 MHz the CPLL gives SR = 50% instead of 20-25% for the RT PLL. A summary of these results is presented in Fig. 7.

The dependences of the SR vs FFO linewidth demonstrates the efficiency of the FFO phase locking by different systems. The stars show the experimental data for the RT PLL with the BW of 12 MHz. Dashed line is a result of simulations approximating the experiment [12]. The “regulation BW” of 10 MHz in simulations corresponds to “BW” = 12 MHz in experiment. The measurements for the CPLL (squares) approximated theoretically by a solid line for regulation BW 20 MHz show the advantage of BW widening and prospects for future improvement. We can say roughly that a twice wider FFO line can be phase locked by the PLL with two times wider BW resulting in the same SR.

Phase noise of the FFO locked by the two systems is shown in Fig. 8. This figure demonstrates an advantage of the CPLL on the RT PLL in the range of offsets from the carrier higher 10 kHz, whereas there is a strong increasing of phase noise level for the CPLL at small offsets from the carrier frequency. This noise increasing is because the CPLL is a first-order PLL system without additional amplifier and any integration filter in the loop. An amplifier and integration filter will give an improvement of a phase noise performance and CPLL stability (wider holding range).

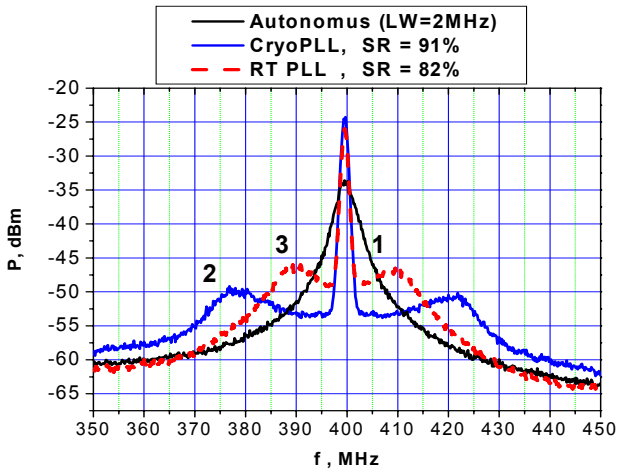

Fig.6. . Down-converted spectra of the FFO operating at 600 GHz: curve "1" – autonomous, "2" – phase locked by CPLL; "3" – phase locked by RT PLL.

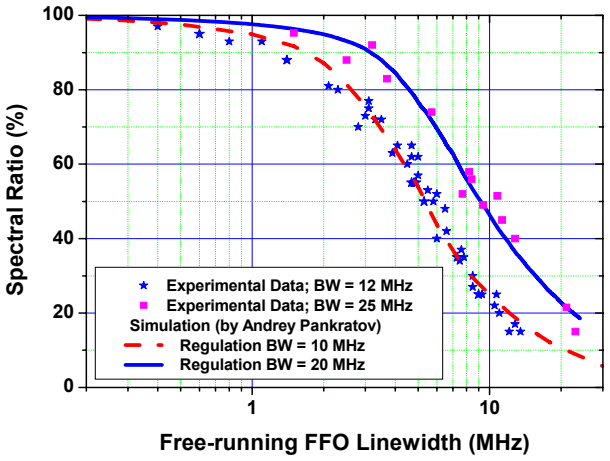

Fig.7. Dependence of the SR vs FFO linewidth for different PLL bandwidths.

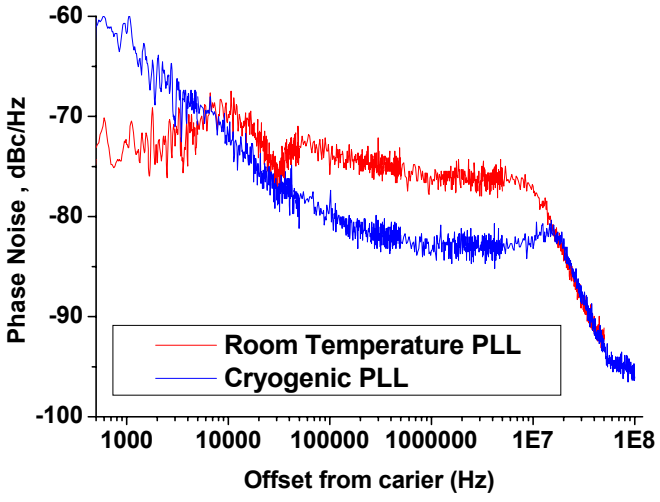

Fig. 8. Phase noise diagram of the phase-locked FFO (linewidth is 4.3MHz).

CONCLUSIONS

Ultra wideband Cryogenic Phase Locking Loop system has been developed and tested. The CPLL has a bandwidth wider than 25 MHz and demonstrate an evident advantage on the RT PLL. The novel CPLL system can phase-lock more than 50% of the FFO spectral line if the free-running FFO is about 10 MHz. Practical implementation of CPLL looks especially promising for the development of the SIR arrays.

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