A Novel Dual-Chip Single-Waveguide Power Combining Scheme for Millimeter-Wave Frequency Multipliers

José V. Siles, *Member IEEE*, Alain Maestrini, *Member IEEE*, Byron Alderman, Steven Davies, and Hui Wang

***Abstract*—In this work, we propose a novel dual-chip power combining scheme where two symmetrical MMIC chips are mounted on a single transmission waveguide. This configuration adds an extra degree of freedom in power combining as it allows to double the number of diodes in split-block waveguide multipliers, and thereby, to increase the power handling capabilities of frequency multipliers by an additional factor of 2. The two chips are symmetrically placed along the E-plane within the transmission waveguide. This adds an additional symmetry plane that simplifies the computational cost of the circuit simulations since just half of the structure can be simulated by defining a perfect H-plane boundary condition at the symmetry plane. The proposed topology is demonstrated throughout the design of a dual-chip biasless 190 GHz broadband Schottky doubler based on United Monolithic Semiconductor's (UMS) technology.**

***Index Terms*—Circuit simulation, Millimeter-wave circuits, Power combiners, Schottky diodes, Schottky diodes frequency converters.**

I. INTRODUCTION

BIG efforts have been made in the recent years to develop solid-state sources providing high local oscillator (LO) power levels at millimeter-wave bands. State-of-the-art sources have already demonstrated LO power levels up to 800 mW at 90-100 GHz, and up to several watts are expected at 100 GHz with MMIC amplifiers based on GaN transistors [1]. This represents a good opportunity to continue improving the LO power generation at THz frequencies by means of Schottky multiplier chains.

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J. V. Siles, was with LERMA, Observatory of Paris, 75014 Paris, France. He is now with the Department of Signals, Systems and Radio-communications, Technical University of Madrid, 28040 Madrid, Spain (phone: +34 657231217, fax: +34 913367362; e-mail: jovi@gmr.ssr.upm.es).

A. Maestrini is with LERMA, Observatory of Paris, 75014 Paris, France (e-mail: alain.maestrini@obspm.fr).

B. Alderman is with the Rutherford Appleton Laboratory, Chilton, Oxfordshire, OX11 0QX, UK (e-mail:B.Alderman@rl.ac.uk).

S. Davies is with the Department of Physics, University of Bath, Bath BA2 7AY, UK (e-mail:s.r.davies@bath.ac.uk).

H. Wang was with LERMA, Observatory of Paris, 75014 Paris, France. She is now with the Rutherford Appleton Laboratory, Chilton, Oxfordshire, OX11 0QX, UK (e-mail:hui.wang@stfc.ac.uk).

However, traditional multiplier chains based on GaAs Schottky diodes cannot handle such amount of LO power since chips featuring either a large number of diodes or excessively large anode areas would be required. In split-waveguide designs, the size of the chip is limited by the dimensions of the transmission waveguide and other constraints [2].

Several alternatives may be considered to deal with this problem. On the one hand, Schottky diodes based on semiconductor composites with larger bandgap than GaAs might be employed for the first multiplication stages of THz LO chains. In this context, GaN Schottky multipliers featuring 2 or 4 diodes could easily handle a 1 W input power at 100 GHz although conversion efficiencies would be around a 25 % lower than those achieved with GaAs Schottky diodes due to the lower electron mobility of GaN [3]. Novel materials like carbon nano-tubes and graphene, featuring both large bandgap and high electron mobilities, could be also employed in the near future for Schottky multipliers [4, 5].

On the other hand, power-combining schemes also offer a very good alternative to increase the power handling-capabilities of GaAs Schottky multipliers [1]. One possible power-combining scheme has been recently demonstrated with excellent results for a 300 GHz tripler. It consists of two mirror-image tripler circuits that are power-combined in-phase in a single waveguide block using compact Y-junctions at the input and output waveguides [2].

This work proposes a novel dual-chip single-waveguide power combining-scheme that adds an additional symmetry to the multiplier circuit, increasing by an additional factor of two its power handling capabilities. This topology is demonstrated through the design of a 190 GHz doubler with UMS technology. The most important design and technical difficulties connected to this topology are also outlined herein. The design of the doubler has been carried out at LERMA, Observatory of Paris, and the post-processing at the University of Bath. Block fabrication and assembly will be performed at Rutherford Appleton Laboratory, Oxford (UK). Results from the 1st foundry run were not satisfactory mainly due to wafer imperfections and difficulties in the block assembly as a consequence of the complex topology, For the 2nd run, a ~10 % efficiency over a ~15 % 3-dB bandwidth is expected.

II. Dual-Chip Single-Waveguide Power Combining Scheme for Multipliers

The dual-chip single-waveguide power combining scheme proposed in this work consists of two chips symmetrically placed along the E-plane of the transmission wave-guide, as it is shown in Fig. 1. With this topology, the power handling capability of a frequency multiplier is increased by a factor of two since it features double number of anodes than a single-chip design. In order to maximize the input power coupled to the diodes, the distance between the chips must be as lowest as possible so they are located near the center of the waveguide where the maximum of the exciting TE_{10} mode is.

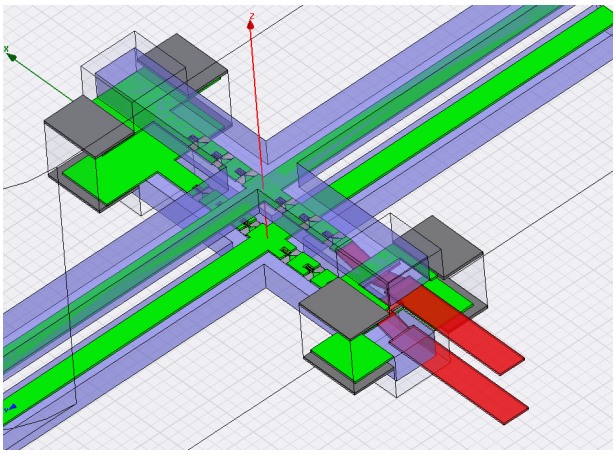
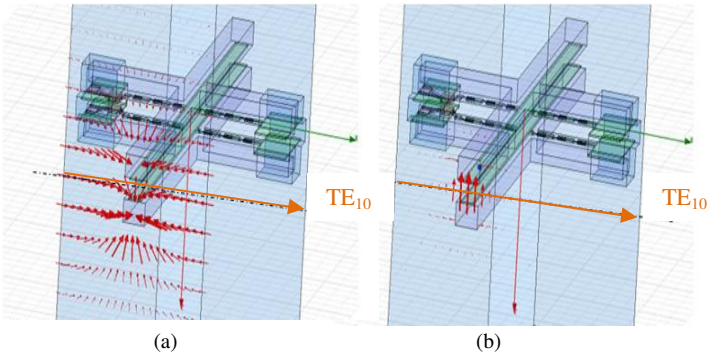


Fig. 1. Dual-chip single wave-guide scheme for frequency multipliers.

The two suspended microstrip lines can theoretically propagate two quasi-TEM modes (see Fig. 2). However, only one quasi-TEM mode (Fig. 2a) will be excited since the electric field lines of the second quasi-TEM mode (Fig. 3b) will be orthogonal to the input TE_{10} mode according to the geometry of the circuit. Note that the electric field corresponding to the 1st quasi-TEM mode (Fig. 2a) is tangential to the symmetry plane. Hence, if a perfectly symmetric circuit is assumed, only half the structure (with only one chip) can be simulated in HFSS by defining a perfect H-plane boundary condition at the symmetry plane. This reduces the computational cost of the design process.



(a) (b)

Fig. 2. Theoretical quasi-TEM modes propagated by the two suspended striplines of the proposed dual-chip power combining scheme.

Contrarily to the in-phase power combining scheme shown in [2] (see Fig. 3), the topology proposed here does not use duplicated circuits combined by means of Y-junctions at the input and at the output because the two chips are embedded in a single waveguide. Hence, the complexity of the block is reduced. However, the assembly procedure in the dual-chip single-waveguide structure becomes much more complex because a very precise control in the positioning of the two chips is crucial in order to guarantee the symmetry of the circuit. This and other difficulties concerning the proposed scheme will be discussed in the following section.

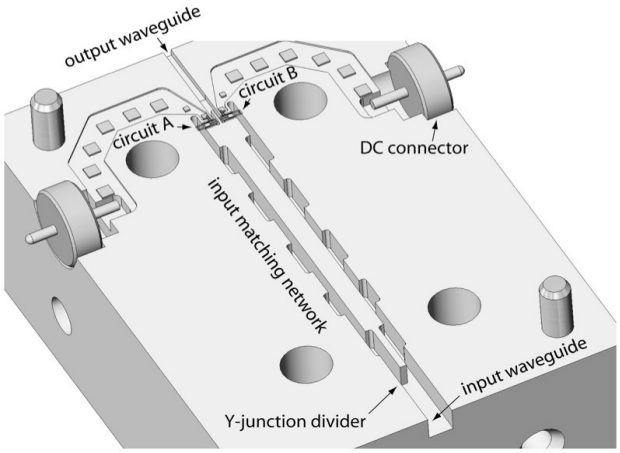


Fig. 3. In-phase power-combined dual-chip tripler at 300 GHz (proposed by A. Maestrini [2]). Each chip is assembled onto a different waveguide. Y-junctions are employed for power-combining.

It is important to remark that a combination of these two schemes might be employed in order to achieve a X4 increase in the power-handling capability of a traditional multiplier.

III. Fabrication Difficulties

The main difficulties concerning this novel dual-chip power-combining scheme are presented through the measurement results corresponding to the 1st foundry run of the design of a dual-chip 190 GHz Schottky doubler based on UMS technology (featuring 6 anodes per chip). This doubler was initially designed for a 100 mW input power and a -12 V reverse bias voltage per chip (-2 V per anode) since the nominal breakdown voltage provided by UMS was -6 V per anode. The expected efficiency was 25 % over a 6 % 3-dB bandwidth. However, the actual breakdown voltage of the chips was found to be -2 V per anode due to deficiencies in the wafer during the fabrication process, and thereby, a -12 V reverse bias voltage per chip could not be applied. Moreover, the actual GaAs-substrate thickness of the chips ranged between 32 µm and 36 µm, instead of the nominal value of 50 µm. The distance between the chips after the assembly was also measured and a non-uniform separation varying between 32 and 44 µm along the channel was found (nominal design distance between chips was 40 µm).

Under these circumstances, the measured performance of the doubler was extremely poor as it can be seen in Figs. 4 and 5. The bias voltage of each chip was optimized for each analyzed frequency in the tests in order to maximize the provided output power. The input power was fixed to 50 mW in order not to overpump the diodes. RF measurements showed an important asymmetry in the effective power coupled to each chip whereas the measured I-V curves at DC corresponding to each chip were found to be exactly

symmetrical. The measured maximum output power was 0.450 mW. It can be seen in Fig. 4 that only in the vicinity of the peak of efficiency both chips demand the same bias voltage for optimum performance of the doubler. Out of this zone, important discrepancies can be observed in the optimum bias voltage that was found for each chip. It was also noticed during the test that the doubler efficiency experiences a certain variation (from 0.7 % to 0.85 % in Fig. 4) when acting on the screws of the block. This could be due to the fact that this mechanical operation changes the distance between the chips compensating somewhat the asymmetries in this distance. The problem with the lack of symmetry becomes even more evident when measuring the DC current across each chip. Big discrepancies can be observed in Fig. 5 between the two chips even in the case when similar bias voltages are selected for each chip.

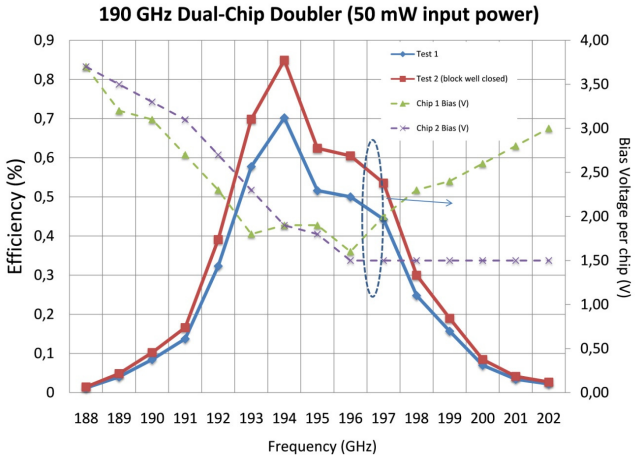


Fig. 4. Measured efficiency of the 190 GHz doubler (1st foundry run). Dashed lines indicate the optimum bias voltage for each chip to maximize measured efficiency.

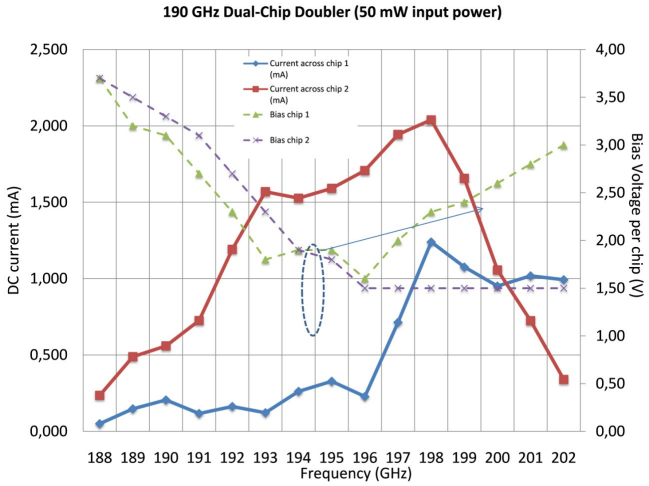


Fig. 5. Measured DC current across each chip of the 190 GHz doubler (1st foundry run). Dashed lines indicate the optimum bias voltage for each chip to maximize measured efficiency.

To summarize, it is evident that the sensitivity of the doubler to the distance between the chips is high so a larger separation between them is necessary due to the difficulty in precisely controlling this distance during the assembly if it is excessively small. Furthermore, a high accuracy is also necessary during the fabrication and post-processing of the chips in order to reduce as much as possible the asymmetries in the circuit.

IV. Design of a Dual-Chip Single-Waveguide 190 GHz Doubler (2nd Foundry Run)

The doubler is a split-block waveguide design that features twelve UMS Schottky planar diodes on two chips monolithically fabricated on a 50-µm GaAs-based substrate. Diodes on each chip are connected in series at DC and both chips are inserted within the output waveguide. Each of the two E-plane probes located in the input waveguide couple the signal at the fundamental frequency to each chip. The waveguide channel between the input and output waveguides prevents the second harmonic from leaking into the input waveguide. The distance between chips is 100 µm to favor the assembly and reduce the impact of misalignments. The general scheme of the 190 GHz doubler can be seen in Figs. 6 and 7.

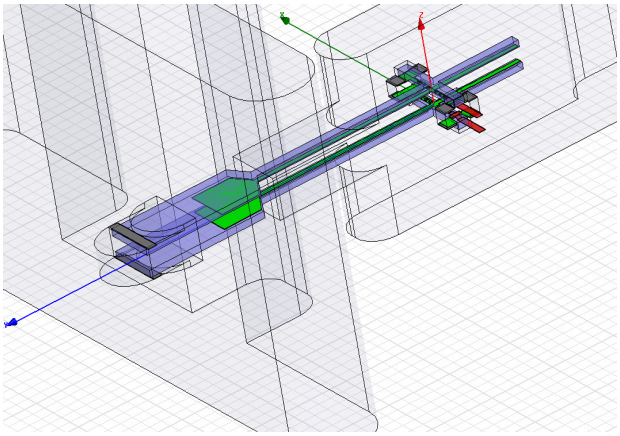


Fig. 6. General scheme of the dual-chip single-waveguide 190 GHz doubler.

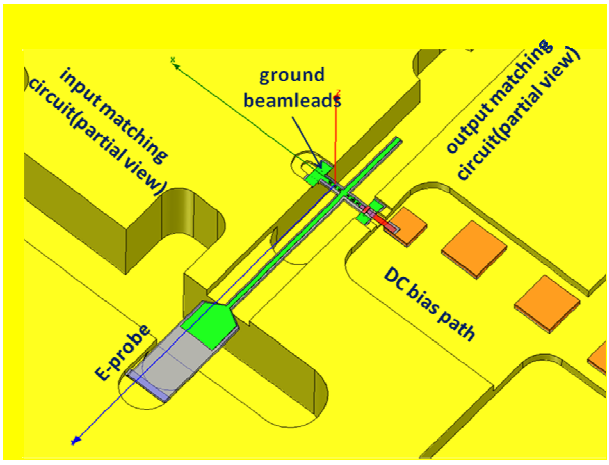


Fig. 7. 3D view of the bottom part of the waveguide block with the 190 GHz doubler bottom chip installed. It features 6 Schottky diodes in a balanced configuration. The upper part of the block contains the second chip, which is symmetrical to the bottom chip.

The circuit features additional matching elements in the input and output waveguides, made with a succession of waveguide sections of different heights and lengths (see Fig. 8).

The Schottky diodes provided by UMS for this work are adequate for mixers but not for multipliers. Both the epilayer

thickness and doping are not optimum for a state-of-the-art doubler design in terms of efficiency: diode epilayer is already fully depleted at ~ 0.1 V and the expected DC breakdown voltage for this wafer is ~ -5 V. Under these circumstances, the optimum bias voltage per anode should be around -3 V in order to maximize the power handling capabilities of each anode. However, a biasless design was finally considered in order to enlarge the frequency bandwidth and guarantee safe operation regime for the diodes. The use of a dual-chip topology for this design is necessary to increase the number of diodes, and thereby, the supported input power. Note that individual DC bias lines for each chip have been included in order to add a tuning parameter to deal with possible asymmetries between the two chips.

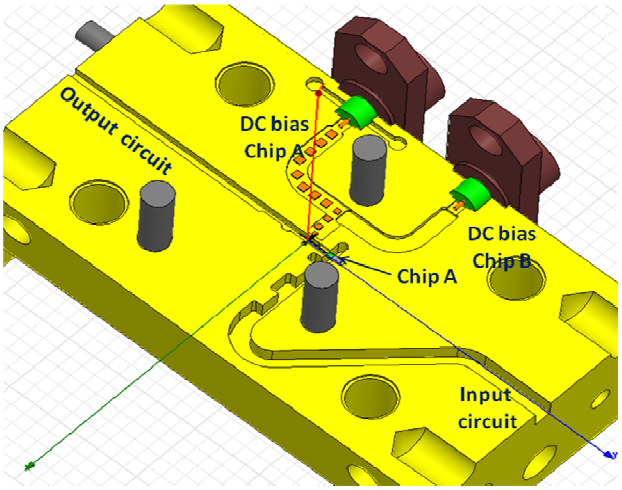


Fig 7: 3D view of the bottom part of the waveguide block, showing the two DC bias paths (one per chip).

The design methodology combines Agilent's ADS linear/nonlinear harmonic balance circuit simulation to optimize and compute the performance of the circuit, with Ansoft's HFSS 3D electromagnetic simulation to model accurately the diodes geometry and waveguide structures. Due to the special characteristics of the provided UMS diodes, simple analytical nonlinear Schottky diode models, like the standard Schottky diode model included in ADS, are not valid. The Schottky model employed for this design in ADS simulations has been specifically adjusted by means of empirical results and physics-based simulations.

A room-temperature conversion efficiency of a ~10% over a 15% 3dB-bandwidth is expected for the 2nd foundry run of the dual-chip single-waveguide 190 GHz doubler, as can be seen in Figs. 8 to 11. An available input power of 80 mW has been considered and the DC characteristics of the employed diodes are the following: a 18 fF zero junction capacitance (C_{j0}), a 4.4 Ω series resistance (R_s) and a ~$4 \cdot 10^{-14}$ A saturation current (I_s). The fabrication and post-processing have been improved with regards to the 1st foundry run in order to avoid some of the technical difficulties discussed in the previous section. Furthermore, the larger separation between the two chips makes it easier the assembly of the chips guarantying a more accurate control of the distance during the assembly.

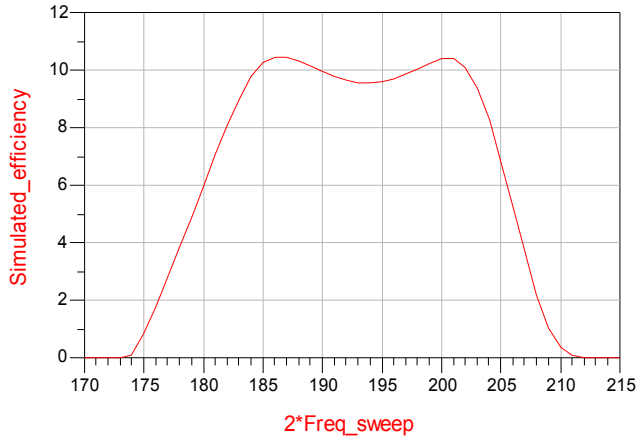


Fig 8: Predicted efficiency (%) of the 12-anode dual-chip 190 GHz balanced doubler at room temperature with 80 mW input power.

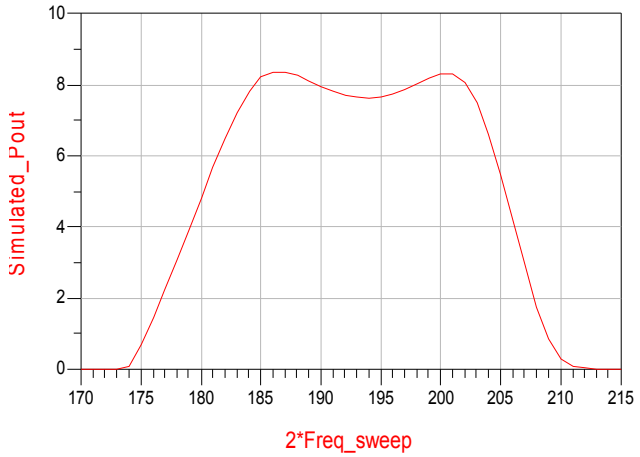


Fig 9: Predicted output power (mW) of the 12-anode dual-chip 190 GHz balanced doubler at room temperature with 80 mW input power.

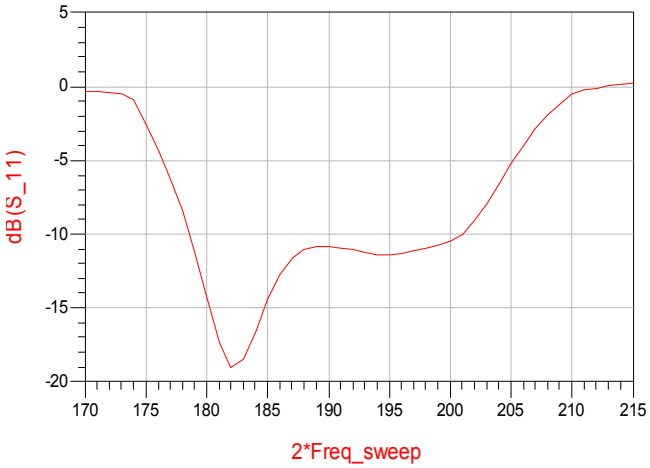


Fig 10: Predicted input matching of the 12-anode dual-chip 190 GHz balanced doubler at room temperature with 80 mW input power.

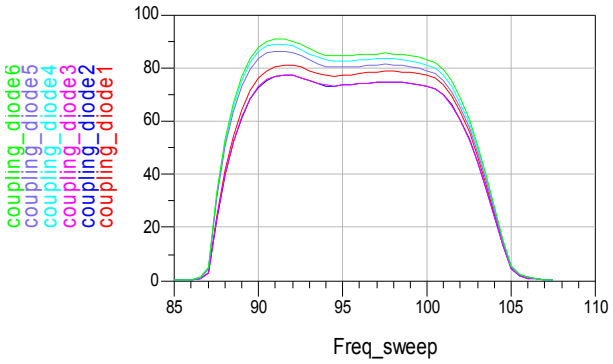


Fig 11: Predicted input coupling to each diode corresponding to the dual-chip 190 GHz balanced doubler at room temperature with 80 mW input power.

V. Conclusion

A novel dual-chip single-waveguide power combining scheme for frequency multipliers has been proposed and demonstrated through the design of a 190 GHz doubler. It allows to double the number of diodes in the design in order to increase the power handling capabilities of the multiplier. State-of-the-art efficiencies cannot be achieved with this specific design due to the limitations of the Schottky diodes provided by UMS to operate as multipliers. However, with an accurate control of the fabrication and assembly processes to guarantee the symmetry between the two chips and well optimized diodes (to be used as multipliers), state-of-the-art performances would be obtained without sacrificing efficiency or bandwidth compared with a single chip implementation. This work represents a further step to increase the LO power provided by multiplier-based solid-state sources beyond 1 THz.

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