

Design and Fabrication of 190-GHz Dual-Chip Single-Waveguide Schottky Doublers

José V. Siles^{1,2}, Alain Maestrini², Byron Alderman³, Steven Davies⁴, Hui Wang³ and Tapani Närhi⁵

¹Dept. Signal, Systems and Radiocommunications
Technical University of Madrid, Spain
Email: jovi@gmr.ssr.upm.es

²Université Pierre et Marie Curie–Paris 6 &
Observatoire de Paris, LERMA, France
Email: alain.maestrini@obspm.fr

³Dept. Millimetre-Wave Technology
Rutherford Appleton Laboratory, UK
Email: byron.alderman@stfc.ac.uk

⁴Department of Physics
University of Bath, UK
Email: s.r.davies@bath.ac.uk

⁵European Space Agency (ESA/ESTEC), Email: tapani.narhi@esa.int

Abstract

The next generation of Schottky multipliers will take advantage of the high power already available from driver amplifiers (up to 500 mW in the 70-113 GHz band) and of the several watts expected at 100 GHz from MMIC amplifiers based on GaN transistors [1]. Power-combining strategies consisting in using several chips on a single split-waveguide multiplier block [2,3] will make it possible to handle the high LO power provided by state-of-the-art LO sources at 100 GHz, and thereby to increase the available LO power at terahertz frequencies.

In this work, we will present the design of power-combined 190-GHz Schottky-diode doublers using United Monolithic Semiconductor (UMS) BES Schottky process based on the dual-chip single-waveguide topology described in [3]. The doublers feature two MMIC chips with a series array of 6 planar Schottky diodes each, integrated into a 50- μm -thick GaAs substrate. A bias-less design was chosen to accommodate the mixer-optimized UMS BES Schottky diodes that feature short epilayers and subsequently relatively low breakdown voltages. Two designs have been made. The first one consists of two symmetrical circuits that incorporate beam-leads ground connections and a cross-shape 50- μm -thick substrate for lowering the dielectric load. This version of the doubler requires several post processing steps after the completion of the nominal UMS BES process. These steps are performed at the University of Bath and at the Rutherford Appleton Laboratory (RAL). The second version of the doubler does not require post processing steps. It features two symmetrical circuits implanted on a 50- μm -thick rectangular substrate and no beam leads are employed.

The first design with post-processing is expected to achieve ~10 % efficiency over a 15 % 3-dB bandwidth, whereas 7-10% efficiency over a 12 % 3-dB bandwidth is predicted for the second design without post-processing. The MMIC chips for both 190-GHz doublers have been already delivered by UMS and the multiplier blocks are now under process at RAL. RF measurements of the doublers are planned for the beginning of 2010. This work was supported by the European Space Agency and the CNES.

REFERENCES

- [1] J. S. Ward, G. Chattopadhyay, J. Gill, H. Javadi, C. Lee, R. Lin, A. Maestrini, F. Maiwald, I. Mehdi, E. Schlecht and P. Siegel, "Tunable broadband frequency-multiplied terahertz sources," *33rd International Conference on Infrared, Millimeter and Terahertz Waves*, Sep. 2008.
- [2] A. Maestrini, J. S. Ward, C. Tripon-Canseliet, J. Gill, C. Lee, H. Javadi, G. Chattopadhyay and I. Mehdi, "In-phase power-combined frequency triplers at 300 GHz," *IEEE Microwave and Wireless Component Letters*, vol. 18, no. 3, pp. 218-220, Mar. 2008.
- [3] J. V. Siles, A. Maestrini, B. Alderman, S. Davies, and H. Wang, "A novel dual-chip single-waveguide power combining scheme for millimeter-wave frequency multipliers," *20th International Symposium on Space Terahertz Technology*, pp. 205-209, Apr. 2009.