Modeling SIS Junction Arrays for APEX Band 3 (385–500 GHz)

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Abstract— **A methodology for the modeling of superconducting-insulator-superconducting (SIS) junction arrays will be presented and compared with measured results. In many cases, junction arrays (either in parallel or series) are treated as a single equivalent junction. The APEX Band 3 (385–500 GHz) receiver design has been implemented with two junctions connected in parallel via a section of inductive microstrip line. In this case, it is desirable to separately model each junction as the pumping between junctions is no longer symmetrical across the entire band. Since the performance of the SIS junction depends on its terminating network, a complicated interaction occurs when another junction is part of the embedding impedance and, therefore, there remain aspects of its performance that are difficult to analyse. A simplified model, demonstrated with MATLAB, will be given and compared with a more complete model implemented using a common circuit simulator, Agilent ADS. In both cases, each junction is represented by a quasi 5-port network determined using the quantum theory of mixing. The model is then used to predict the performance of the APEX Band 3 mixer and compared with measured results.**

I. Background and Motivation

One common topology for superconducting-insulator-superconducting (SIS) mixer design is to use parallel junctions connected by a section of inductive microstrip line. This has been referred to as the twin junction, as in [1], parallel-connected twin junctions (PCTJ) in [2] and an asymmetric "two-feed" configuration [3]. The twin junction has a wide operating bandwidth, as first proposed in [4], and improved power handling, as is common to all junction arrays. The twin junction also offers a unique advantage due to its self-terminating structure such that the dependence of the admittance of the connecting circuitry (i.e., the probe) is reduced; that is, for each junction the opposite junction is in parallel with the rest of the circuit admittance.

The twin junction may be impedance matched using values realizable with microstrip transmission line, given the SIS junction fabrication constraints. A simplified waveguide-based design approach consisting of an E-probe, microstrip quarter-wave transformer, and twin junction is outlined below:

- Choose the lowest reliable R_NA for fabrication of the wafer, since lower R_NA implies broader bandwidth (where $Q = \omega R_N C_J = \omega(R_N A)C_S$ is a measure of bandwidth, R_N is the normal state resistance, C_J is the junction capacitance, A is the junction area, and C_S is the specific capacitance). A good design value is ~20–30 Ω μm^2.
- Design an RF probe with the lowest achievable impedance covering the frequency range; often resulting in a value approximately 35 Ω.
- Choose a suitable characteristic impedance for the microstrip quarter-wave transformer. Fabrication constraints limit the upper range of characteristic impedance of the microstrip to around 13 Ω (given a single deposition process step of SiOx with a thickness between 100–300 nm and minimum Nb line widths of ~5 μm).
- With the given probe and quarter-wave transformer impedances, this results in a transformed impedance of a few Ohms. Since SIS junctions have an RF impedance approximately equal to R_N at these frequencies of interest, the twin junction circuit has an impedance close to $R_N/2$ at the mid-band frequency, therefore a target R_N of ~6–8 Ω is used and the junction size determined.
- The length of the microstrip connecting the junctions is chosen so that the input impedance of the twin circuit has a resonance centred within the band.

As can be seen from this approach, impedance matching to the probe (or coupling at RF) is emphasized. Following this methodology, a promising design for the APEX telescope receiver band 3 (385–500 GHz) was shown in [5]. It is novel, employing a key integration of the LO coupler which drives many features of the design. The coupler, in this case, also serves as the quarter-wave transformer between the probe and the twin circuit, and is a hybrid slot microstrip coupler which employs the use of slots cut into the ground plane to achieve the desired coupling. Another feature of the slots is that the LO feeding circuitry is de-coupled from the IF, reducing the IF capacitance.

Typical results of the mixer chip are shown in Fig. 1 and indicated a frequency offset in the noise performance. Several key improvements were made in the processing, described in [6], yet still the offset persisted. Furthermore, it was difficult to differentiate between the effects of the integrated LO circuitry and the matching to the twin SIS structure; this served as motivation for a more detailed look at the interaction between the two junctions.

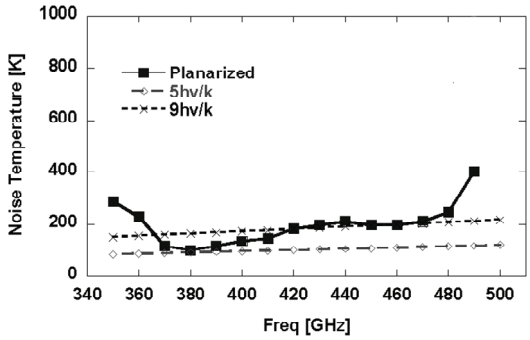

Fig. 1 Measured DSB results showing a frequency offset in performance. Figure is from [6].

II. First Approach using MATLAB

As pointed out in [3], the large signal response (i.e., the LO signal) is distributed between the junctions asymmetrically across the entire frequency band. Also, since the performance of the SIS junction depends on its terminating network, a complicated interaction occurs when another junction is part of the embedding impedance and aspects of its performance are difficult to analyse. How does the inevitable phase difference between the junctions affect the performance? How do the noise components of each junction combine? What is the resulting noise and signal power delivered to the IF? What role does pumping symmetry between the junctions play? To address these questions, each junction was represented using the theory outlined in [7].

The usual simplifying assumptions were made concerning the large signal analysis; a quasi 5-port analysis was used for each junction with only the fundamental of the LO considered but with the sideband harmonics terminated by the junction capacitance [8].

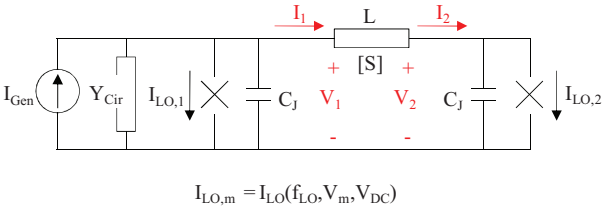

Fig. 2 Large signal view of twin circuit. V_1 and V_2 are the complex large signal voltages that determine the pumping level for each junction. I_{LO} is the complex tunneling current through each SIS junction as given in [7], I_{Gen} is the generating current source of the LO, Y_{Cir} is the admittance of the entire circuit excluding the twin circuit (e.g., the probe and transformer), C_J is the junction capacitance, and L is the s-parameter matrix describing the inductive microstrip line between the junctions.

Fig. 2 illustrates the circuit that must be solved for each LO frequency. A simplifying assumption can be made such that one may assume that I_{Gen} may be adjusted, in amplitude and phase, so that V_2 has zero phase and some initial magnitude [3]. For example, as an initial starting point, the LO pumping across *junction 2* may be set at $\alpha_2 = eV_2/hf_{LO} = 1$. Under this simplification, V_1 may be found using:

$$I_2 = Y_{CJ}V_2 + I_{LO,2} \quad (1)$$

and

$$V_1 = A(V_2) + B(I_2) \quad (2)$$

where A and B are from the ABCD matrix of the microstrip line connecting the junctions. From this it is clear that the pumping symmetry of the junctions is determined by the relationship between C_J and the length of microstrip line between the twin junctions.

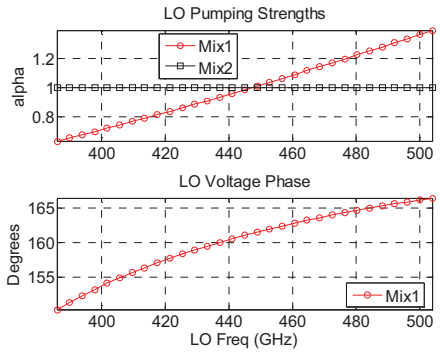

Fig. 3 Large signal voltage distribution between junctions in the twin circuit as illustrated in Fig. 2. In this case, the length of microstrip line connecting the junctions has been chosen to resonate at the middle of the band. Note that the phase difference is the LO phase across *junction 1* with respect to *junction 2*.

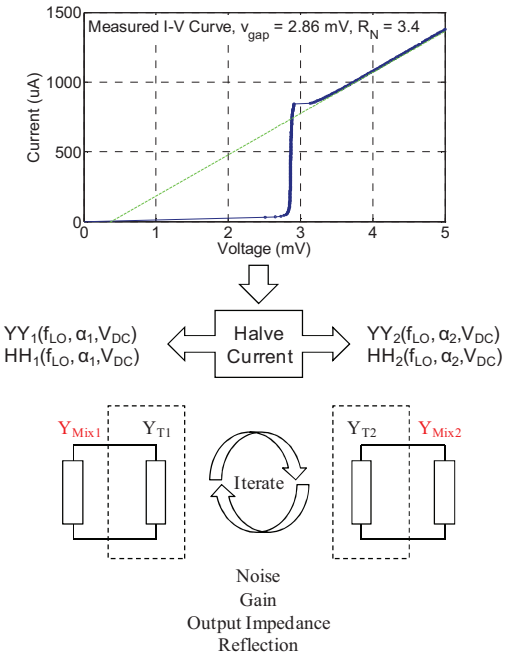

Fig. 4 Overview of the small signal modeling approach for the twin junction mixer. Beginning with a measured I-V curve, the small signal admittance and noise correlation matrices, *YY* and *HH*, are found according to the LO pumping levels (e.g. shown in Fig. 3). The small signal parameters are then calculated according to the termination matrix, Y_T, for each junction (shown in Fig. 5).

Fig. 3 shows how the relative pumping relationship between each junction undergoes a reversal above the

resonant frequency. Note that in practice, it is not possible to distinguish between the current of each junction during measurement and, in realistic tuning, as the LO power is optimised, the current through each junction is simultaneously established. In this way, it is seen that Fig. 3 is a simplification, but it is useful for analysing the pumping asymmetry and to therefore better understand the twin tuning circuitry. In paragraph III, the assumption of pumping levels is extended by constraining both junctions to a fixed value in an effort to more closely replicate practical tuning.

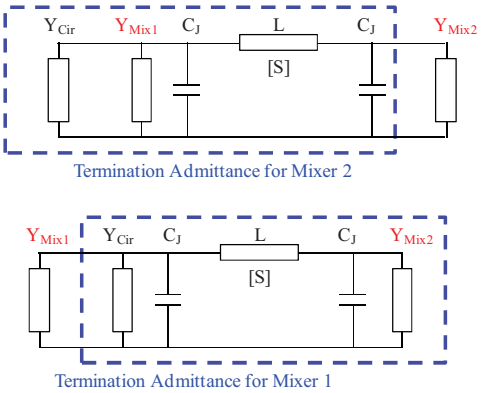

Fig. 5 Illustration of the embedding impedances, or termination matrix Y_T, of each junction within the twin junction topology. Y_{Cir} is the admittance of the entire network (i.e. the probe, choke and transformer) excluding the twin circuit, C_J is the geometric capacitance of the SIS junction, L is the inductive microstrip line connecting the junctions and Y_{Mix} is the admittance of the junction which depends on its terminating matrix. Note that circuit elements are defined for each sideband frequency.

Using the unique pumping strengths of each junction, α_1 and α_2, the small signal analysis can be computed as shown in Fig. 4 and Fig. 5. Since the measured I-V curve includes both junctions, a new I-V curve for parallel junctions can be created by halving the current which is then used to compute the small signal noise and admittance matrices, *HH* and *YY*. The final step is to find the appropriate embedding impedance for each junction, referred to here as the termination matrix of each junction, Y_T. An iterative process was used, with R_N used as an initial guess at all sideband ports for each mixing junction. Within this initial modeling approach, only the small signal parameters delivered to each termination matrix were determined. In other words, the responses from each junction were analysed separately and not combined.

In retrospect, the following inconsistencies contributed to inaccuracies during this first approach to modeling. The phase difference of the large signal voltage between the two junctions was not used to correct the phase of the admittance matrix of *junction 1* (see below for a more complete approach). Furthermore, the measured I-V curve used for design was taken from a wafer with the best results achieved thus far; however, it was not known at the time that the resulting junction sizes were 20–30% smaller from the target due to processing. Nevertheless, the measured data fit the simulation reasonably well and a new mask set was created. An important result of the study demonstrated that the nominal line length between the junctions was previously tuned below the middle of the band, and the length was reduced from 12.2 µm to 11.5 µm, with a prediction to shift the frequency response upwards approximately 15 GHz.

A. Design of the Mixer Chip

Of the chips with the integrated LO coupler, several options were introduced: 'A' designs were matched for best impedance match to the probe, and 'B' designs were matched with an emphasis to shift the frequency of the nominal design approximately 7% higher. Each design also included a variation of the microstrip line length between the junctions to account for a ±10% deviation in junction capacitance. For example, A1, A2, and A3 designs incorporated a line length of -1, 0, and +1 µm with A1 corresponding to an upwards shift in frequency. Another layout was included in the mask that did not include the LO circuitry, but instead used a single microstrip line as an impedance transformer (referred to here as 'C' design).

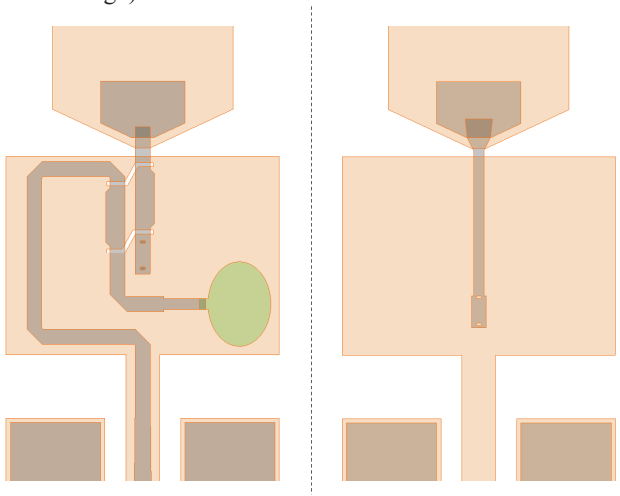

Fig. 6 Close-up of the mixer chip layout for designs 'A' and 'B' (left) that have the integrated LO coupler, and 'C' (right) using a single quarter-wave transformer.

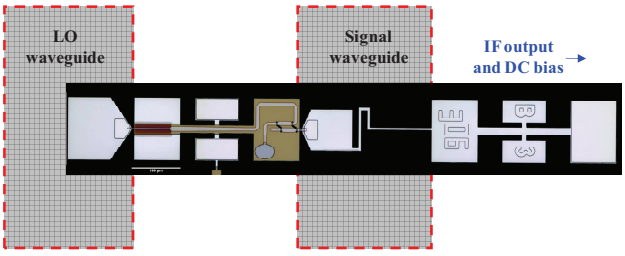

Fig. 7 Photo of the 'B' design incorporating the LO coupler on the chip. The dashed lines indicate the placement of the chip within the LO and RF waveguides of the mixer block.

Fig. 6 to Fig. 9 show the design and simulated results for the key components of the chip design. Two identical chokes are used to isolate the LO and IF from the signal. The signal is coupled through a probe with a high impedance line that serves as a path for both the IF output and DC biasing [9]. A bond-wire from the middle section of the RF probe serves as the DC ground (see discussion below). The LO is coupled through a separate waveguide probe and combined through a hybrid slot microstrip coupler located on the first section of

the RF choke; the coupler also acts as a quarter-wave transformer. Following the transformer is the twin circuit. The termination on the coupler is formed from Nitrogen-doped sputtered Titanium alloy as described in [10]. The surface resistivity is chosen close to that of the coupler port impedance, and a small section of inductive line is used to compensate for its capacitive nature.

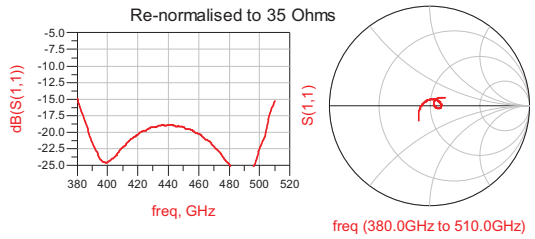

Fig. 8 Simulation of the RF probe with complete choke structure.

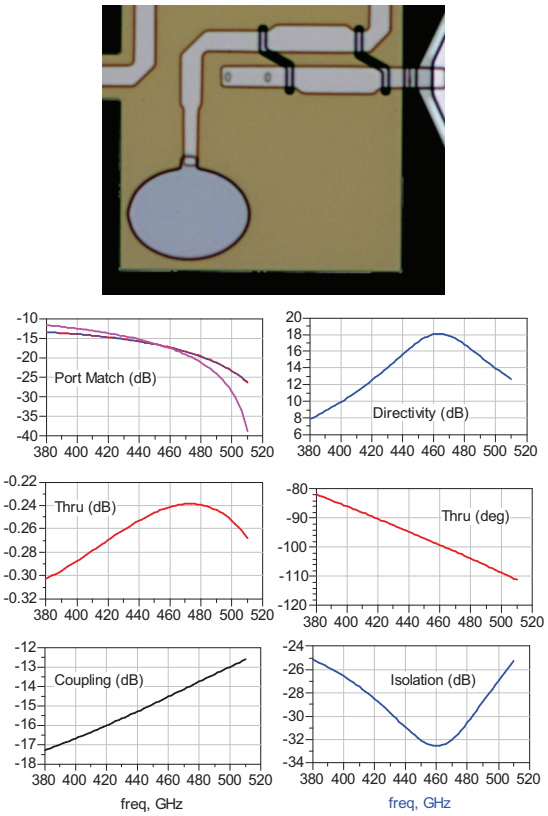

Fig. 9 Simulated response (bottom) and photograph (top) of the integrated LO coupler with resistive termination. The coupler is formed from microstrip, referenced to the first section of the RF choke, and has increased coupling from slots cut into the ground-plane. The twin junctions are shown following the coupler.

B. Measured Results and Discussion

Of those designs with the integrated LO coupler, only the 'A' designs were measured as the 'B' designs were diced slightly wider and would not fit within the mixer channel without modifying the mixer block. Despite the variations of microstrip tuning lengths, these designs continued to show a poor response at high frequency. Considering Fig. 10, it is seen that the A1 designs appear to have a slightly better performance at high frequency, but the result is not conclusive. Note that between the A1 and A2 designs, the nominal resonant point of the twin circuit was set at 460 and 430 GHz respectively.

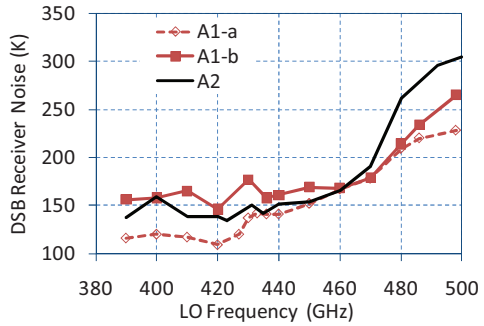

Fig. 10 Measured DSB receiver noise using the 'A' designs.

In an effort to understand the effects of the coupler, design 'C' (without the on-chip LO coupler) was tested using a micro-machined waveguide LO coupler [11]. Fig. 11 shows the substantial improvement in DSB noise when layout 'C' is used with the cold waveguide LO coupler.

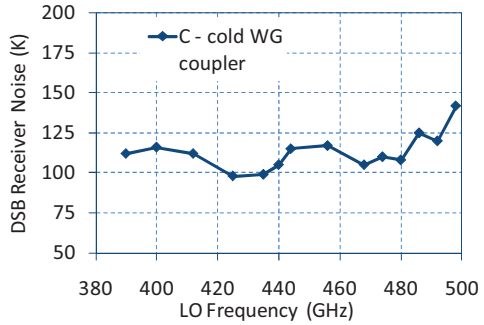

Fig. 11 Measured DSB receiver noise of 'C' chip layout that uses a cold waveguide LO coupler.

While it is not known the exact reason for the degradation with the integrated coupler, the difference in response deserves some discussion. One very important advantage of the 'C' designs is that the bonding location for the DC ground may be moved to the LO end of the RF choke. This is the ideal location to bond as here the choke is most effective in isolating the effects of the bond-wire. With the integrated coupler, bonding cannot occur on the end because of the LO probe and, due to the relatively large diameter of the bond-wire and its added asymmetry, a resonance within the choke may occur, as shown in Fig. 12. From extensive simulation, it was determined that through careful control of the length and placement of the bond-wire, the resonance could be minimized, but, in practice, this is difficult.

The measured effect of the bonding was compared between bonding on the hammer of the choke, as shown in Fig. 12, and bonding on the first section of the choke (i.e., the LO end) and is shown in Fig. 13. A clear degradation is seen due to the bonding location, but it is apparently not the sole

contributor to the troubling performance shown with the integrated coupler.

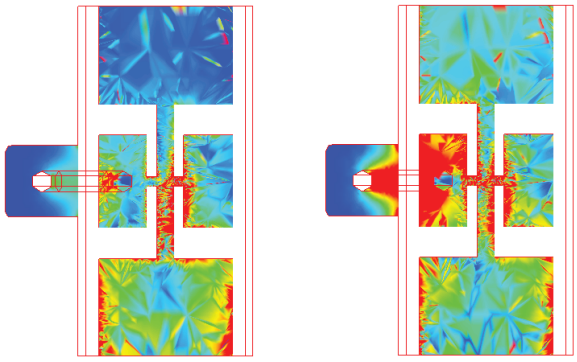

Fig. 12 Simulated surface current along the RF choke (a top view as shown placed in the mixer block channel) with a bond-wire extending from the centre-left hammer of the choke to a point on the mixer block, where the current intensity is indicated using a colour scale ranging from red (strong) to blue (minimal). The left figure shows a frequency where the bond-wire is sufficiently isolated, whereas on the right a resonance involving the bond-wire is shown at a frequency where the performance is severely degraded. The bond-wire has a diameter of 18 µm. An ideal location for the bond-wire is on the upper pad of the choke, where symmetry is preserved and maximum isolation is achieved.

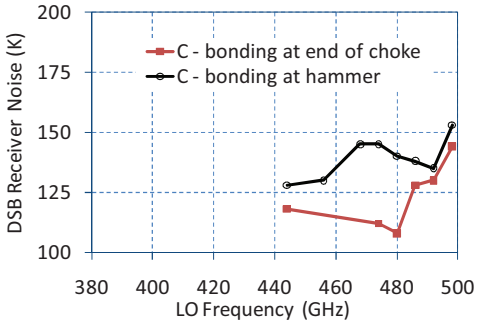

Fig. 13 Effect of bonding when bonded on the hammer as compared to the first section of the choke.

Therefore, it is quite likely that the integrated LO coupler exhibits some unexpected performance. The coupler is very sensitive to processing errors especially with respect to the slot dimensions and alignment. Furthermore, the slot widths at this frequency have a strong effect on the phase and impedance of the coupler, causing a strong slope in the coupling and off-centred input matching (as shown in Fig. 9 and by comparing the physical length of the transformer sections in Fig. 6). Because of increased LO noise coupling at these frequencies, the overall noise is impacted. Finally, there may be another unexpected effect since field lines are not well confined within slot-line modes.

III. Modeling with Agilent ADS

In an effort to improve on the modeling of the SIS twin circuit (in particular to account for the large signal phase distribution between the two junctions) and to analyse the combined response delivered to the IF, the small signal noise and admittance matrices were joined into a complete circuit using Agilent ADS [12] following a methodology similar to that described in [13] for a single junction. It is appropriate to mention here *SuperMix* (an extensive software package that is used by several groups in SIS junction array designs) that uses the theory of [7] in addition to a harmonic balance analysis of the LO [14]. One motivation within this paper is to perform a simplified analysis using a circuit simulator familiar to many designers across the industry.

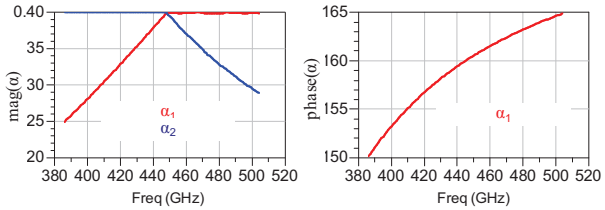

Fig. 14 Large signal pumping magnitude and phase between junctions in the twin circuit. In this case it is assumed that neither the left nor right junction may exceed some maximum pumping level (in this case 0.4).

In this setup, the pumping distribution of the LO was determined in the same manner as described above. It is important to recall that the phase of the down-converted IF signal is a function of the phase difference between the LO and RF signals at each junction. One may assume that this relative phase difference between the LO and RF is the same for each junction in the twin circuit, i.e., both the LO and RF undergo the phase change as illustrated by Fig. 3. Additionally, the spatial separation of the junctions at IF is negligible so that the down-conversions from each junction add in phase. In order for the small signal conversions to add in phase, the small signal admittance matrix of the first junction, YY_1, must be modified according to

$$YY_{1,mn}{}' = YY_{1,mn}e^{j(m-n)\varphi} \qquad (3)$$

where φ is the phase of the LO voltage and m and $n = 0,\pm1,\pm2$ representing each sideband of the 5-port network following [7]. Eq. (3) is identical to that found in [3]. Note that it is not necessary to modify the noise correlation matrix, HH_1, since it is assumed here that the noise between the two junctions is not correlated (this is also stated in [7]).

Following the steps outlined in [13], each junction in the array was first represented as a noiseless 5-port uniquely described by its LO pumping, measured I-V curve, and DC biasing. Instead of fixing the pumping of *junction 2* to some value, it was assumed here that neither junction may exceed some maximum pumping level as shown in Fig. 14.

The small signal analysis was then set up by the following steps. The "noiseless" admittance matrix of each junction was combined with noise current sources at each sideband port, shown in Fig. 15, with magnitudes equal to

$$I_{Noise,m} = \sqrt{HH_{mm}} \qquad (4)$$

with units of $pA/\sqrt{Hz}$. Using the noise correlation block in ADS, *NoiseCorr*, the noise currents were related according to normalized values

$$h_{mn} = 1/\sqrt{HH_{mm}HH_{nn}} \quad , m \neq n. \qquad (5)$$

To form the twin circuit, the two junctions were attached at each port through a pi-network representing the junction capacitance and inductive microstrip line as seen in Fig. 16.

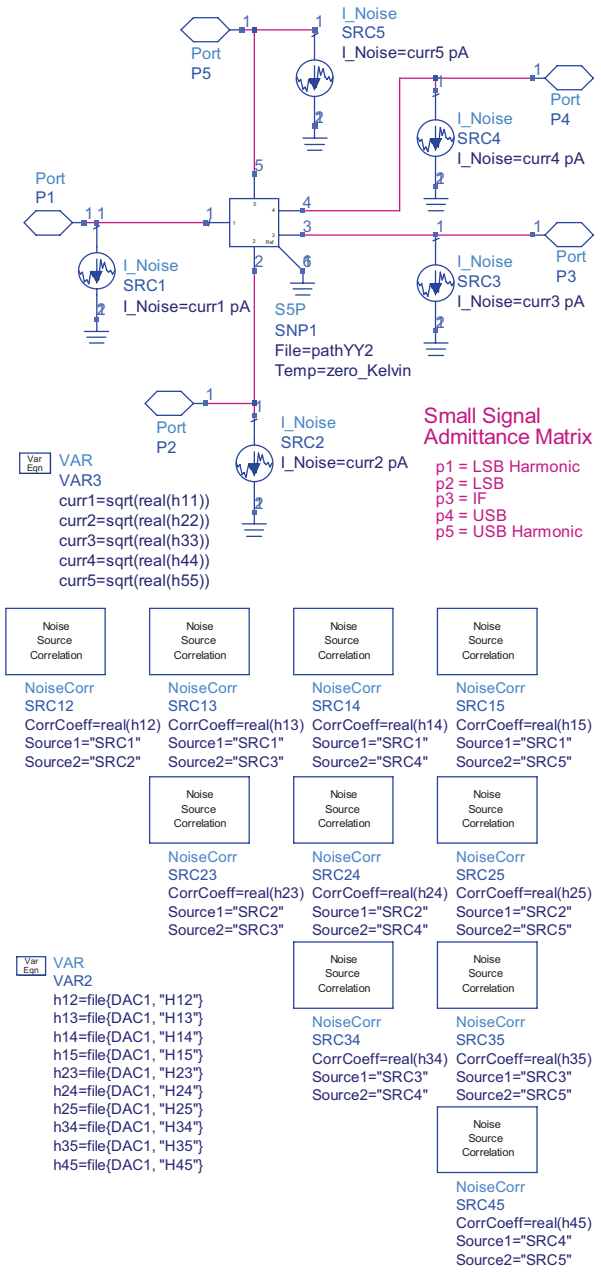

Fig. 15 Network representing each junction of the array in Agilent ADS. Noise currents are combined to the "noiseless" linear 5-port network and correlated using the *NoiseCorr* circuit block.

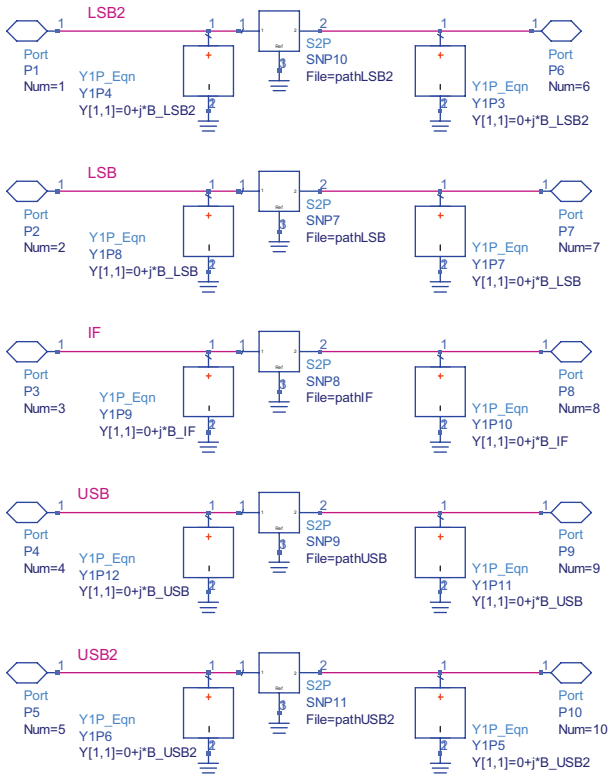

Fig. 16 Network showing the sideband port connections of each junction completing the twin circuit. Each port consists of a pi-network of the junction capacitance, determined by the susceptance calculated at each sideband frequency, along with simulated s-parameters of the inductive microstrip line.

Following the notation in [7], lower-sideband ports and admittances have been conjugated (e.g., susceptances and s-parameters have been conjugated).

The simulation was performed with respect to an LO frequency sweep, so the respective embedding impedances (i.e., probe and transformer) included a frequency offset for each sideband. Fig. 17 shows the completed twin circuit connected to ports containing the respective embedding impedance for each sideband (separately modeled).

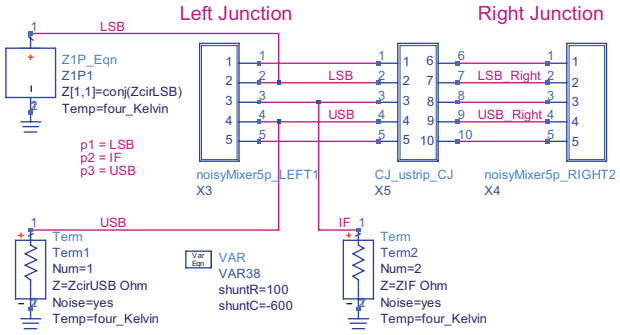

Fig. 17 Full twin mixer chip simulation showing the twin circuit connection terminated with the respective sideband impedances that contain the surrounding circuitry (e.g., the probe and transformer).

C. Comparison of Simulated and Measured Results

Following the earlier discussion above, it is appropriate to compare the measured performance with the simulation for the 'C' layout. Note that the small signal matrices have been calculated from a measured I-V curve typical of the wafer (see Fig. 5) using a 2.2 mV DC bias (the complex LO tunneling current is close to purely real at this point). It is assumed that $R_N A = 20\ \Omega\ \mu m^2$ for the wafer resulting in a junction capacitance of 300 *fF* from junction areas of 3.0 μm^2 (these were the targeted design values verified by dip testing of the wafer). As an initial (though not complete) validation step, the IF port was short-circuited; this causes the input RF admittance of each junction to appear close to a shunt resistance value of R_N. Fig. 18 shows a nice agreement with this assertion.

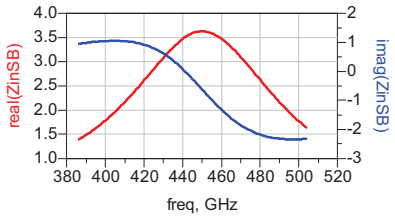

Fig. 18 Input impedance at the upper-sideband, *ZinSB*, when the IF port is short-circuited using layout 'C'. The result closely matches that of the twin circuit if each junction is represented as a pure shunt resistance equal to R_N.

An interesting result of the simulation shows that this particular circuit appears to have high gain with moderate pumping values over the lower half of the band. Furthermore, at the higher edge of the band, conversion gain drops off and is not improved with increased LO pumping. When comparing with the measured results, the pumping should be reduced to stable levels (i.e., no generation of reflected power and negative conversion gain). Under these conditions, one can see a reasonable resemblance between the measured and simulated values when compared with Fig. 11 above. The DSB system noise has been modeled as:

$$T_{sys,DSB} = \frac{T_e}{2} + \frac{hf_{LO}}{k} + \frac{T_{IF}}{|S(2,1)|} \qquad (6)$$

where T_e is the equivalent noise single-sideband noise temperature of the circuit, T_{IF} is the noise of the IF chain (taken to be 10 K), and S is the s-parameter matrix between the ports as illustrated in Fig. 17.

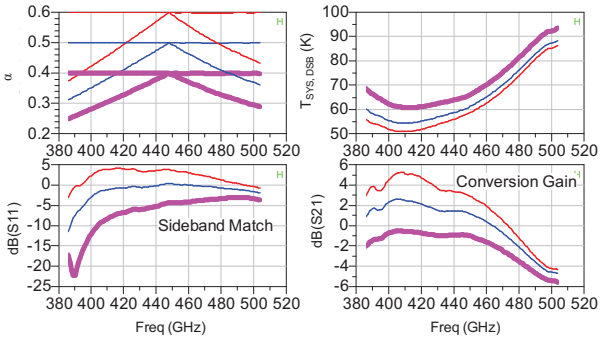

Fig. 19 Simulated results of the full mixer chip for the 'C' layout showing the dependence on LO pumping magnitude, where maximum α = 0.6 (red), 0.5 (blue), and 0.4 (pink).

Fig. 20 indicates the noise dependence on the tuning length of the microstrip line between junctions. It is interesting to see that centred noise performance does not exactly correspond with resonating out the junction capacitances at the mid point of the band. This finding appears to be corroborated independently in [2] who found it was necessary to reduce the microstrip line length by 15%.

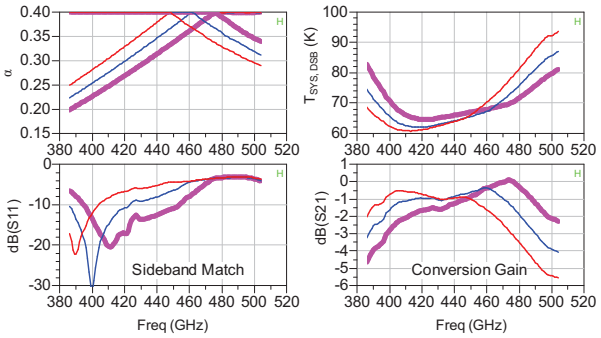

Fig. 20 Variation of the length of microstrip line between the junctions where the length is given as 11.5 (red), 11.0 (blue), and 10.5 (pink) µm. The noise performance of the twin circuit becomes centred as the resonance point is shifted towards the upper portion of the band.

IV. Conclusions

An overview of the design, measurement, and modeling of the APEX band 3 mixer chip (385–500 GHz) has been presented. It was found that the integrated coupler contributed to poor performance at higher frequency and, while the precise cause is unknown, it is speculated that it is due to the size of slots for this frequency range, or that the slots in the ground plane enhance vortex penetration in the ground Nb layer of the mixer circuitry which causes an increasing RF loss as the LO frequency rises (approaching 70% of the Nb gap frequency).

Version 'C' of the mixer has been installed at the APEX telescope ([15]), during March 2010, as the third receiver channel of the Swedish Heterodyne Facility Instrument ([16]).

A methodology for simulating SIS junction arrays with Agilent ADS has been presented and applied to the twin junction design. It is shown that the twin junction circuit is sensitive to LO pumping levels, and that for a centred noise performance across the band, the resonance point of the junction capacitance should be offset towards the upper part of the band.

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