Design of a High-Power 1.6 THz Schottky Tripler Using 'On-chip' Power-Combining and Silicon Micromachining

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***Abstract*— In this work, we present a novel concept for power-combined high-power frequency multipliers consisting of four multiplying structures integrated on a single-chip with the input and output waveguides perpendicular to the waveguide channels, where the diodes are located, by using silicon micromaching techniques. The input power is equally divided in-phase by four E-probes located at the input waveguide. The produced output power is recombined at the output using the same concept. A 1.6 THz tripler has been designed using this architecture. The expected conversion efficiency of the tripler is ~ 2-3 % efficiency over a ~ 20 % bandwidth for a 32 mW of total input pump power.**

***Index Terms*—Terahertz technology, frequency multipliers, local oscillator sources, Schottky diodes, power-combining, silicon micromachining.**

I. Introduction

The availability of increasing output power at W-band together with the use of power-combining schemes and high-thermal conductivity substrates have led to record measured output power of terahertz sources in recent years. Recently, 1.4 mW of output power at 0.9 THz with two cascaded Schottky based frequency triplers driven with a 400-500 mW W-band HEMT power module has been reported [1]. Moreover, power levels up to 10 mW at 600 GHz and 0.1 mW at 1.9 THz are envisioned using this W-band source. The tremendous progress in GaN-based power amplifier technology, with output power levels in excess of 5 W recently demonstrated at W-band, makes it now possible to conceive solid-state multiplied sources beyond 3 THz [2], as well as to develop multi-pixel heterodyne instruments for ground and space based applications in the THz range [3].

In this work, we report on the design of a novel power-combined 1.6 THz Schottky frequency tripler intended to handle around a 30 mW input power to produce ~1 mW at 1.6 THz. The design of Schottky based triplers at these frequency ranges is mainly constrained by the shrinkage of the waveguide dimensions with frequency and the minimum diode mesa sizes, which limits to two the maximum number of diodes per chip. Hence, multiple chip power-combined schemes become necessary to increase the power-handling capabilities of high frequency multipliers. However, the use of traditional power-combining topologies already demonstrated at frequencies below 1 THz [1, 4] presents several challenges for frequencies beyond 1 THz. On the one hand, the use of several Y-junctions or hybrid couplers to divide/combine the input/output power at these frequency bands increases unnecessarily the electrical path of the signal at a range of frequencies where the waveguide losses are considerably high. On the other hand, guarantying a perfect alignment of the very small chips during assembly in order to preserve the balanced nature of the multiplier is practically impossible, with the subsequent impact on the multiplier performance. The novel concept presented herein (see Fig. 1) overcomes these difficulties by performing the power-combining directly 'on-chip' instead of using 4 different chips. Four E-probes are located at a single input waveguide in order to drive 4 multiplying structures (with 2 diodes each). The produced output power is then recombined at the output using the same concept. The four multiplying structures are physically connected on one-chip so the alignment and symmetry of the circuits can be very well preserved since that is controlled by the high accuracy of MMIC lithography. Contrarily to traditional frequency triplers, in this design the input and output waveguides are perpendicular to the waveguide channels where the diodes are located. Therefore, the multiplier block can be more easily fabricated using Silicon micro-machining technology [5] instead of regular metal machining.

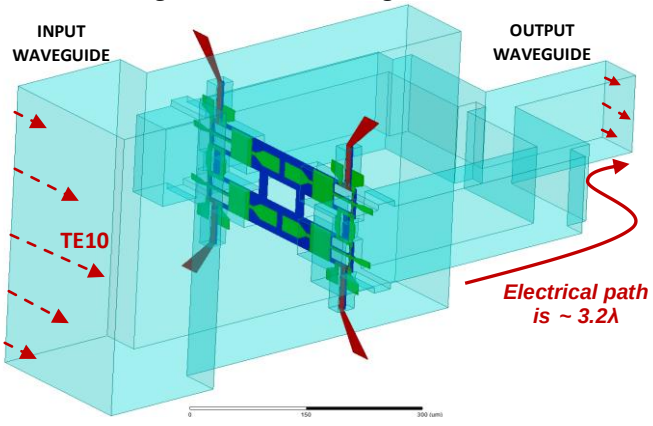

Fig. 1. 'On-chip' power combining scheme for frequency multipliers.

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II. DESCRIPTION OF THE ON-CHIP POWER COMBINED FREQUENCY TRIPLER TOPOLOGY

Based on the frequency multiplier topology described in [1,6], this novel concept exploits the 3D capabilities of the Silicon micromachining techniques in order to place the MMIC multiplier chip perpendicular to the E-plane of both the input and output waveguides. With this strategy, four identical E-probes can be used in-phase with the electric field lines of the exciting TE_{10} mode to equally divide the input signal into four ways directly on-chip as can be seen in Fig. 2. The same concept is applied to recombine the power at the output. This prevents the need of using waveguide-based power dividing structures that would add undesired excess losses to the circuit. In addition, the balance and symmetry of the circuit with this new approach, which is crucial to obtain a good performance in any power-combined frequency multiplier at terahertz frequencies [4, 7], lies on the superior accuracy of the lithographic fabrication of the MMIC chip and Silicon micro-machined blocks (<1 μm) rather than on the tolerances involved with manual assembly and traditional metal milling (5-10 μm). This could represent a big step for future multipliers operating beyond 1 THz where dimensions of critical elements of the device can be as low as 10-20 um between 1-2 THz, and 5-10 um beyond 2 THz.

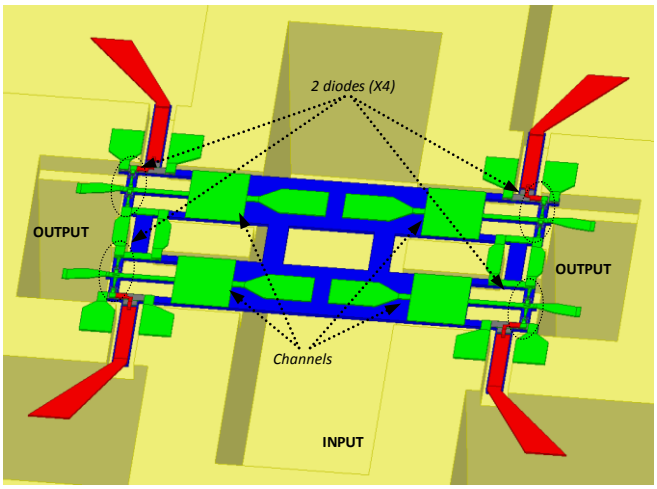

Fig. 2. Close-up view of the 1.6 THz on-chip power-combined MMIC device. Four beamleads (in red) provide independent bias to each diode branch. If fine tuning of the tripler performance is not required, only a single bias line would be necessary.

Note that this topology inherently provides two independent outputs that can be either combined together using a Y-junction, as shown in Fig. 1) or used to feed two independent frequency mixers in order to enable direct multi-pixel operation.

III. 1.6 THz TRIPLER DESIGN

The complete power-combined tripler was designed using the methodology presented in detail in [2], which is based on an iterative process that involves the use of Ansoft HFSS for the electromagnetic simulation of the multiplier architecture and Agilent ADS for nonlinear simulation of the Schottky diode device and the harmonic balance optimization of the matching circuitry.

Once the input power has been split at the input probe level, the topology in Fig. 2 can be seen as four identical frequency triplers located at four independent small waveguide channels between the input and output waveguides. Each of these multiplying structures features two Schottky planar varactor diodes of approximately 1.2 fF of zero bias junction capacitance and has several stripline sections of low and high impedance used to match the diodes at the input and output frequencies and to prevent the third harmonic from leaking into the input waveguide. In order to balance the circuit, the dimensions of both the channel and the circuit are chosen to cut off the TE-mode at the second (idler) frequency. The dimensions of the output waveguide ensure that the first and second harmonics are cut off at the output, and the balanced configuration of the diodes ensures that the power levels from all the even harmonics of the input signal are strongly suppressed. The design is completed with a series of waveguide sections to provide broadband input matching to the diodes.

The predicted performance of the on-chip power combined frequency tripler for a 32 mW input power is presented in Fig. 3. A conversion efficiency of ~ 2-3 % is expected over a ~ 20 % bandwidth.

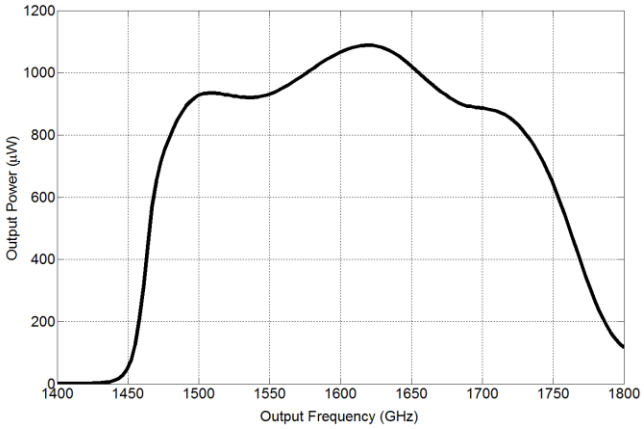

Fig. 3. Predicted performance of the on-chip power combined 1.6 THz frequency tripler for an input power of 32 mW.

IV. COMPARISON BETWEEN ON-CHIP POWER COMBINING AND TRADITIONAL QUAD-CHIP POWER COMBINING

In order to evaluate the advantages of the proposed multiplier scheme over other power-combining techniques, an equivalent quad-chip frequency tripler has been designed following the same specifications and identical number of diodes an anode sizes. In this case, two levels of Y-junctions at the input and output waveguides have been employed to divide/combine the input/output signals. The scheme is similar to that proposed in [7]. The main constraint for this quad-chip design is the necessity to use at least two dc bias feed through. This sets a minimum distance between the multiplier chips and leads to an undesired increase in the electrical path of the output signal (17 wavelengths) as can be seen in Fig. 4. However, for the on-chip power-combined topology, the complexity of the bias circuitry is greatly reduced since it can be placed on a plane perpendicular to the input and output waveguides. The electrical path is then around 3 wavelength (see Fig. 1), which implies a reduction of more than a factor of 5 in the output waveguide losses.

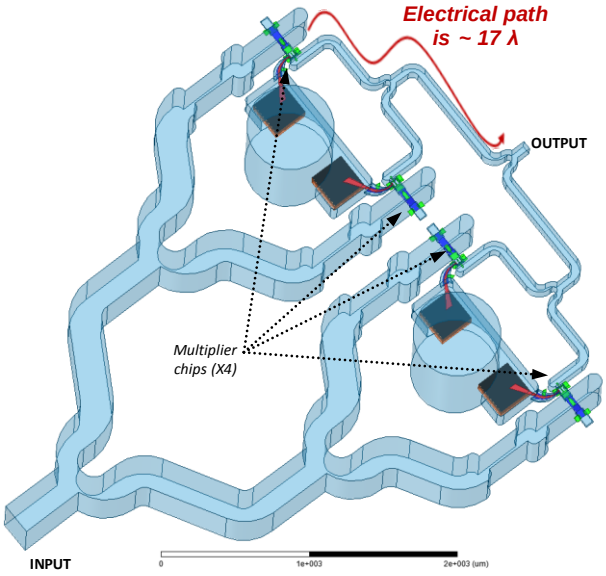

Fig. 4. Quad-chip power-combined 1.6 THz Schottky diode tripler.

The comparison between the two architectures are plotted in Fig. 5, together with the simulated performance of a single-chip 1.6 THz tripler designed for 8 mW, one fourth of the input power of the power-combined multiplier. This single chip corresponds to one of the branches shown in Fig. 4. It can be clearly seen the degradation in the conversion efficiency of the quad-chip tripler mainly due to the waveguide losses connected with the necessity of using a number of Y-junctions to power-combine the input and output signals (red dashed line). However, the on-chip power-combined tripler (black solid line) exhibits an efficiency very close to the single-chip multiplier design (dashed blue curve), which would set the reference for an ideal power-combined multiplier. Only the bandwidth is slightly reduced due to the fact of having kept the same dimensions for the reduced-height input waveguide in all the three cases, which made it necessary to reduce the lengths of the four E-probes so they could still fit together within the input waveguide. A better optimization of both the E-probes and the input waveguide dimensions in the on-chip power combined tripler would allow recovering the lost bandwidth with regards to the single-chip tripler.

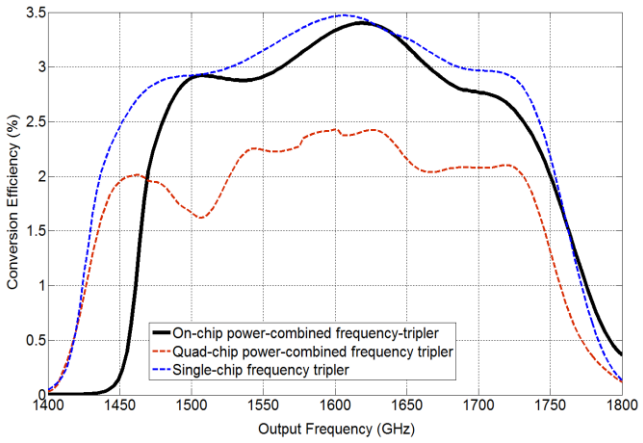

Fig. 5. Conversion efficiency of the single-chip, quad-chip power-combined, and on-chip power-combined 1.6 THz Schottky diode triplers.

V. Silicon-Micromachined Block Design

As already mentioned, the block design is based on the 3D integration of Silicon micromachined waveguide circuits. The concept is similar to tradition split-waveguide block designs but a number of very thin Silicon wafers are stuck together in order to define both the waveguide channels were the diodes are located and the input and output matching sections. Eight 245 um-thick Silicon wafers needs to be employed to fit the matching sections, the waveguide channel where the chip is placed, and the Y-junction to recombine the signal at the output. Wafer to wafer alignment is performed using Silicon alignment pins of diameters between 0.5 and 1 mm. The length and width of the Silicon wafers (20 x 20 mm) are chosen to coincide with the standard metal block dimensions used in our laboratory at JPL. The total thickness of the block is 1.96 mm, which represents a reduction of 5-10 times with regards to the metal block dimensions that would be necessary for a traditional split-waveguide metal block design, like the structure presented in Fig. 4.

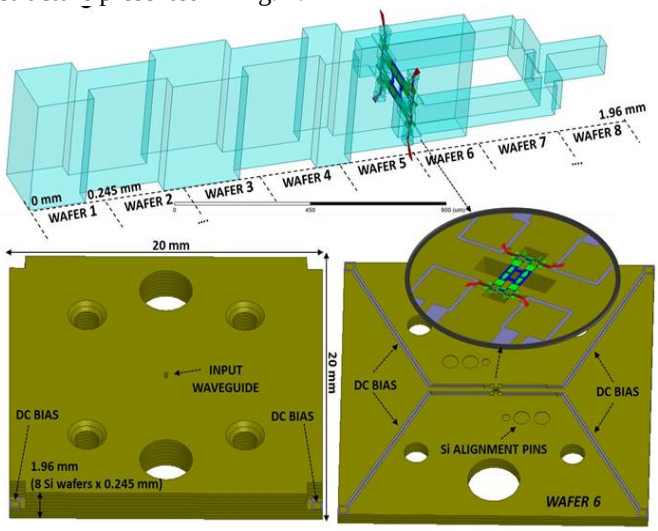

Fig. 6. Final scheme of the on-chip power combined 1.5 THz Schottky tripler includind the input matching and output Y-junction (top). Block design for Silicon micromachining featuring eight 0.245 mm-thick Silicon wafers (bottom left). Detailed view of the Silicon wafer where the chips is located (bottom right). The full block dimensions are 20x20x1.96 mm.

VI. Conclusion

The novel on-chip power-combining topology for high-frequency multiplier design presented herein allows the power handling capabilities of traditional frequency multipliers by a factor of four.. The advantage of this approach with regard to other power-combining techniques involving multiple chips is that additional losses or performance degradation due to circuit imbalances are avoided. The topology is presented through the design of a 1.6 THz frequency tripler for a nominal input power of 32 mW. The use of Silicon micromachining instead of metal milling also makes it possible to considerably reduce the mass and volume of the multipliers.

The final goal of this work is to develop high-power all-solid state terahertz local oscillator sources to enable multi-pixel spectroscopy at 1.9 THz and 2.7 THz and to extend the use of Schottky technology up to 4.7 THz.

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