"32-channel Multi-Chip-Module" The Cryogenic Readout System for Submillimeter/Terahertz Cameras

Yasunori Hibi, Hiroshi Matsuo, Taishi Ookawa, Hirohisa Nagata, Hirokazu Ikeda, and Mikio Fujiwara

Abstract— **We have been investigating the submillimeter/ terahertz camera with the large format SIS (Superconductor - Insulator - Superconductor) photon detector array. To realize the submillimeter/terahertz camera, a cryogenic readout system matching to the SIS detector properties is necessary.**

For this readout system, we have developed several kind of ICs (Integrated Circuits) constructed with n-channel GaAs-JFETs. We also have designed and manufactured 32-channel multi-chip-modules with these ICs. These modules can make 32-channel parallel input photo current signals into one or two serial output voltage signal(s). Size of these is 40mm x 30mm x 2mm. The estimated total power dissipation is about 400 μW.

Index Terms—**Application specific integrated circuits, Cryogenics, Gallium arsenide JFETs, Image sensors, Multichip modules,**

I. Introduction

OBSERVATIONAL astronomers desire to obtain submillimeter/terahertz astronomical observational data comparable to other wavelength/frequency data. To response these desires, developments of various high sensitivity submillimeter/terahertz cameras with many superconductive detector pixels are advancing. In these cameras, trans-edge sensor (TES) bolometers [1], kinetic inductance detectors (KIDs) [2], and superconducting tunnel junction (STJ) detectors [3]-[5] are employed. These superconductive detectors are used in deep cryogenic temperature. Therefore, to realize high performance submillimeter/terahertz cameras with such detectors, the multi-channel readout system workable in cryogenic temperature are required.

Since TES detectors and KIDs detectors are low impedance type detectors, the cryogenic readout system for these detectors must be suitable for low impedance type detectors. Therefore, those readout systems constructed by low input impedance devices such as superconducting quantum interference devices (SQUIDs) or high frequency amplifiers with high electron mobility transistors (HEMTs) have been developed. On the other hand, STJ detectors are relatively high impedance type detectors, the cryogenic readout system for STJ detectors must be suitable for high impedance type detectors.

We planned a cryogenic multi-channel readout system referred to the CMOS camera readout system; one of the room temperature readout system for high impedance type detectors [6]-[9]. To realize this cryogenic readout system, we have developed and investigated some functional cryogenic integrated circuits (ICs) constructed with n-channel GaAs JFETs [10]-[12].

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II. The N-channel GaAs JFETs Cryogenic Performances

As reported in Fujiwara, Sasaki, and Akiba 2002 [13], the n-type GaAs JFETs offer good cryogenic performance. At 4.2K, they show good statistic characteristics even their power dissipation below 1 μW. Typical cryogenic characteristics are shown in Fig. 1. Furthermore, GaAs JFETs are also can easily work even at 0.3K [14]. Especially about input referred voltage noise, the value is around 3 $\mu V_{rms}/Hz^{0.5}$@1Hz and this value can be suppressed by thermal cure [15] or infrared irradiation [16]. Except performances of these, the gate capacitance which a gate width of 5 μm and a gate length of 100 μm is smaller than 50 fF and the EFET OFF resistance which a gate width of 5 μm width and a gate length of 5 μm is larger than 100 TΩ [12]. These facts indicate that GaAs JFETs are very suitable for electric switches. In addition, Fujiwara and Sasaki 2004 [15] showed that the FET gate leakage current of these devices is 10^{-18} A or smaller. This suggests that GaAs JFETs may be excellent choice to be combined with high impedance detectors such as STJ detectors. However, p-type GaAs JFETs do not exist commercially, so extra care must be taken when designing the circuits.

III. The GaAs JFETs Integrated Circuits

A. 16-Channel AC-coupled CTIAs

The capacitive trans-impedance amplifier (CTIA) transforms input current signal into low impedance voltage signal. The circuit concept of the AC-coupled CTIA is shown in Fig. 2 a). The reason of taking the "AC-coupled"

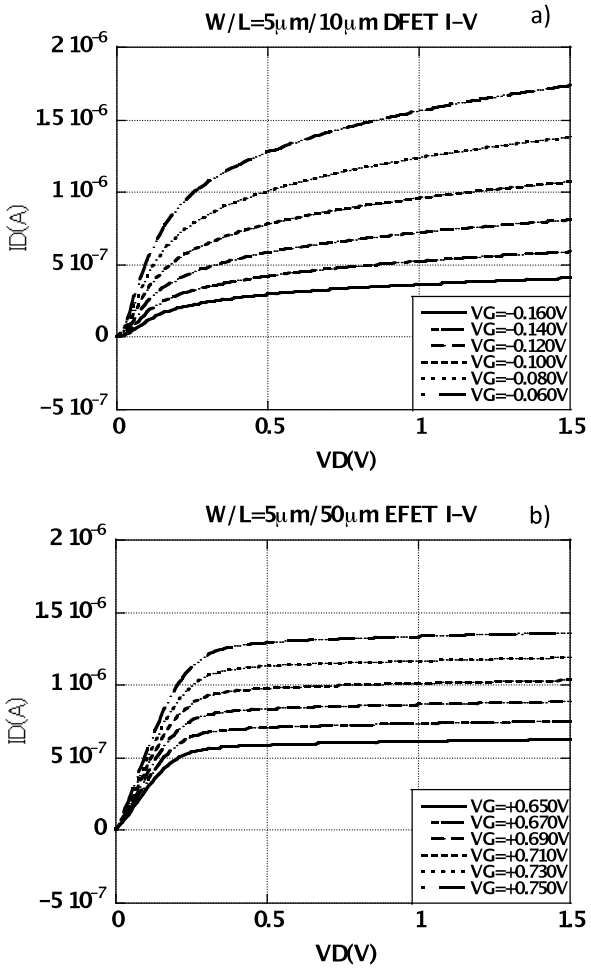

Fig. 1. Typical cryogenic (4.2 K) "ID-VDs" of the GaAs-JFETs when VS=0V. The gate size of a) is width of 5 μm and length of 10 μm. And a) is depletion type (when VG=0V, ID≠0A) FET. The gate size of b) is width of 5 μm and length of 50 μm. And b) is enhancement type (when VG=0V, ID=0A) FET.

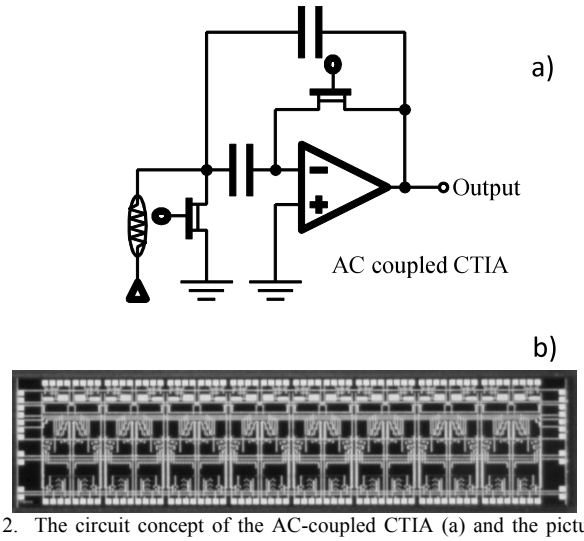

Fig. 2. The circuit concept of the AC-coupled CTIA (a) and the picture of 16-ch AC-coupled CTIAs IC (b).

mechanism is to suppress input offset voltage distribution when many amplifiers are integrated.

From our previous developments, we got 16-channel AC-coupled CTIAs. The power dissipation of this IC is about 50 μW and input offset voltage distribution is lower than 3 mVp-p. Fig. 2b) shows a picture of 16-ch AC-coupled CTIA. The physical chip size is 2 mm x 8 mm x 0.2 mm.

B. 32:1 Multiplexer with Sample-and-Holds

A multiplexer transforms parallel signals into serial signal. By combining sample-and-holds with the multiplexer, data sampling timings and data output timings can be settled voluntarily. A part of circuit diagram of the multiplexer with sample-and-holds is shown in Fig. 3 a).

We have developed 32:1 multiplexers with sample-and-holds and show this IC in Fig. 3 b). The power dissipation of this IC is about 30 μW. The physical chip size is 2 mm x 8 mm x 0.2 mm, too.

C. 32-Channel Shift Register

A shift register is one of the simple digital memory circuits. We have developed the cryogenic shift register for generating multiplex timings. The circuit diagram of the flip-flop, which is one unit of the shift register, is shown in Fig. 4 a).

There are D (depletion)-type and E (enhancement)-type FETs in the n-type GaAs JFET. Then, one of the simplest digital logic circuit called DCFL (Direct Coupled FET Logic) is able to be realized by GaAs JFETs [19]. By combining such basic logic circuits, we designed and investigated a master-slave type shift register. We have developed 32-channel shift registers and show this IC in Fig. 4 b). The physical chip size is also 2 mm x 8 mm x 0.2 mm. The design power dissipation of this IC was 16 μW and the real power dissipation is larger than 80 μW. This is because that device parameter selection is too conservative.

D. 32-Channel Voltage Distributer

The voltage distributer can distribute differential level voltage signals to each output terminal. Our aim to use the cryogenic voltage distributers is to keep each AC-coupled

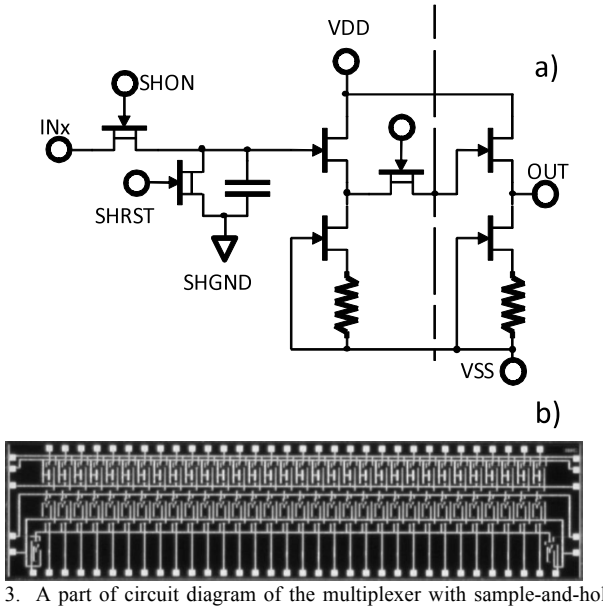

Fig. 3. A part of circuit diagram of the multiplexer with sample-and-holds (a) and the picture of 32:1 multiplexer with sample-and-holds IC (b).

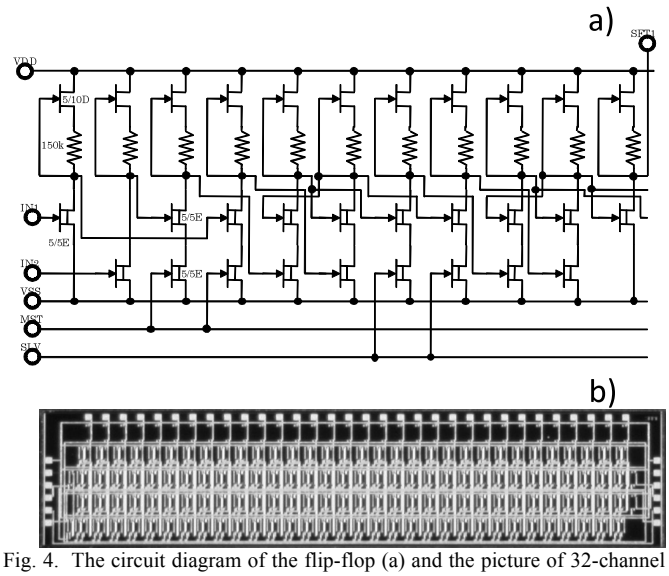

Fig. 4. The circuit diagram of the flip-flop (a) and the picture of 32-channel shift register IC (b). "5/10D" means it is depletion type JFET which gate size is width of 5 μm and a gate length of 10 μm. And "5/5E" means it is enhancement type JFET which gate size is width of 5 μm and a gate length of 5 μm.

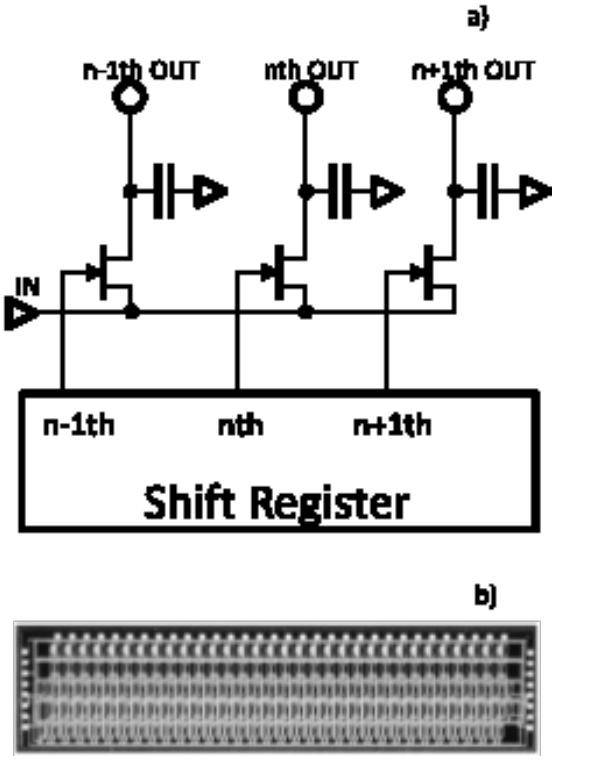

Fig. 5. The circuit concept of the voltage distributer (a) and the picture of 32-channel voltage distributer IC (b).

CTIAs in optimal operating conditions. The circuit concept of the voltage distributer is shown in Fig. 5 a).

We have designed and investigated the 32-channel voltage distributer constructing from the 32-channel shift register and sample-and-holds. We show this IC in Fig. 5 b). The physical chip size is same as previous three ICs. The total power dissipation is about 30 μW.

IV. Cryogenic Readout System

A. Design Concept

We show the concept of the cryogenic multi-channel readout system in Fig. 6. We referred the multi-channel readout system of the CMOS camera and designed this cryogenic readout system. Operational outline of this system is following. Firstly, parallel input current signals are exchanged to parallel voltage signals by AC-coupled CTIAs. Secondly, the parallel voltage signals are sampled and held by sample-and-holds. Thirdly, the held parallel signals are transformed serial voltage signal by multiplexer operated by shift-register. The unique point of this system is the following. By including shift registers in this cryogenic system, the number of digital addressing lines from warm electronics is reduced. And by inserting two multiplexers operated by shift-registers, the operational dead time can be minimized.

B. The 32-ChannelMultitip Module

Based on above concept, we designed and manufactured a 32-channel multi-chip module. This module can transform 32-channel parallel input current signal to 2-channel serial output voltage signals. We show the photograph of this in Fig. 7. This module is made of low temperature co-fired ceramics (LTCC) with 4 wiring layers and 2 ground layers. The size of this module is 40 mm x 30 mm x 2 mm. The estimated total power dissipation of this is around 400 μW.

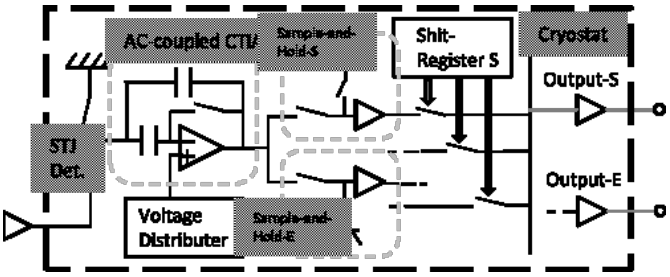

Fig. 6. Schematic of the cryogenic multi-channel readout system. This system has 2 sample-and-holds per 1 AC-coupled CTIA.

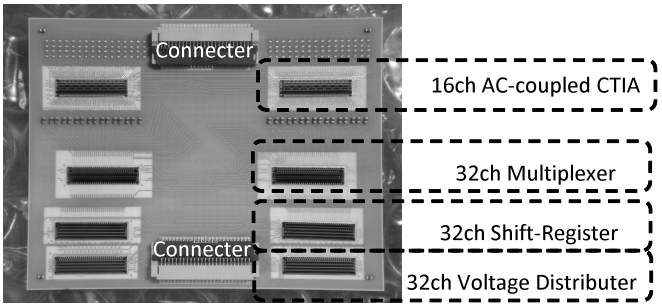

Fig. 7. The picture of the 32-ch cryogenic multichip module. 32-channel parallel input current signals input from upward connecter. Output serial voltage signal, supply sources, and digital signals input from downward.

V. Cryogenic Test Environments

As shown in Fig. 8 a), we set the multi-chip module into wet type cryostat. For signal input and output, we designed a flexible printed circuit (FPC) with 50 lines. This FPC is shown in Fig. 8 b). The DC power source of this module is generated and supplied by the exclusive room temperature electronics shown in Fig. 8c). And the digital signals for the module operation are generated by the other device and supplied through the electronics. In this test, we used 910 kΩ metal film resistances for dummy detectors.

VI. Summary

For realization of a multi-pixel sub-millimeter/terahertz camera, we have developed the multi-channel cryogenic readout system. N-channel GaAs-JFETs offer good cryogenic performances. In particular, the gate leakage current of these JFETs at cryogenic temperatures are extremely low ($<10^{-18}$A). This property makes the devices attractive for use with high-impedance cryogenic sub-millimeter/terahertz detectors. Therefore, we have designed and investigated several kinds of cryogenic circuits with GaAs-JFETs: AC-coupled CTIAs, shift registers, multiplexers with sample-and-holds, and voltage distributers. For connecting these circuits, we designed and manufactured the 32-channel multichip module. And we have prepared test devices for cryogenic test of the modules. Just now, we start investigating the 32-channel multichip modules for the submillimeter/terahertz cameras.

Acknowledgment

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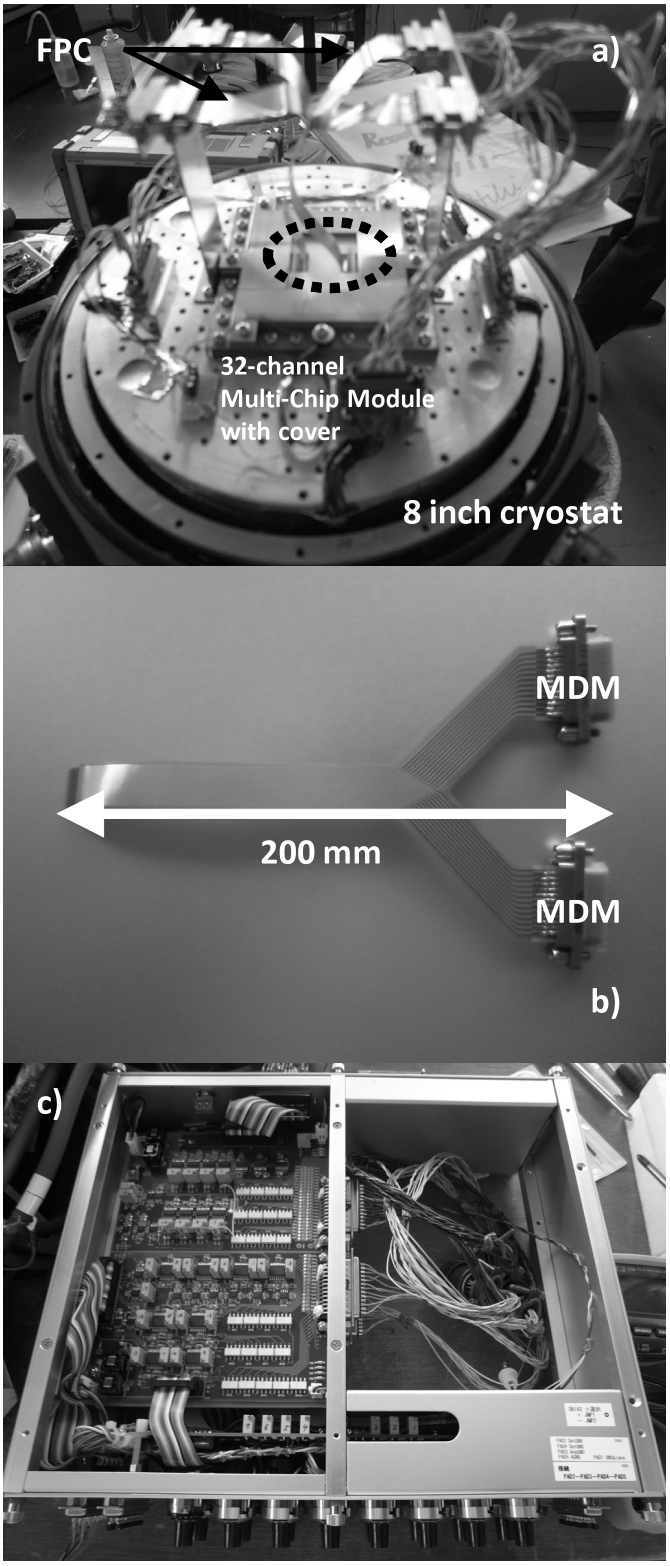

Fig. 8. Photographs of measurement environments. a) Inside of the wet type cryostat. b) FPC itself. c) The exclusive room temperature electronics.

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