Performance of a 700 GHz Unilateral Finline SIS Mixer

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***Abstract*—We present a novel design and the measured performance for a superconductor-insulator-superconductor (SIS) mixer, operating near the superconducting gap of niobium (Nb), in the frequency range of 600–700 GHz.**

A key feature of the mixer design is the employment of a unilateral finline taper to provide smooth transition from the high-impedance waveguide mode to the low-impedance of planar circuits suitable for the operation of SIS tunnel junction. This geometry of the transition can be electromagnetically modelled and optimised to give a short mixer chip with wide RF bandwidth. The finline taper and all the superconducting transmission lines are integrated on-chip and deposited on a 60 μm thick quartz substrate. This results in an extremely simple mixer block design, comprising a feed horn and a straight waveguide section; no backshort or any mechanical tuning structure is needed.

In this paper, we describe the design of the mixer chip, including full electromagnetic simulations of the passive circuits, combined with the heterodyne mixer gain and noise temperature predictions. We have tested the mixer performance from 595 GHz to 702 GHz and measured best receiver noise temperature of 145 K at 600 GHz, corrected for a beam splitter of 75 μm thickness. The need for a thick beam splitter was caused by the lack of sufficient power from the local oscillator (LO) which was optimised between 630–720 GHz and because our mixer was tuned low as a result of larger than designed tunnel junction. Nevertheless, our investigation has demonstrated that superconducting finline mixers work well at high frequencies and have several advantages over other designs, in particular simple mixer block and large substrate for integration of planar circuits.

***Index Terms*—SIS mixers, Submillimeter wave receivers, On-chip integration, Planar circuit**

I. Introduction

We have previously reported the successful operation of antipodal finline SIS mixers at millimetre and submillimetre frequencies [1], [2], [3], [4], [5] with performance comparable to other mixer designs. These mixers have important advantages as a result of fully integrated transmission lines on a large substrate. This yields a simple mixer block design, without a backshort or mechanical tuners, and plenty of space on the substrate for elegant integrating of planar circuits such as sideband separation or balanced designs.

These advantages become particularly attractive at high frequencies, where tolerances on manufacturing high performance mixer blocks becomes stringent. Antipodal finline mixers however, employ a long section of gradually overlapping fins to form the microstrip. Since the overlapping fins are only separated by 400 nm of oxide, the manufacturing of this section is difficult and makes the mixer chip rather long. The mixer chip described in this paper employs an alternative design based on a unilateral finline taper which transforms the waveguide into a slotline. Once the width of the slot becomes small enough to lower the impedance, a transition to a microstrip or coplanar waveguide (CPW) becomes straightforward [6]. As we shall see later, this retains all the advantages of the finline mixer mentioned above, and yet yields a much shorter mixer chip which helps to reduce RF losses and provides many more devices on the wafer. Moreover, the simple geometry enables full wave simulation of the mixer chip and removes the difficulty of fabricating the antipodal section.

The design of the unilateral finline mixer chip has already been reported [7], [8], hence it will only be briefly mentioned in this paper. In particular, we will show how to obtain a good match between the RF source and the device over a large range of frequencies. We will also give detailed reporting of the experimental investigation carried out to study the gain and noise temperature performance of the new mixer. The experimental results will be analysed using the CalTech package *SuperMix* [1] [9], in conjunction with the Ansoft High Frequency Structure Simulator (HFSS).

II. Mixer design

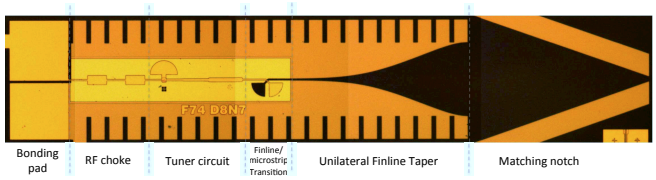


Fig. 1. Overview of a 700 GHz unilateral finline mixer chip with a direct finline-to-microstrip transition on a 60 μm quartz substrate, showing the transition stubs, tuning circuit and the RF choke. The SIS tunnel junction is located at the microstrip below the half-moon stub.

The concept of the unilateral mixer chip design is shown in Fig. 1. It comprises a triangular matching notch in the

[1]A quantum mixing software package written by a Caltech research group to study the behaviour of SIS mixers.

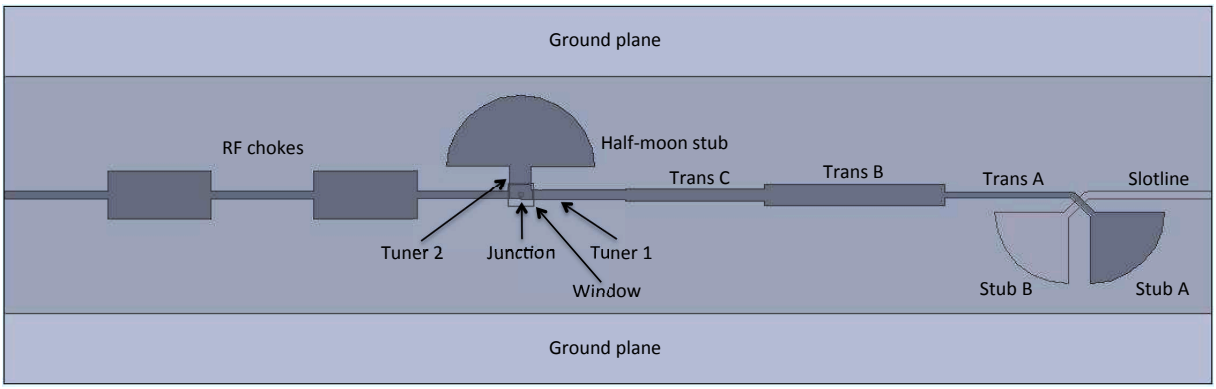


Fig. 2. Enlarged drawing of the planar circuitry consisting the slotline-to-microstrip transition, tuning circuit and the RF chokes.

substrate, a unilateral finline taper, a finline-to-microstrip transition, a tuning circuit, a four-sections RF choke and two IF bonding pads. Our mixers are designed to work with a circular Nb/AlO$_x$/Nb SIS tunnel junction with an area of 1 $\mu\mathrm{m}^2$. This corresponds to a normal resistance of approximately 20 Ω and junction capacitance of 75 fF. The Nb ground plane film (250 nm thick) which form the finline is separated from the Nb wiring film (400 nm thick) forming the microstrip by a 475 nm silicon monoxide (SiO) insulating layer. The entire structure is deposited on one side of a 60 μm quartz substrate.

The finline taper transforms RF power from the waveguide mode into a slotline over a wide RF bandwidth. The profile of the taper is carefully calculated to obtain the shortest possible taper without limiting the bandwidth [10]. The final design is checked with Ansoft HFSS for a full 3-D electromagnetic simulation, including the effect of superconductivity surface impedance. The impedance of the loaded waveguide is matched to the free space via a simple triangular quarter-wavelength notch, which turns out to be sufficient for quartz substrates. For substrates with higher dielectric constant, multiple notch transformers should be used. The slotline width needs to be tapered to approximately 2.5 μm in order to reduce the characteristic impedance to the values suitable for CPW or microstrip ($\sim$20–30 Ω).

The transition from the slotline to microstrip is realised through direct coupling of power across the dielectric layer, as shown in Fig. 2. Both the slotline and the microstrip are connected to 90° radial stubs, each has a radius of approximately $\lambda_g/4$. At the crossing plane, the slotline radial stub appears as an open-circuit, whilst the microstrip radial stub appears as a short-circuit. This combination forces the RF signal to propagate from the slotline to the microstrip with minimum mismatch losses. This direct transition also has all the different layers clearly separated, avoiding potential shorting during fabrication.

The mixer planar transmission lines include 4 components: two inductive strips, a multi-section transformer and an RF choke. The two inductive strips, one in series to the junction and one in parallel, are used to tune out the junction capacitance at two slightly different frequencies. This provides two deep dips in the return loss (see Fig. 3) around the centre frequency in the matching diagram and thus broadens the RF bandwidth [7], [8]. The multi-section transformer is used to match the impedance of this sub-circuit to the output of the slotline-to-microstrip transition. Finally, an RF choke is placed after the tunnel junction to prevent RF signal from leaking into the IF path.

The various components used in our mixer design were optimised using the Ansoft Designer and HFSS. The profile of the finline taper was calculated using our own software, *FinSynth* [10], which synthesises and analyses the tapers using the Optimum Taper Method (OTM). To verify the heterodyne mixing performance of the designed mixer, we exported the scattering matrix of the various components optimised by HFSS into *SuperMix* to construct a full rigorous mixer model.

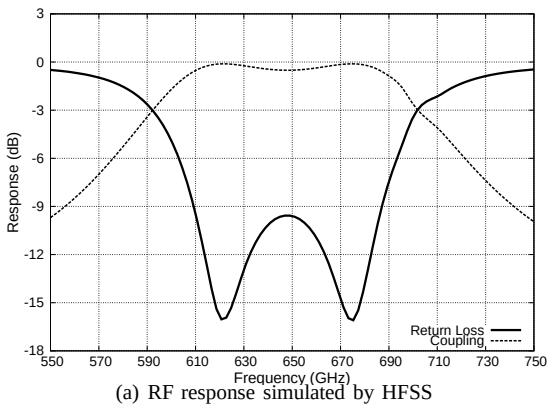
III. Mixer simulations

Following the design of the individual components, an HFSS model of the combined circuits was created in order to analyse the complete mixer chip structure. This took into account the effect of all interfaces, making sure the combination of various parts do not introduce anomalies in the final performance of the mixer design. Fig. 3 (a) shows the return loss and insertion loss of the complete RF design generated by HFSS. As can be seen, the electromagnetic simulator predicts an RF bandwidth of $\sim$100 GHz centred at 650 GHz. The power coupled to the junction is better than –0.5 dB within the entire operating bandwidth.

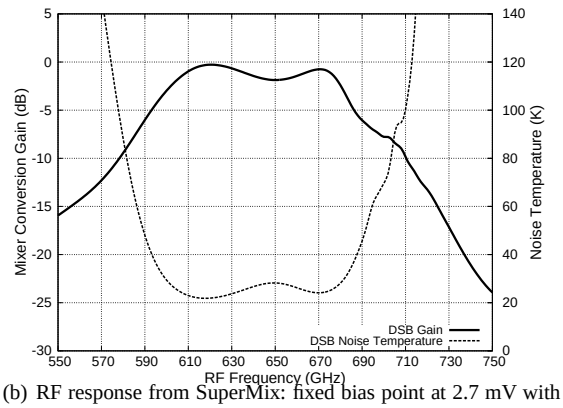
In Fig. 3 (b), we show an example of the calculations of *SuperMix* using the complete mixer model. The mixer chip S-parameters were imported from HFSS. These predictions match well with the HFSS output, verifying the integrity of our mixer design across a wide RF bandwidth. It can be seen that the RF gain and noise temperature are reasonably flat across the band. The simulation in Fig. 3 (b) shows clearly the effects of losses above the superconducting gap voltage, where the mixer conversion gain starts to deteriorate rapidly above 670 GHz.

IV. Device fabrication

Our mixer chips were fabricated at KOSMA, University of Cologne processing facility, by Dr. Paul Grimes. The Nb-AlO$_x$-Nb trilayer was deposited at the same time as the rest



(a) RF response simulated by HFSS



(b) RF response from SuperMix: fixed bias point at 2.7 mV with IF frequency set at 5 GHz

Fig. 3. (a) HFSS simulation showing broadband tuning of about 100 GHz centred at 650 GHz. (b) SuperMix simulation showing the predicted heterodyne performance of the mixer chip.

of the planar transmission lines. The mixer design assumed junctions with current density of $\sim$14000 A/cm^2 and an area of 1 μm^2. With these parameters and the tuning circuit dimensions, the mixer would have given good performance from 600 GHz to 700 GHz. However, impedance recovery performed to find the position of the resonance frequency and close inspection of the pumped IV curve, indicated that the tuning was shifted to below 600 GHz. Considering that the normal resistance of the junction came below the design value of 20 Ω, the low tuning frequency could be explained by a larger than designed tunnel junction area. This conclusion was supported by HFSS simulations which showed that an increase in the junction capacitance narrows down the operating bandwidth and shifts the tuning range downwards in frequency. The *SuperMix* model constructed earlier but with a larger junction area showed similar behaviour to the HFSS model. Unfortunately, our LO did not produce much power below 610 GHz, hence thick beam splitter needed to be used. Due to the broadband tuning design however, the performance did not deteriorate substantially at the high frequency end.

V. Results and analysis

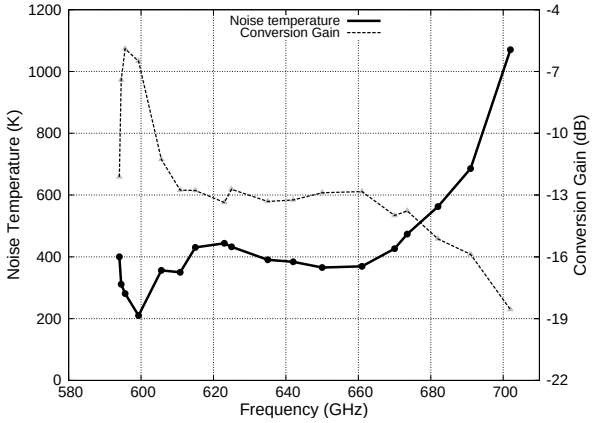


Fig. 4. Measured conversion gain and noise temperature against frequency for the tested unilateral finline mixer over the operating bandwidth.

The Y-factor of the mixer was measured over the frequency range where the LO power was sufficient to pump the device to an acceptable level. In Fig. 4, we show the measured gain and double-sideband (DSB) receiver noise temperature as a function of frequency between 595–702 GHz. These values represent the raw uncorrected data of the receiver, which includes the optical, the transmission line and the IF conversion loss, in particular the losses incurred by the 75 μm beam splitter used to pump the mixer near 600 GHz.

The best noise temperature was measured at 600 GHz,

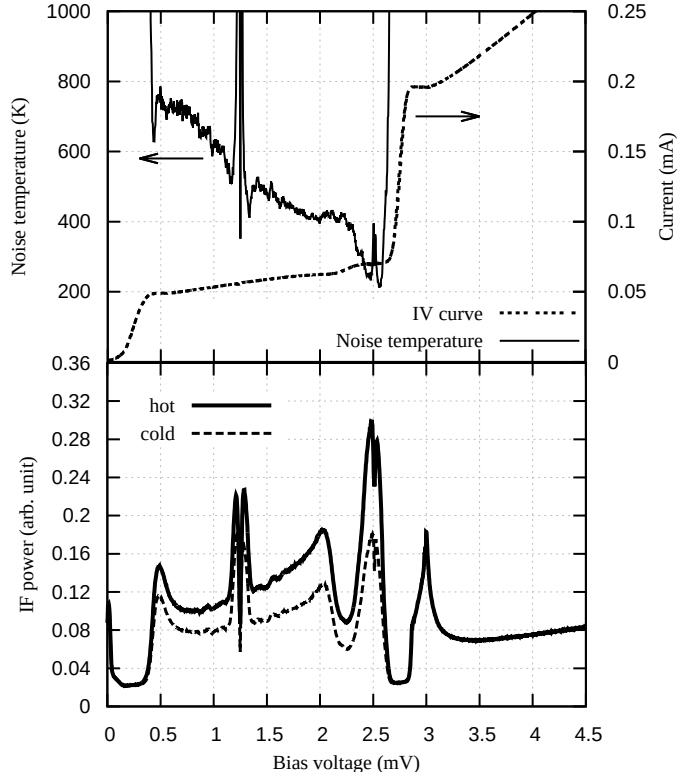


Fig. 5. IV characteristic of the tested mixer irradiated with a 600 GHz RF signal. The noise temperature curve is calculated using the measured hot and cold loaded IF curve.

significantly lower in frequency than the designed tuning central band (650 GHz), for reasons we explained in the previous section. As we have indicated above, we were unable to test the mixer below 600 GHz as a result of lack of LO power. Nevertheless, the tuning double dips are clearly seen in the plot and seem to be located around 600 GHz and 650 GHz. The uncorrected noise temperature below the superconducting gap was measured below 400 K. This is well above what can be achieved by modern mixers at these frequencies but is consistent with the behaviour of an untuned mixer. This argument can be supported by the result at 600 GHz where the noise temperature dropped to 145 K if corrected against the beam splitter thickness, and yet included all the other noise contributions.

In Fig. 5, we have plotted in the upper frame, the pumped IV curve and the noise temperature as a function of the biased voltage at 600 GHz. In the lower frame, we show the hot and cold IF response used to generate the noise temperature plotted above. The Shapiro steps can clearly be seen on top of the photon steps, indicating an incomplete suppression of Josephson pairs current. The Josephson features can be further suppressed by increasing the magnetic field across the junction, but would resulting in a slight suppression of the superconducting gap. The best noise temperature values are obtained at bias voltage values close to the superconducting gap, which can clearly be seen from the IF conversion plots.

VI. Conclusion

We have designed and tested a 700 GHz unilateral finline SIS mixer in the frequency range of 595–702 GHz. The mixer chip was fully modelled using a combination of HFSS and *SuperMix*. The measured performance agreed with the software predictions but was degraded at the high frequency end by a significantly larger than designed tunnel junction. The best uncorrected receiver noise temperature of 210 K was measured at 600 GHz using a 75 μm thick beam splitter, and remained reasonably low for the entire frequency range. The experimental investigation and data analysis indicate that the unilateral finline mixer should yield noise temperature of 100–150 K between 600-700 GHz. This performance, in addition to the large substrate area and simple mixer block, makes it attractive for designing balanced and single sideband mixers at THz frequencies.

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