Design of a 650 GHz Planar Circuit Balanced Mixer

Boon-Kok Tan, Ghassan Yassin, Paul Grimes, Karl Jacobs, and Stafford Withington

***Abstract*—We present the design of a broadband balanced superconductor-insulator-superconductor (SIS) mixer, which uses two back-to-back unilateral finline tapers. A key feature of our design is the use of a thin silicon-on-insulator (SOI) substrate, which enables the employment of a finline mixer at high frequencies. We integrated all of the required superconducting RF circuits onto a single chip using planar circuit technology, and retained the simplest fabrication processes without any lumped elements. This approach results in a very simple mixer-block design, which is desirable for constructing medium-format focal-plane imaging arrays. In the paper, we present in detail the electromagnetic modelling of each of the planar components making up the entire balanced mixer. The electromagnetic simulations were carried out using HFSS, and the heterodyne performance of the complete balanced chip was accessed using SuperMix.**

***Index Terms*—Superconducting coherent detectors, system-on-a-chip, submillimeter wave integrated circuits, silicon on insulator technology.**

I. Introduction

ADVANCED astronomical observations require mixers that are highly sensitive, low noise and can operate with broad RF and IF bandwidths. In recent years, sub-millimetre (sub-mm) receivers using superconductor-insulator-superconductor (SIS) tunnel junctions have already approached quantum-limited performance. The next paradigm is the construction of large-format focal-plane arrays. Previously, we reported a single-ended 650 GHz unilateral finline SIS mixer design [1] [2], requiring only a simple mixer-block architecture, which is highly desirable to enable the construction of compact medium-format (64 pixels) array receivers. In this paper, we upgrade the single-junction design to construct a balanced SIS mixer that can operate within ALMA Band 9 (602–720 GHz).

In contrast to the single SIS junction mixer, a balanced mixer has the ability to reject local oscillator (LO) noise, and to fully utilise the available LO power by eliminating the local-oscillator beam splitter (e.g., [3] and [4]). Our balanced SIS mixer uses two back-to-back unilateral finline tapers as waveguide to planar-circuit transitions. Unilateral finline chips have large substrate areas, which allow the elegant integration of complicated circuits [5] [6]. Both the finline tapers and the additional circuits required for balanced mixer operation are deposited on one side of a 15 μm silicon-on-insulator (SOI) substrate [4] [7]. The very thin substrate presents only a slight dielectric loading to the waveguide, and hence prevents the excitation of high-order modes over a relatively large bandwidth. The mixer-block also becomes simpler, and requires only a single rectangular waveguide without any supporting grooves in the wall. The chip is supported via gold beam leads (a few microns thick) attached between two halves of the split block. This arrangement makes balanced THz receivers markedly easier and cheaper to fabricate.

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II. Balanced SIS Mixer Design

In principle, one can form a balanced mixer by connecting two independent SIS mixers to the output ports of a 180° or 90° RF hybrid, and combine both the down-converted IF signals from the mixers using a 180° IF hybrid. Here, we chose to use a quadrature RF hybrid for its compactness, in conjunction with a 180° IF hybrid for output signal summation. As shown in Figures 1 and 2, our balanced mixer comprises six major RF components: unilateral finline tapers with matching notches, finline-to-microstrip transitions, an RF quadrature hybrid, DC/IF blocks, superconducting tuning circuits with SIS junctions, and RF chokes terminated with IF beam leads.

The easiest way to understand the operation of a balanced mixer is by considering the phases of the LO and the RF, with an additional LO noise component $\mathrm{LO}_{(n)}$ in-phase with the LO signal itself [8] [9]. For simplicity, we have assumed that all of these incoming (GHz) signals share the same reference phase $0°$. The RF signal from the sky and the LO signal generated locally, coupled onto the chip separately through two finline to microstrip transitions, enter the RF quadrature hybrid to produce two channels that each have a 90° phase difference between the RF and LO. These are written as $\mathrm{RF}\angle 0° + (\mathrm{LO} + \mathrm{LO}_{(\mathrm{n})})\angle 90°$ in the upper arm, and $\mathrm{RF}\angle 90° + (\mathrm{LO} + \mathrm{LO}_{(\mathrm{n})})\angle 0°$ in the lower arm, of Figure 1. Before feeding these combined signals into two separate SIS mixers, two DC/IF blocks are placed between the RF hybrids and the RF tuning circuits leading to the tunnel junctions, which prevent DC and IF coupling between the mixers. From each mixer, we now have IF outputs where the down-converted LO noise signals are $\pm 90°$ phase-shifted between the two branches. It can be seen that when the down-converted signals are combined in the 180° IF hybrid, the IF signal appears at the **sum** (Σ) port without LO noise, and the LO noise component appears at the **difference** (Δ) port without any signal. The configuration shown in Figure 1 assumes that both SIS mixers are biased with the same polarity. If they are biased with opposing polarity, one simply has to flip the polarity of the IF output of one of the mixers, since the IV characteristic of an SIS junction is anti-symmetric. In this case, the **sum** port

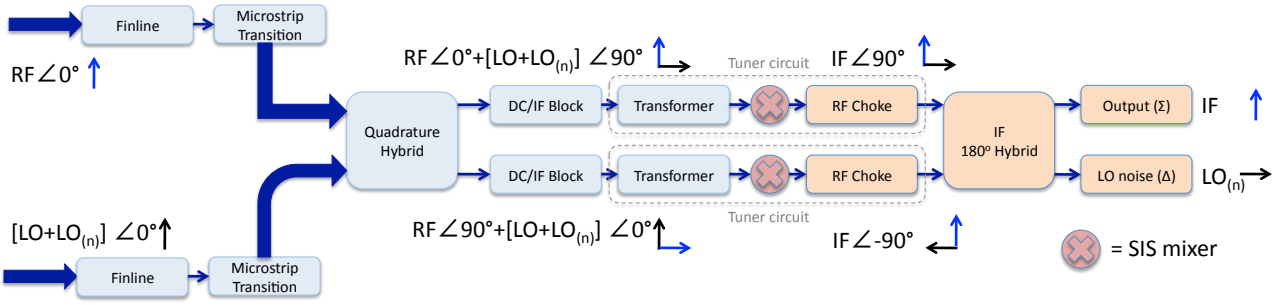


Fig. 1. Block diagram showing the components needed for a balanced mixer design. The phasors for the LO components are shown in black arrows, while the RF phasors are in blue. The 0° phase is referenced to the upward pointing direction and clockwise for positive phase shift.

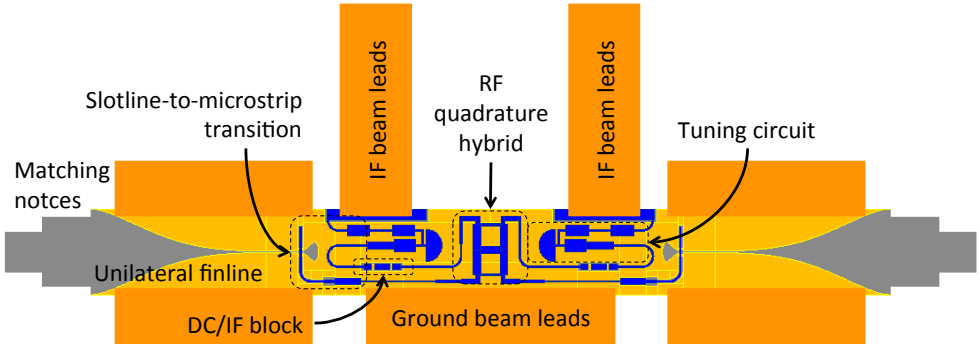


Fig. 2. Layout of the final balanced mixer chip showing various on-chip circuit components.

would be the LO noise output, while the **difference** port is the desired IF signal.

III. Design of the RF Passive Circuit Components

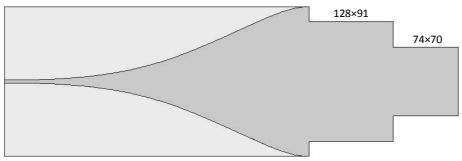
Conventionally, the components of a balanced SIS mixer are fabricated using mechanical machining techniques, which is challenging in the THz region. Also, the mixer blocks and other RF waveguide components (e.g., RF hybrid) are mechanically attached together (e.g., [3]), and the two single-ended SIS chips have to be carefully selected to ensure optimum performance. This approach results in a bulky, complicated assembly, which is exceptionally difficult to mass produce and pack into a focal plane imaging array. In recent years, there has been a great deal of enthusiasm to simplify these designs to enable the deployment of more advanced SIS mixers in the form of compact imaging arrays [4] [10].

We chose to use only planar circuit technology to ensure that the mixer block is kept as simple as possible. All of the RF components required are integrated on-chip, with a simple configuration consisting of a 15 μm SOI substrate ($\sim$2 mm long), a niobium ground layer (250 nm), a silicon monoxide dielectric layer (475 nm) and a niobium wiring layer (400 nm). This design removes the need for a separate hybrid block, and since both junctions are fabricated on the same chip, only a single external coil is needed to suppress the unwanted Josephson currents. The entire balanced mixer block is greatly simplified and reduced in size. The back-to-back architecture leads to a configuration that requires only a single, straight rectangular waveguide. The signal from the sky is coupled to the chip from one side of the block via a feed horn, while the LO power is coupled to the other side via a similar feed horn. A key advantage of this arrangement is that it eliminates the need for an LO-injection beam splitter, which normally wastes 90% or more of the available LO power. The lowering of the LO power requirement opens up the possibility of using a photonic LO source (e.g., [11]) rather than the commonly used varactor multiplied sources.

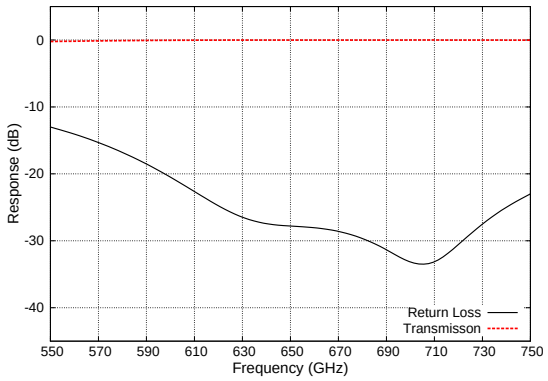
The balanced SIS mixer presented here is designed to work with circular Nb/AlO$_x$/Nb SIS tunnel junctions having an area of 1 μm^2. This size corresponds to a normal resistance of approximately 20 Ω, with a current density of approximately 14 kA/cm^2, and junction capacitance of 75 fF. All of the individual on-chip RF circuit components are matched with a system-wide characteristic impedance of 20 Ω (3 μm microstrip).

A. Waveguide-to-slotline transition

The profile of the unilateral finline taper was calculated using *FinSynth*, an Oxford University software package written by North [12]. *FinSynth* uses the Optimum Taper Method to search for a finline profile that has minimum length for a predesignated return loss. The profile of the taper was synthesised by converting the computed cutoff frequency taper into a slotline taper. The final design was checked by carrying out a full 3-D electromagnetic simulation using Ansys HFSS, including the effect of superconductivity on surface impedance, and the stepped dielectric matching notches.

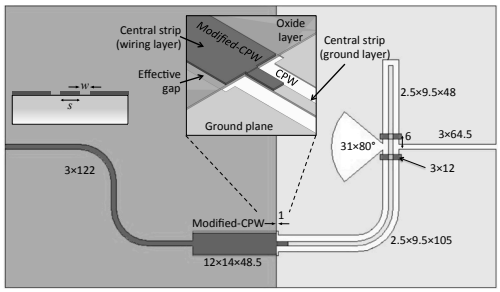


(a) Unilateral finline

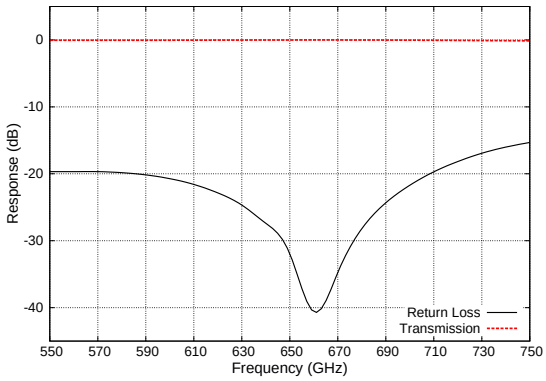


(b) S-parameters at 700 GHz band

Fig. 3. (a) Layout of the unilateral finline taper with a 2-step notch. The quoted dimensions of the matching notches are in width×length, in μm. (b) HFSS simulated transmission and return loss across the designated RF bands.



(a) Slotline to microstrip transition



(b) S-parameters at 700 GHz band

Fig. 4. (a) Layout of the slotline-to-microstrip transition via CPW sections. An enlarged 3-D view of the modified-CPW cross-over is shown in the inlet for clarity view. The dimensions for most structures are in width×length. For CPW, the quoted dimensions are in $s \times (2w + s)\times$length, in μm. (b) Return loss and coupling efficiency across the designated RF band.

As seen in Figure 3 (a), the unilateral finline tapers the slot width from 160 μm (waveguide height) to 2.5 μm, which reduces the characteristic impedance of the waveguide to values suitable for CPW or microstrip matching, ∼20–30 Ω. It is worthwhile noting that the slotline is in fact a natural high-pass filter, which prevents the IF signal from reaching the RF port. This feature is especially important when a broad IF operating range is required [13]. A matching notch is introduced before the finline to match the impedance of the substrate loaded waveguide to the empty waveguide. In our design, we used a 2-step rectangular notch (approximately quarter-wavelength long) to achieve a wide RF bandwidth. Figure 3 (b) shows the computed scattering parameters of the unilateral finline taper with the appropriate matching notches. The performance is excellent with the return loss below –20 dB over more than a 150 GHz bandwidth.

B. Slotline-to-microstrip transition

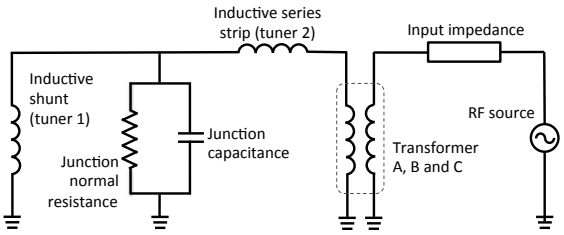
A transition is required to transform the slotline to microstrip. However, the design of this transition is not straightforward [5] because even for a 2.5 μm slot, suitable for photolithographic fabrication, the impedance of the slotline is still much higher than a suitable microstrip. On the other hand, CPW offers a wide range of impedance values that can be exploited to bridge the slotline-to-microstrip mismatch. Neglecting the fringing effects, the characteristic impedance of CPW is determined mainly by the ratio of the central strip width (s) to the gap width (w) between the central strip and the ground plane. Figure 4 (a) shows the final design of the slotline-to-microstrip transition. The RF power is guided from the slotline to CPW using a radial slotline stub and a quarter-wavelength ($\lambda_g/4$) CPW stub. Two short air-bridges are deposited across the CPW near the slotline-CPW junction to make sure that the ground planes are equipotential.

The section labelled 'Modified-CPW' is in fact a CPW with its central strip and the ground plane separated by an oxide layer. The gap w is defined by the effective distance between the edge of the central strip on top of the oxide layer and the edge of the ground plane beneath the oxide layer. This arrangement was adopted for two reasons: Firstly, to bring the CPW central strip over the top of the oxide layer, preparing it to form a microstrip line. Secondly, it allows a very narrow CPW gap to be employed without the likelihood of shorting the central conductor to the ground plane. As seen in Figure 4 (b), this method of designing the slotline-to-microstrip transition works well, having more than 160 GHz of bandwidth with less than –20 dB return loss.

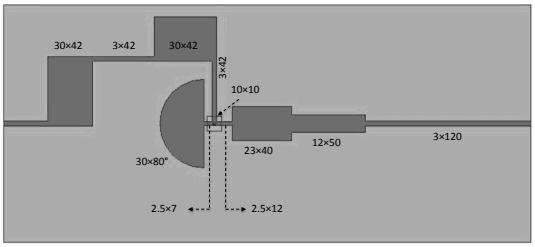
C. Tuning circuit

The tuning circuit comprises four parts: an inductive strip with a half-moon stub, an inductive strip before the junction, a multi-section transformer, and an RF choke [2] [6]. The lumped element equivalent circuit is shown in Figure 5 (a). In order to match the junction impedance across a wide bandwidth, two inductive strips, one in series and another parallel to the junction, were used to provide two resonance dips either side of the centre frequency.

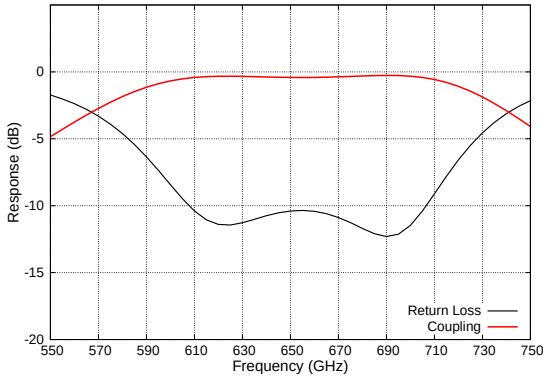
The first inductor, **Tuner 1** in Figure 5 (a), is a microstrip terminated with a $\lambda_g/4$ half-moon stub, which acts as a short



(a) Equivalent circuit



(b) Superconducting tuning circuit



(c) S-parameters at 700 GHz band

Fig. 5. (a) Electrical diagram representing the RF tuning circuit of the finline mixer. (b) Layout of the RF tuning circuit with an RF choke to prevent RF leakage to the IF port. The dimensions for various structures are similar to the previous figures. (c) Return losses and coupling efficiency of the tuning circuit across the designed RF band.

at RF frequencies. The microstrip line transforms the short into the inductance that is required to tune out the capacitance of the junction at frequency ω_1. To first order, the length of this microstrip can be calculated using the expression $\beta l \approx Z_0 \omega_1 C$, where $\beta = \dfrac{2\pi}{\lambda}$ is the guided wavenumber, C is the capacitance of the junction, Z_0 is the characteristic impedance of the microstrip (a function of the width of the line), and l is the length of the microstrip in the unit of electrical wavelength.

The second inductive microstrip, **Tuner 2**, is placed before the junction to tune out the residual capacitance at a slightly shifted frequency ω_2. The width and the length of this microstrip section can be determined using the standard transmission line equation $Y_s = (Y_l + iY_0 \tan\beta l)/(Y_0 + iY_l \tan\beta l)$, where Y_s is the source admittance, Y_l is the load admittance, $1/Y_0$ is the characteristic impedance of the line and βl is the propagation constant. By setting the imaginary part of Y_s to zero, the length of the microstrip can be obtained in terms of βl. The value of Y_0 is determined by the chosen width of the microstrip.

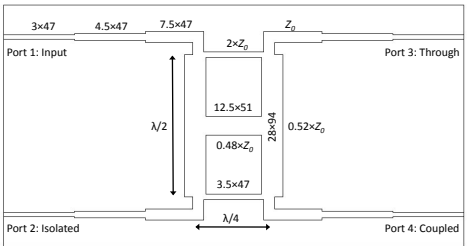
Connecting both inductive strips to the junction leads to the overall reactance being zero at two frequencies, giving the two poles in the matching diagram [14], as shown in Figure 5 (c). To match the impedance of this sub-circuit to the output impedance of the slotline-to-microstrip transition, a 3-step transformer was employed. Finally, a 5-section RF choke, consisting of alternating high and low impedance $\lambda_g/4$ sections of microstrip, was placed after the SIS junction to provide high rejection of the RF signal across the operating bandwidth: see Figure 5 (b). This filter prevents RF power leaking into the IF path.

D. RF quadrature hybrid

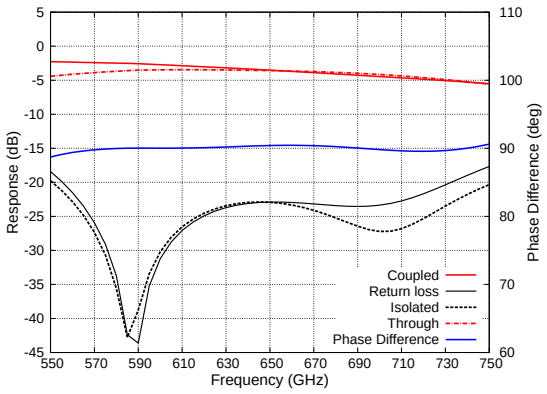
The RF quadrature hybrid was realised by a microstrip branch-line hybrid with a 90° phase difference between the two arms, as shown in Figure 6 (a). We cascaded two branch line hybrids to increase the bandwidth.

The highest impedance line, and therefore the narrowest microstrip, in the hybrid was chosen to be $2Z_0 \approx 20\Omega$, where Z_0 is the characteristic impedance of the four input/output arms. This impedance corresponds to a microstrip having a width of about 3 μm, well within standard photolithographic fabrication. A transformer was then used to transform the 10 Ω input/output microstrips back to the 20 Ω line. The distance between each T-junction is close to $\lambda_g/4$. All dimensions were then optimised for bandwidth in the final design using HFSS.

As shown in Figure 6 (b), the return loss and the coupling between the two input ports are less than –20 dB across the



(a) Quadrature hybrid



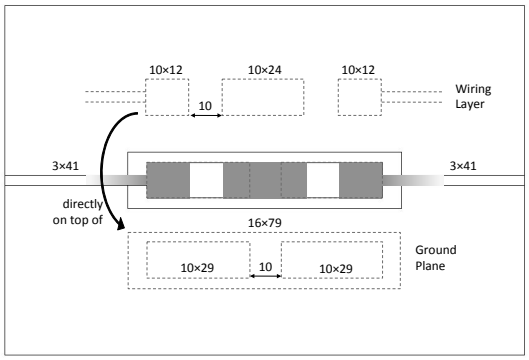
(b) S-parameters at 700 GHz

Fig. 6. (a) Layout of the 90° RF quadrature hybrid, with the dimension optimised by HFSS. (b) The S-parameters and the phase difference between the **coupled** and **through** arm of the hybrid across the designed RF band.

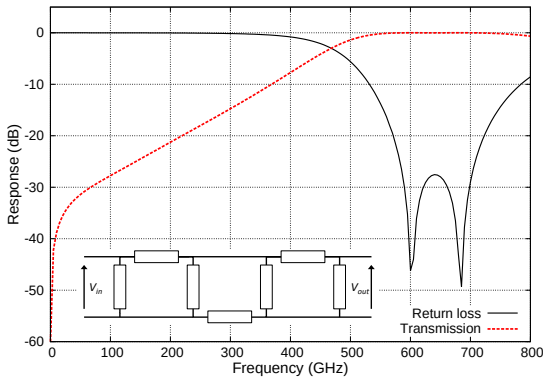
operating frequency range. The coupling to the **coupled** and the **through** arms is close to –3 dB, with only a small variation of ± 0.5 dB. The phase difference between the two output arms is constant at $90^\circ \pm 0.5^\circ$ across the entire band.

E. DC/IF block

The DC/IF block is used to isolate the two SIS tunnel junctions, and to prevent IF power leaking between the two mixers. To avoid using lumped elements, we employed a broadside coupler. The RF power from the microstrip is coupled to the underlying CPW, both separated by an oxide layer, and back to the microstrip, as shown in Figure 7 (a). The overlapping region between the microstrip with the central strip of the CPW determines the parallel capacitance between the input and the output ports, while the gap between the microstrips, and the gap between CPW stages gives the series capacitance (see the circuit diagram in the inlet of Figure 7 (b)). To first order, the required capacitance of the structure can be estimated from the overlapping areas and gap distances. This initial value was then optimised within the HFSS model to include the effects of the inductance of the transmission lines. Since both transmission lines are not in contact with each other, they are therefore always DC-isolated, and only the RF power within the resonant frequency band is allowed to pass through with minimum return loss. In circuit terms, it acts like a bandpass filter at RF frequencies, as shown in Figure 7 (b). Again, we cascaded two broadside couplers to widen the operating RF bandwidth.



(a) DC/IF block



(b) S-parameters at 700 GHz

Fig. 7. (a) Layout of the broadside coupler as DC/IF block. (b) The equivalent circuit and the performance of the DC/IF block simulated using HFSS.

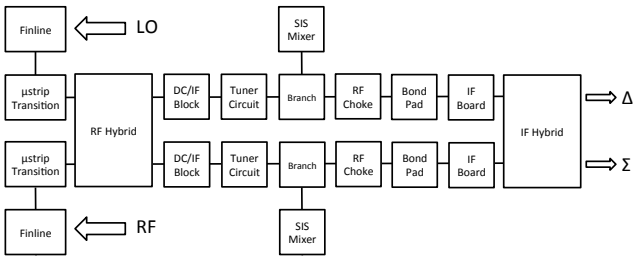


Fig. 11. Block diagram shows the various components included in the SuperMix simulation.

IV. Full Balanced Mixer Chip Simulations

The entire balanced mixer chip is electrically too large for HFSS to perform full 3-D electromagnetic modelling and further optimisation. Consequently, we approached the problem with two alternative techniques: Firstly, we combined only the subsection of the RF chip that includes the RF quadrature hybrid, the DC/IF blocks and the tuning circuits, without the finline taper and the microstrip transition. In the second method, we exported the HFSS generated S-parameters of each RF circuit component into Ansoft Designer (a schematic circuit design package) to form a complete RF mixer chip model. Both methods allow us to predict the performance of the complete mixer, but do not provide a means for full optimisation.

Figures 8 and 9 show the results of the simulations using HFSS and Ansoft Designer, respectively. It can be seen that the results obtained using the different methods agree well with each other. The power coupling to the two SIS junctions is almost identical, averaging at -4 ± 1 dB from 600–700 GHz. The phase difference between the two IF outputs from the SIS mixers is also kept to within $90 \pm 2^\circ$ from 580–720 GHz, while the return loss and isolation between the two input ports remains below –10 dB for about 120 GHz.

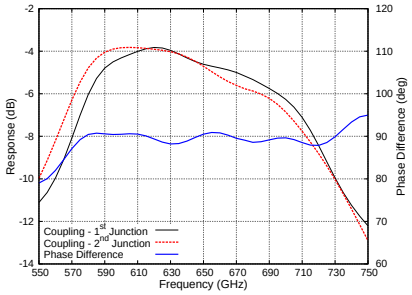
In order to estimate the heterodyne mixing performance of the complete balanced mixer, we formed a full-chip SuperMix [1] model via the HFSS generated S-parameters of individual circuit components [2], as shown in Figure 11. In Figure 10, we show an example of these calculations. Note that no IF transformer is included in these SuperMix calculations, but only two 50 Ω lines were used. As expected, the performance is good from 600–700 GHz and the IF response is flat, as shown in Figure 10 (b).

The fact that all of the simulated results from the different packages agree well is important because the circuit components presented above were simply cascaded to form the final balanced SIS mixer without further optimisation. The promising performance predicted by the packages demonstrates that our method of designing SIS mixers with complex circuit functionality is entirely feasible.

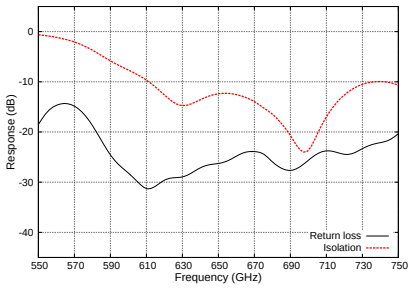
V. Conclusion

We have presented the design of a wideband unilateral finline balanced SIS mixer at 650 GHz using SOI planar-

[1] A Caltech superconducting SIS mixer design and analysis package [15].
[2] The 180° IF hybrid used was reported previously in [16].

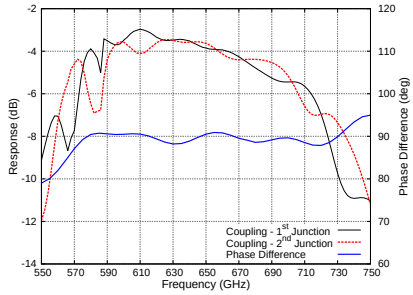


(a) Coupling and phase difference

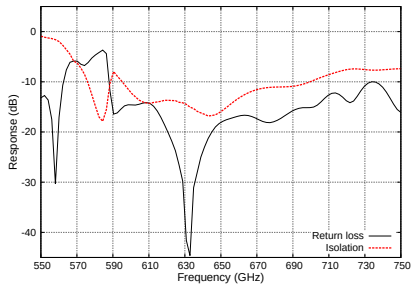


(b) Return losses and isolation

Fig. 8. HFSS simulation of a subsection of the mixer chip including the RF quadrature hybrid, the DC/IF blocks and the tuner circuits.

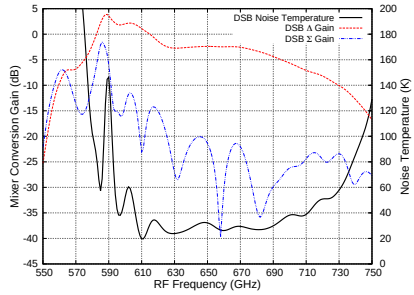


(a) Coupling and phase difference

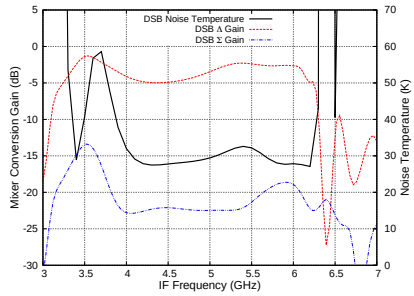


(b) Return losses and isolation

Fig. 9. Ansoft Designer simulations of the full balanced chip by importing various S-parameters from HFSS. The phase different is adapted from HFSS simulation with only the quadrature hybrid, DC/IF block and the tuner circuits.



(a) RF response



(b) IF response

Fig. 10. SuperMix simulations showing the predicted behaviour of the final design of the balanced mixer chip.

circuit technologies. The design results in an easy-to-fabricate mixer chip and mixer block with elegant yet fully integrated planar circuits. The performance was simulated fully using a rigorous 3-D electromagnetic package in conjunction with SuperMix. The simulated results predict satisfactory RF and IF performance across the designated RF and IF bands.

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