

# A High-Power Biasable 180-200 GHz Schottky Frequency Doubler Using Single-Waveguide Power-Combining

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## Abstract-

With state-of-the-art all-solid state terahertz sources producing now power levels of tenths of microwatts beyond 2 THz [1], efforts are now focused on increasing the amount of produced LO power in order to enable both arrays and room-temperature single-pixel receivers beyond 1-2 THz. For this task, more compact and effective power-combining topologies need to be employed to increase the power generated by Schottky diode based multiplied LO sources.

A novel dual-chip in-phase power combining doubler topology consisting in using two chips “sandwiched” within a single-waveguide channel was first introduced and successfully demonstrated in [2]. The proposed topology was robust and compact and avoids the use of Y-junctions or hybrid couplers. However, the achieved performance at 190 GHz was not state-of-the-art since the Schottky diodes available were not optimum for multiplier operation.

In this work, we present the design of a new 180-200 GHz MMIC doubler based in this recently introduced single-waveguide dual-chip topology (see Fig. 1a) and using the 12  $\mu\text{m}$  GaAs T-shape membrane process and Schottky diode process developed at the Rutherford Appleton Laboratory (RAL). The diodes are biased to achieve optimum varactor conditions and maximize the second harmonic generation. Two independent bias lines are included (one per chip) to allow the possibility of compensating possible unbalances between the two chips. State-of-the-art performance (25-30 % efficiency) is expected with power handling capabilities from 200 mW up to 400 mW (see Fig. 1b)

This work is part of *The Millimeter-wave Integrated Diode and Amplifier Source (MIDAS)* project to develop generic integrated Schottky diode and amplifier sources using European technology. The circuits are now under fabrication at the Rutherford Appleton Laboratory.

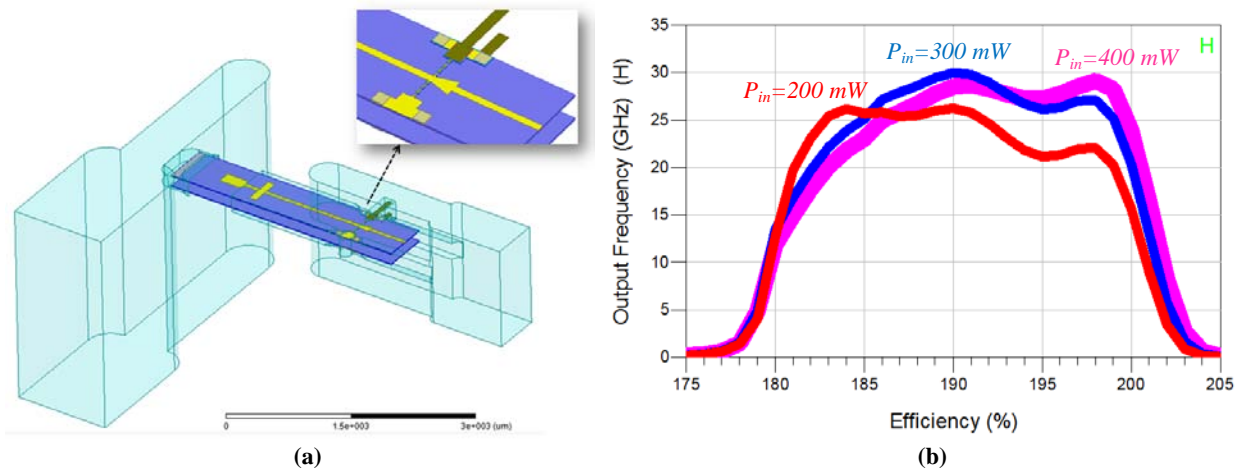


Fig. 1. MIDAS high-power dual-chip single-waveguide 190 GHz doubler design (a) and expected performance (b).

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