W-band balanced frequency tripler using a novel coupled lines biasing scheme compatible with flip-chip mounting

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***Abstract*- We present here a novel biasing scheme similar to [1] for balanced frequency triplers that is compatible with flip-chip mounting of the Schottky diodes chip onto a host carrier circuit, and that does not involve complicated lithographic fabrication techniques such as on-chip or on-circuit thin film capacitors. It uses coupled suspended striplines circuit architecture in order to bring two separate biasing lines to both half of the chips, allowing for independent biasing of each half of the diodes chip. This can be advantageous in order to correct for slight imbalances in the chip and circuit. Measurement results on a 83-105 GHz tripler using Teratech discrete tripler diodes and an AlN based circuit with a coaxial input shows a typical efficiency of approx. 7 %, with input power handling up to 200 mW, and 3 dB RF bandwidth of 83-105 GHz.**

I. INTRODUCTION

W-band sources are the base of high power and high frequency sources for millimeter and sub-millimeter spectroscopic and radiometric applications that require high spectral purity and high efficiency. For instance, good efficiency and minimum output power of 3-5 mW is required at W-band to pump a 183 GHz sub-harmonic mixer without the need to re-amplify the signal [2]. Moreover, in order to build Local Oscillator chains for the high millimeter and sub-millimeter frequencies, it is necessary to have a W-band source that does not generate undesired spurious harmonics that could mix in the following amplification/multiplication stages.

Traditionally, W-band multiplied sources that do not include an amplifier as last stage are either transistor based multipliers that are limited in efficiency due to the resistive nature of the active device (FET), or Schottky diode based, which are more efficient and have demonstrated already very good efficiencies and power handling capabilities. The possibility to reverse bias each Schottky diode is an advantage compared to unbiased devices in anti-parallel configuration for instance since it improves the efficiency and power handling capabilities. A cross-channel balanced configuration is usually preferred to a single anode device since it provides high even harmonics rejection (mainly 2nd and 4th one), and enables to put many Schottky devices in series in order to improve power handling capabilities. However, balanced triplers are traditionally more suited to MMIC technology since they traditionally require an on-chip MIM capacitor for biasing [3-4]. At W-band, it represents a lot of real estate on the wafer (chip size is relatively big).

We present here a novel biasing scheme for balanced frequency triplers that is compatible with flip-chip mounting of the Schottky diodes chip onto a host carrier circuit, and that does not involve complicated lithographic fabrication techniques such as on-chip or on-circuit thin film capacitors.

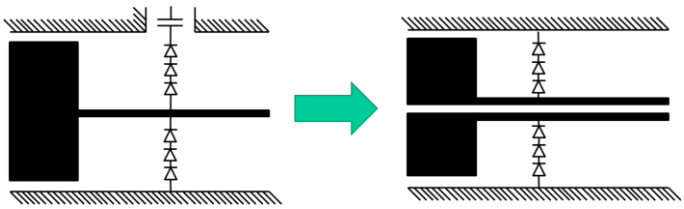


Fig.1: Proposed W-band balanced tripler using discrete Schottky diode chip using novel coupled lines biasing scheme (right) *VS* traditional biasing of balanced triplers (left).

II. W-BAND TRIPLER DESIGN

This novel approach uses a similar architecture as the multi-anode balance tripler previously described, but having a novel biasing scheme based on coupled lines. This original transmission line enables the use of discrete chip in a balanced configuration, without the need to develop a more complex on-chip or on-circuit MIM capacitor. This novel approach is illustrated in Fig. 1&2. As you can see in Fig. 1, a narrow gap in the central microstrip line allows for independent biasing of each separate transmission lines. At RF frequencies, these lines are coupled to each other, and the main propagating mode is the microstrip mode, as it would be if there was only one central microstrip line. By introducing as well gap on the GaAs tripler central pad as shown in Fig. 2, each branch of the chip featuring 3 anodes each can be reverse biased independently, making all the 6 anodes operating in Varactor mode, as it would be with a more traditional multi-anodes tripler. This architecture also allows for slightly different bias voltages to be applied on each branch of the chip, in order to compensate for any slight imbalances in the chip electrical characteristics. It is also expected that a differential biasing can be applied instead of two independent biasing voltages in order to bias the tripler.

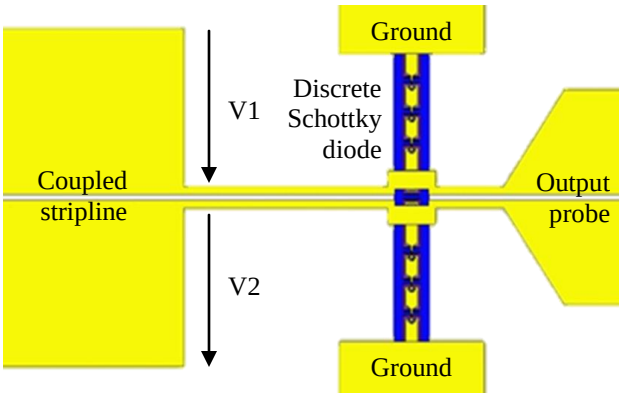


Fig.2. W-band balanced tripler based on novel coupled lines biasing scheme, and featuring a discrete 6-anodes tripler chip transferred onto AlN designed by RPG and fabricated by RAL using the standard Teratech process [5]. Chip size is approx. 700 um x 50 um.

The optimization and simulation of the tripler is done using a combination of 3D-EM simulations using HFSS (Ansys) [6], and ADS (Agilent) [7] non-linear circuit simulations. The predicted performances are shown below. For a fixed input power of 80 mW, the predicted efficiency ranges from 4% to 8% in the 82-105 GHz frequency range. The input return loss is calculated better than -10 dB, and the 4th harmonic rejection better than 30 dB. The input power range is estimated between 50 and 200 mW, thanks to the biasing capabilities of the tripler.

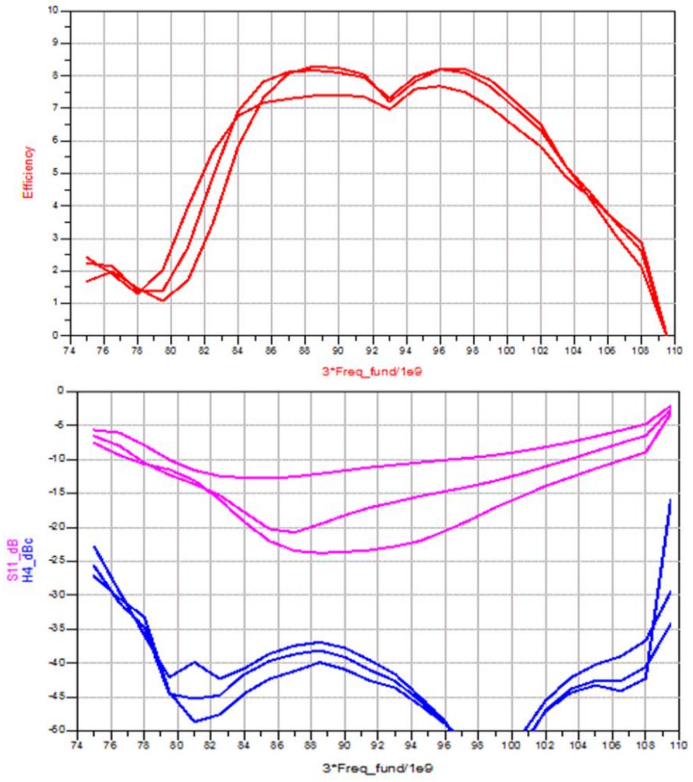
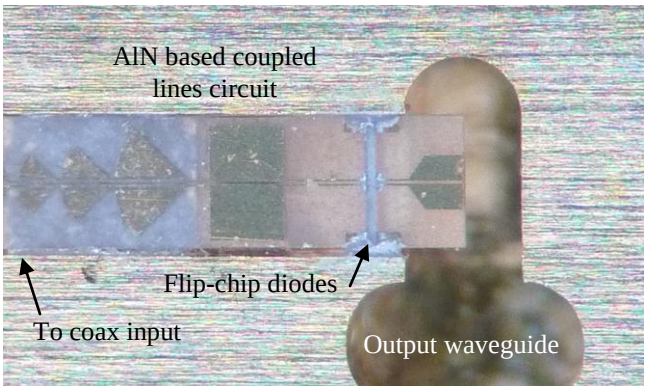


Fig.3.Top: Predicted performance of the W-band tripler for an input power of 80 mW, and differential reverse biasing between 2 V and 6 V. Bottom: upper curves shows the efficiency, lower curves show the input return losses and 4th harmonic rejection.

III. W-Band Tripler Fabrication

The W-band tripler featuring an AlN based circuit has been designed, fabricated and assembled by RPG. Two SMA connectors are used for the biasing lines. One K-type glass bead connector is used for input RF signal in Ka-band. The circuit is based on a 50 um thick AlN substrate. This choice is motivated by the high thermal conductivity of AlN (typ. 120-180 W/m.K), allowing for efficient heat dissipation of the tripler chip.



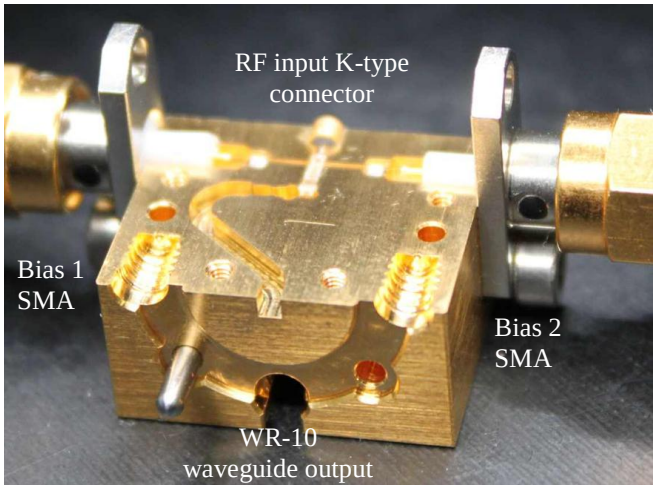


Fig.4. Top: Detailed view of the W-band tripler circuit, with the 6-anodes Varactor tripler chip flip-chip mounted onto the 50-um AlN circuit. Bottom: View of the RPG W-band tripler block (lower half), with the AlN circuit mounted inside and connected to two SMA connectors for biasing and a K-type glass bead for RF input signal.

IV. W-Band Tripler Test Results

Measurement results on a 83-105 GHz tripler using RAL discrete tripler diodes and an AlN based circuit with a coaxial input shows a typical efficiency of approx. 7 %, with input power handling up to 200 mW, and 3 dB RF bandwidth of 83-105 GHz. The bias voltage ranges from 1.7 V/branch in the low power range (approx. 50 mW), up to 6.5 V/branch in the high power range (approx. 160-200 mW), demonstrating the wide range of usable input powers for this tripler. Moreover, it is noticed that a fixed offset of 0.3 V between each branch is

necessary to get optimum efficiency and output power, regardless of the input frequency and power.

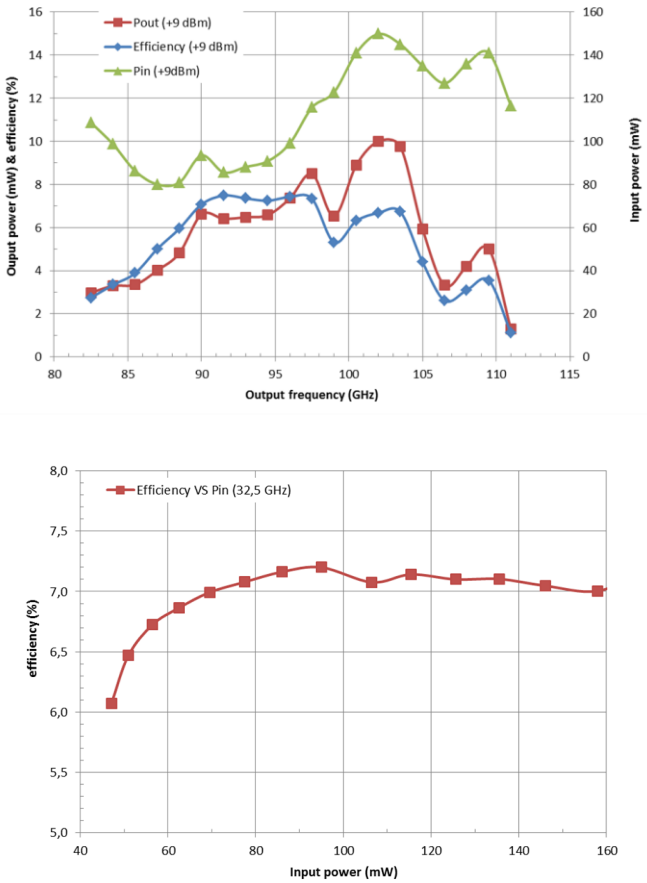


Fig.5. Top: Performances of the W-band tripler VS output frequency. Bottom: Efficiency VS input power of the W-band tripler at 97.5 GHz output frequency.

CONCLUSION

The design, fabrication and test of a W-band balanced tripler based on discrete GaAs Schottky diodes fabricated by RAL is presented. It includes a novel simple biasing scheme based on coupled microstrip lines on AlN based substrate designed and fabricated by RPG. Test results show that the tripler exhibits performances which are in accordance with the simulations. The output power is over 5 mW between 88.5 GHz and 105.5 GHz which corresponds to almost half of the W-band. It is also possible to replace the input coaxial K-type connector by a waveguide flange connection in order to reduce spurious harmonics from the lower frequency stages.

The tripler architecture has been validated over a wide range of input frequencies (i.e. 27.5-35 GHz) and powers (i.e. 80-200 mW). The microstrip input access of this W-band tripler allows further integration of an active multiplier/amplifier driver stage which is commercially available in Europe (for instance the CHX-2095 and CHA3093c devices from UMS [8]) into a very compact W-band source.

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