Solid State Frequency Multipliers at Sub-Millimeter Wavelength Using European Schottky Technology

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***Abstract*—We report upon the design of solid state frequency multipliers : a 380 GHz single-chip doubler, a 300 GHz single-chip tripler and a 300 GHz power combined dual-chip tripler. They are all designed with a dedicated model of european integrated Schottky diodes and in the triplers case with their on-chip capacitor for bias connection. A dedicated technology is developped in order to enhance device performance, in particular improve the power handling capabilities which vary from 50 mW for the single chip 380 GHz doubler up to 400 mW for the 300 GHz dual-chip tripler. The circuits are under fabrication at STFC-RAL.**

***Index Terms*—Frequency multipliers, Schottky diode, Doubler, Tripler, Power-combining, Sub-millimeter wave.**

I. Introduction

The terahertz spectrum is now willing to be fully exploited to enrich applications that span the physical, biological, and medical sciences. One of the remaining technology challenge at THz frequencies is to generate conveniently useful amounts of power. Schottky diodes based solid-state devices stand as first candidates where compact, non-cryogenic and efficient sources are needed. Therefore the Millimeter-wave Integrated Diode and Amplifier Source (MIDAS) project aims at developing MMIC power amplifiers and Schottky varactor diode circuits using European technology. The primary objective of the program is to demonstrate a 125 mW source operating at 270 - 300 GHz in conjunction with power combining technology. The designs of three last stage frequency multipliers using on-chip capacitor and integrated Schottky diodes are proposed during the first phase of the program and are presented in this article: a single-chip 380 GHz doubler, a 300 GHz single-chip tripler, and a 300 GHz in-phase power-combined dual-chip tripler. We report on the design and performance of these three designs.

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A. Towards a high frequency and high power MMIC fabrication process

MMIC technology applied to integrated Schottky structures is the key issue to lead to reproducible circuit performances and regarding to this could bring the instrumentalists forward to build well in-phase multi-chip power-combined sources. Furthermore, the technology developments pointed here favour high frequency and high power handling operation. For these reasons the main features discussed during the program focus on lowering the transmission losses while giving a great importance to thermal management : the mesa size is lowered down to 18μm $\times$ 18μm, on-chip capacitors based on polyamide insulating layer are developped to fulfill signal propagation requirements, the diode and circuit parameters are defined during the design phase to reach wide impedance matching, and beam leads (metal membrane) allow to suspend the membrane while providing precise grounding and thermal contact with the block. Diamond membrane has also proved to be beneficial to strengthen the heat path [1] but the bonding to a GaAs membrane is critical [2]. Moreover if the dielectric constant of the processed CVD diamond is not perfectly controlled, the design cannot be optimized accurately. Therefore a thick GaAs membrane could be equivalent electrically and thermally to a thin GaAs membrane transferred onto a diamond membrane. It was decided to design MIDAS project first phase frequency multipliers with a 12μm-thick GaAs membrane providing a thermal capacitance that could be empirically compared to its diamond-substrate transferred circuit counterpart.

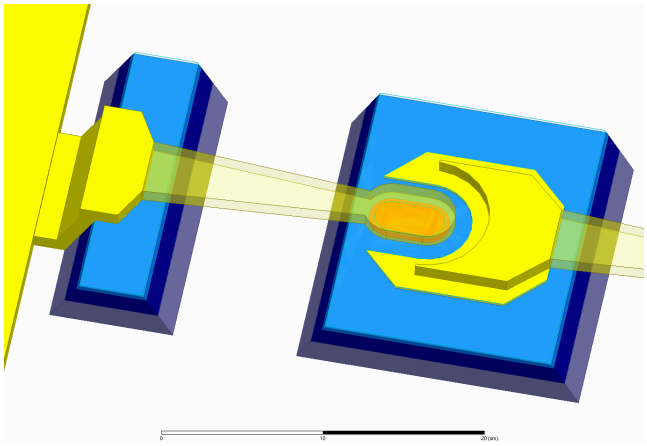

Fig. 1. 3D structure of the STFC Schottky diode upgraded for MIDAS program.

B. 380 GHz Doubler design

The circuit design of a 380 GHz fixed-tuned MMIC doubler is based on the balanced topology presented in [3]. The input frequency was chosen according to the second stage doubler output issued separately in this proceedings, which features a 190 GHz single-waveguide in-phase dual-chip doubler based on [4] and that is expected to provide between 50 to 100 mW depending on its input power handling capabilities (200 to 400 mW at W band) and on the first stage power amplifiers efficiency also developped during the program [1]. The 380 GHz doubler features an anti-serie set of four planar Schottky diodes integrated within the passive microstrip circuit onto a 12-μm thick GaAs membrane. The circuit geometry prevents the input fundamental signal from leaking into the output and also prevents the output second harmonic signal from leaking into the input waveguide. Moreover, the reduced height input waveguide cut off the input signal TM_{11} mode for a more efficient coupling to the diodes. A stepped impedance filter section at the opposite end of the circuit is used as a DC bias voltage path and avoid the leakage of the second harmonic through this port. Therefore on-chip capacitor is not necessary for this particular design. The input and output waveguides, the microstrip channel and the DC bias connector sockets are milled into two split-waveguide metal blocks. The position of the input backshort, the diodes geometry, the input stub near the diodes and the output probe were optimized to reach a wide impedance matching over the input frequency band.

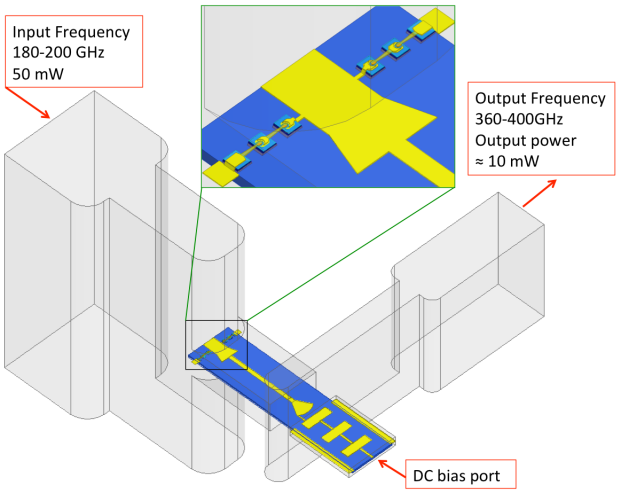

Fig. 2. Picture of the fully optimized 380 GHz doubler placed inside the waveguide cavity.

The methodology used for the design uses a combination of linear/non-linear circuit simulations (Agilent ADS) and 3D electro-magnetic simulations (Ansoft HFSS). Firstly, a standard diode model from the ADS library was implemented together with its close 3D passive environnement (diode cell), plus ideal input and output matching networks. During this simulation, the anode zero junction capacitance and the diode cell geometry (anodes positions, input channel width and input stub length) were optimized using the harmonic-balance routine for 50 mW input power in order to reach optimum efficiency (see Fig. 3). The corresponding diodes impedances are Z_{IN} = 13 - j. 89 Ω, and Z_{OUT} = 33 + j. 28 Ω respectively at input and output frequencies, with a bias voltage of -5 V. These embedding impedances values as a function of frequency were exported into Z-files which were used as a first input of the linear optimization. Secondly, each of the transition in the circuit including step impedances, coupling probes and waveguide transitions were simulated within the 3-D electromagnetic environment with appropriate boundaries, waveports assignment and de-embedding planes. The simulation outcomes (2-D S-parameter matrices and their attenuations, impedances and permittivity values at central guided frequencies) were used a second input of the linear optimization. During this optimization step, the matching network was simulated with the "S-parameter" and "Optim" routines of ADS in order to find optimum lengths of the circuit. The diode impedance frequency set is accessed through a "DAC" file component and the S-parameter matrix through "Data-item" component with a number of ports that corresponds to the ports defined in the 3D EM simulation. A first set of circuit dimensions was found by optimizing the coupling between diodes and output port, which transmission magnitude should reach a maximum of $1/\sqrt{4}$ = 0.5 . The center pad, the output probe and the DC bias filter were optimized for wideband impedance matching. A second set of value was found by refining the optimization with the harmonic balance routine. Few iterations between the linear and the nonlinear optimizations were performed until the emergence of acceptable performance. Finally, the each section values found during the previous steps were feed back in HFSS to build the full doubler circuit structure as shown in Fig. 2. Its performance were then checked using the nonlinear harmonic balance routine.

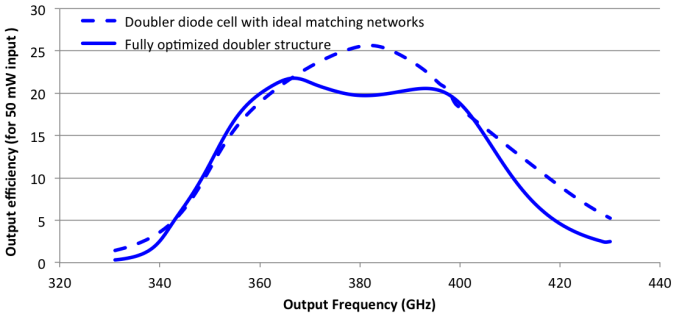

Fig. 3. Predicted performance of the 380 GHz doubler, the dot curve is the efficiency of the diode cell with ideal matching network, the full line is the fully optimized circuit as illustrated in Fig.3.

The electrical parameters of the STFC-RAL Schottky diode model considered in the simulations are a series resistance Rs = 7.5 Ω, an intrinsic zero voltage junction capacitance of Cjo = 15.7fF, a saturation current Isat = 150 fA, an ideality factor = 1.3 and a built-in potential Vbi = 0.85 V. This design was optimized for 50 mW of input power and -5 V bias voltage. The diodes anode area is 2.2μm $\times$ 4.5μm. Fig.3 shows the estimated efficiency of the doubler. Expected Performances gives 20% efficiency over 10% bandwidth.

[1]by Radiometer Physics Gmbh

C. 300 GHz Tripler designs

1) Tripler single chip design: The tripler features six integrated GaAs Schottky diodes in a balanced configuration based on [5]. The on-chip capacitor is integrated within the membrane according to STFC-RAL fabrication process. This integration provides a precise DC connection, but also allows a better control of the bias port, which is shifted away from the diode cell and which dimensions are chosen to avoid any leakage of the output signal. A notch in the bias line is mandatory to meet the photolitographic process requirement but has negligible impact on the circuit performance. The input and output waveguide dimensions cut off respectively the input signal TM_{11} mode and the second idler harmonic TE_{10} and TM_{11} modes. A detailed explanations of the design methodology of the circuit are given in [5]. The optimization is performed using 3D electromagnetic codes alike for the doubler, but the methodology slighty differs from the 380 GHz doubler as the initial diode cell optimization includes the diodes plus a section of the chip-channel and its on-chip capacitor. The optimum diode junction capacitance and bias voltage were determined at the same time to reach highest efficiency and power handling as possible. When the tripler circuit was achieved, then the input waveguide network had to be tuned to reach wide-band performance. This step was done with a linear optimization that allow an easy manual tuning of the matching network circuit. Firstly the tripler diodes ideal impedances were computed with the harmonic balance routine with ideal matching networks to converge to an optimum efficiency. The corresponding set of impedances are Z_{IN} = 32 -j 80 Ω, and Z_{OUT} = 24 + j 44 Ω respectively at input and output frequencies. The idler impedance is close to zero that confirms that the power is ideally transposed to the third harmonic. Secondly, the input and output matching network was divided into several individual sections, and the discontinuous parts between them were simulated in HFSS. The resulting S-parameter matrices and the diodes optimum embedding impedances were then utilized to determinate a first set of circuit dimensions using the linear simulator in ADS by optimizing the coupling between diodes and output port. The optimisation goal of the port-to-port matching is the transmission from the input port to each of the 6 anodes which maximum magnitude were $1/\sqrt{6}$ = 0.4 . When the non-linear matching had achieved the desired coupling with an optimal tuning, the circuit was simulated with the harmonic balance routine to check the tripler coupling efficiency, global efficiency and output power.

The electrical parameters of the Schottky diode model considered in the simulations are a series resistance Rs = 5.4 Ω, an intrinsic zero voltage junction capacitance of Cjo = 26 fF, a saturation current Isat = 100 fA, an ideality factor = 1.2 and a built-in potential Vbi = 0.85 V. The bias value applied to the 6 diodes in series is 13 V. Expected simulated performances gives between 5% and 10% percent efficiency over 17% bandwidth with 200 mW of input power as shown in Fig.4. The block and tripler are being fabricated at STFC

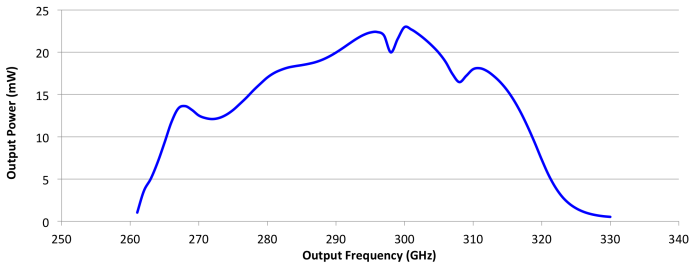

Fig. 4. Simulation results of the Single Chip 300GHz Tripler : Output power with 200 mW of input power.

with a variation of two different epilayer doping densities : 1.10^{-17}cm^{-3} and 3.10^{-17}cm^{-3} and with the corresponding 30μm^2 and 17μm^2 anodes area, with $\pm$ 15% bracketing.

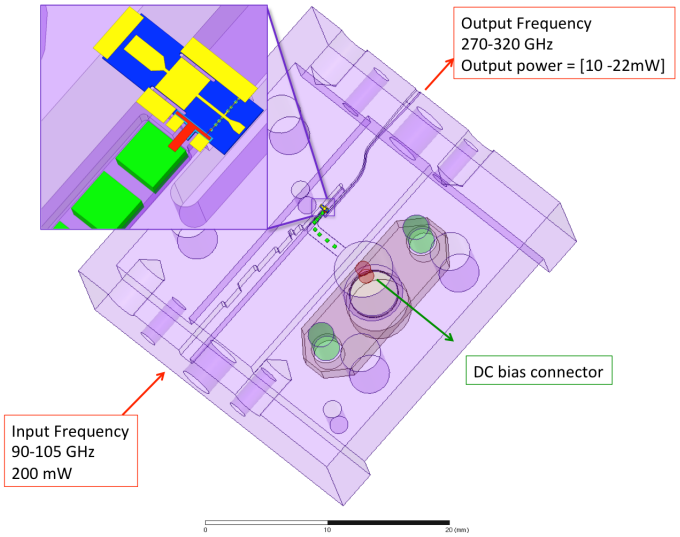

Fig. 5. Single chip 300GHz tripler mounted in half part of the split block with its input waveguide matching network.

2) Tripler power-combined design: The topology used for this design is similar to the one presented in [6], but with bias ports reported to the other side of the input waveguide that makes possible to have in-line matching network waveguide transitions. This solution bypass the need for curvatures in the input waveguide and avoid unwanted phase shift (and imbalance) between the input port and the diodes of the two symmetrical chips. As for the doubler and tripler single-chip designs, the matching network optimization consists in a combinaison of linear / non linear simulations that converge to a final configuration. The ideal diode impedance set used in the linear simulation was the one found for the single chip tripler. The optimisation goal of the port-to-port matching was the transmission between the input port to each of the 12 diodes which maximum magnitude was $1/\sqrt{12}$ = 0.28 . Preliminary performances give above 6% efficiency over 15% bandwidth, therefore 25 mW to 35 mW of output power is expected over the 270-315 GHz band with 400 mW input power.

II. Conclusion

Three multiplier designs are presented : a 380 GHz single-chip doubler, a 300 GHz single-chip tripler and a 300 GHz

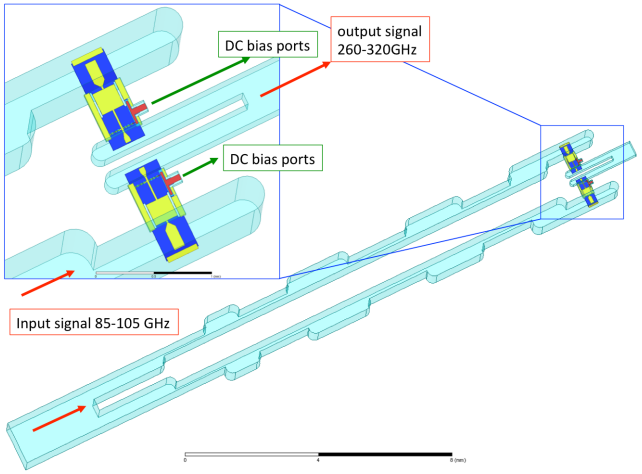

Fig. 6. Picture of the fully optimized dual-chip 300GHz power combined tripler.

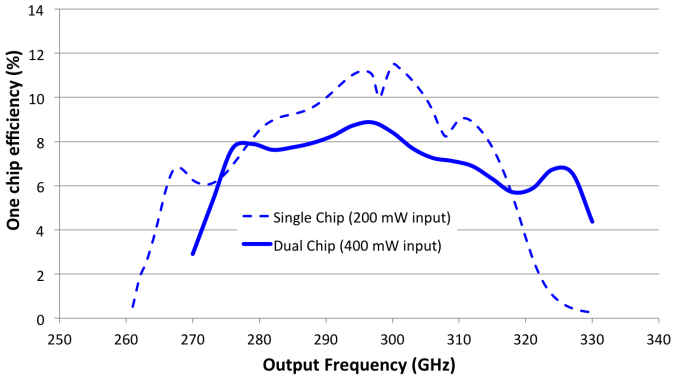

Fig. 7. 300 GHz dual-chip power-combined tripler preliminary predicted output power efficiency compared to the single chip as given in Fig.6.

in-phase power-combined dual-chip tripler. These designs use combinaison of linear/non linear optimization benches where manually tuning of the output and input matching networks is possible with dedicated transmission goals for respectively the output port to each of the diodes (doubler) and the input port to each of the diodes (tripler). This methodology helps to widen drastically the performance bandwidth of the frequency multipliers. These designs are implemented with a model of MMIC diode circuits and their on-chip capacitor developped with STFC-RAL fabrication process for MIDAS high frequency and high power requirements.

ACKNOWLEDGMENT

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