Low Noise TES Array for the Short Wavelength Band of the SAFARI Instrument on SPICA

P. Khosropanah, R. Hijmering, M. Ridder, M. A. Lindeman, L. Gottardi, M. Bruijn, J. van der Kuur, J.R. Gao, B.D. Jackson, H. Hoevers, D. Morozov, and P. D. Mauskopf

***Abstract*—SPICA is an infra-red (IR) telescope with a cryogenically cooled mirror (~5K) with three instruments on board, one of which is SAFARI that is an imaging Fourier Transform Spectrometer (FTS) with three bands covering the wavelength of 34-210 μm. We develop transition edge sensors (TES) array for short wavelength band (34-60 μm) of SAFARI. These are based on superconducting Ti/Au bilayer as TES bolometers with a Tc of about 105 mK and thin Ta film as IR absorbers on suspended silicon nitride (SiN) membranes. These membranes are supported by long and narrow SiN legs that act as weak thermal links between the TES and the bath. Previously an electrical noise equivalent power (NEP) of 4×10^{-19} W/√Hz was achieved for a single pixel of such detectors. As an intermediate step toward a full-size SAFARI array (43×43), we fabricated several 8×9 detector arrays. Here we describe the design and the outcome of the dark and optical tests of several of these devices. We achieved high yield (>93%) and high uniformity in terms of critical temperature (<5%) and normal resistance (7%) across the arrays. The measured dark NEPs are as low as 5×10^{-19} W/√Hz with a response time of about 1.4 ms at preferred operating bias point.**

***Index Terms*—Transition-edge sensor, TES, far infra-red spectrometer, submm spectrometer, SiN membrane.**

I. INTRODUCTION

SPICA is a Japanese-led mission to fly a 3.25 m diameter IR telescope with a cryogenically cooled mirror (~5K) [1]. Cooling the optics reduces the background radiation caused by the ambient temperature of the FIR space telescopes that limits the sensitivity. The loading is then dominated by astrophysical background sources. The SAFARI instrument is an imaging Fourier Transform Spectrometer (FTS) on SPICA with three bands covering the wavelength ranges: 34-60 μm (S-band), 60-110 μm (M-band), and 110-210 μm (L-band) [2]. Transition edge sensor (TES) is the chosen detector technology for the SAFARI instrument that is currently being developed in collaboration with several European institutes. Here the focus is on the detector arrays for the S-band. These are based on superconducting Ti/Au bilayer as the sensitive element on a suspended silicon nitride (SiN) membrane. In order to take full advantage of the cooled optics, the detectors need to have a background-limited sensitivity that translates to a dark NEP of 6.5×10^{-19} W/√Hz as a requirement and 2.8×10^{-19} W/√Hz as a goal. This is about 2 orders of magnitude higher sensitivity than what is required for detectors on a ground based telescope and imposes a great challenge on the detector technology. Among other tight specifications are the array size (43×43), pixel size of 840×840 μm^2 (likely), a speed of 40-100 Hz (i.e. response time of 0.8-4 ms) and a saturation power of about 5 fW.

Previously we presented dark measurements of single pixel TESes with different designs and geometries [3,4], where an electrical (dark) NEP as low as 4×10^{-19} W/√Hz was achieved [5]. Also the optical tests on some of these devices have been reported, where a coupling efficiency of about 40% was measured for a detector with a large absorber (200×200 μm^2) that was sitting in the center of a hemispherical cavity with a conical horn in the front [6-8].

As an intermediate step toward full-size SAFARI detector arrays, we have fabricated arrays of 8×9 of these devices on two different membrane thicknesses. This paper reports on the electrical tests of some of these devices. First the details of TES detectors are explained. Then we move on to the description of the arrays followed by the results of the dark tests.

II. TES DEVICES AND ARRAYS

The devices under test are based on Ti/Au (16/65 nm) bilayer, deposited on 500 or 250 nm thick SiN membrane. The TES size is 50×50 μm^2 and the critical temperature (T_C) is around 105 mK. In order to test these devices optically, we have an absorber close to each TES, which is a 75×75 μm^2 Ta with thickness of 8 nm. The sheet resistance of Ta is about 400 Ω that matches well with the free-space impedance (377 Ω). The absorber and the TES are sitting on a 140×80 μm^2 suspended membrane that is supported by four SiN legs. The legs are 2 μm (nominal) wide and 1000 or 1500 μm long in order to thermally isolate the TES from the reservoir and insure high sensitivity. As it is shown in Fig. 1 parallel legs geometry was used in order to have long supporting legs while keeping the pixel size according to the SAFARI specifications (840 μm).

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P. Khosropanah, R. Hijmering, M. Ridder, M. A. Lindeman, L. Gottardi, M. Bruijn, J. van der Kuur, J.R. Gao, B.D. Jackson and H. Hoevers are with the SRON Netherlands Institute for Space Research, Sorbonnelaan 2, 3584 CA Utrech, the Netherlands (phone: +31-88877-5600; fax: +31-888-77 5601; email: P.Khosropanah@sron.nl).

J. R. Gao is also with Kavli Institute of NanoScience, Delft University of Technology, Delft, the Netherlands.

D. Morozov, and P. D. Mauskopf are with Cardiff University, School of Physics and Astronomy, Cardiff, CF24 3AA, UK.

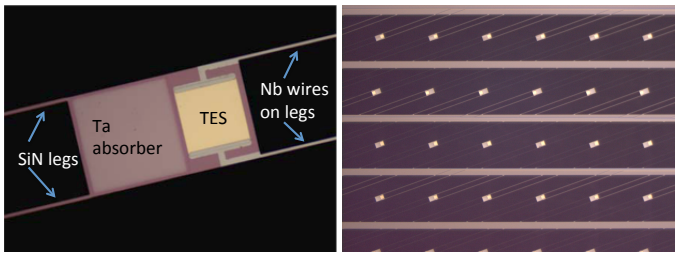

Fig. 1. (Left) A single pixel TES as a part of the 8×9 array. The size of the SiN island is 140×80 μm^2 that is 250 or 500 nm thick. The TES is a 16/50 nm thick Ti/Au bilayer (50×50 μm^2) and the absorber is an 8 nm thick Ta (75×75 μm^2). (Right) A picture of a part of the array with parallel legs geometry. The length of the legs is 1000 or 1500 μm while the pitch size is 840 μm.

III. Dark Tests

Two arrays with 8×9 detectors were selected for the dark tests and overall 14 devices were measured during 4 runs. The designs of TES detectors in the two chips are identical apart from the fact that one was fabricated on a 500 nm thick SiN membrane and the other on a 250 nm one. Fig. 2 shows a picture of one of these arrays.

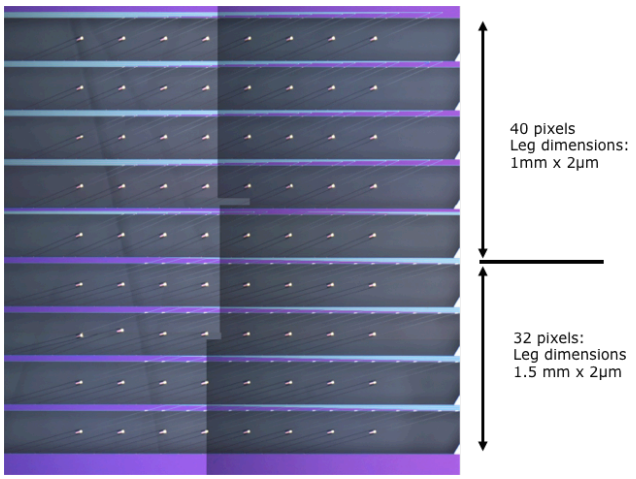

Fig. 2. Picture of an 8×9 TES array. It consists of two TES designs, 40 devices on the top with 1 mm long legs and 32 devises in the bottom with 1.5 mm log legs. The nominal width of the legs for all devices is 2 μm.

For the dark tests the detector chip is mounted in a light tight box that is shown in Fig. 3. It is designed to minimize the background loading due to possible stray light. The electrical wiring of the light tight box to an array chip goes through a meander path that is filled with Stycast mixed with SiC grains, which should act as a perfect blackbody absorber. After a TES chip is mounted, the box is closed, indium sealed and vacuum pumped.

An additional module is attached to this box that accommodates a heater, a coil and a thermometer. The heater and thermometer are used to regulate the temperature on the chip mount locally. The coil is for applying a magnetic field in the vertical direction to cancel a remnant magnetic field if present. Maximum four devices were wired in every run and read out by separate SQUIDs.

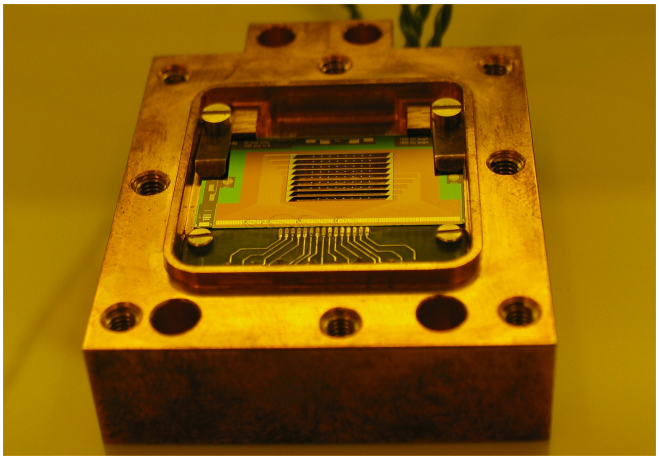

Fig. 3. The light tight box with the array chip mounted inside.

The dark tests start with measuring a series of current-voltage (IV) curves at different bath temperature. The bias power in the superconducting transition determines the saturation power for each of these bath temperatures, which in turn gives the thermal conductance (G) between the TES and the bath. Besides, the responsivity at very low frequency for each bias point is calculated, using the bias voltage across the device and the bias circuit. Next, the noise current spectra are measured at different bias points. Dividing the noise current by the corresponding responsivity gives the dark noise equivalent power (NEP), which is the same at all the bias points in the transition. The details of this characterization method can be found elsewhere [3,4].

The NEP at low frequency is dominated by the phonon noise that can be estimated as [9]:

$$NEP = \sqrt{4\gamma k_B T_C^2 G} \qquad (1)$$

where k_B is the Boltzmann's constant and γ is a number between 0.5 and 1 that depends on the heat transport mechanism and the critical temperature of the TES (T_C) and the bath temperature (T_{bath}). In our case γ is about 0.5 with T_C and T_{bath} being 105 mK and 30 mK, respectively.

Table 1 and 2 summarize the measurement results on the chip with 500 nm thick SiN membrane. In run #1 four devices with 1 mm long legs were tested. The critical temperature (T_C) and the normal resistance (R_n) of these devices were very uniform. The T_C lies between 103 to 106 mK, which is pleasingly close to what we designed (100 mK). Despite having exactly the same geometry, large variations in saturation power and the thermal conductance (G) were measured. We repeated this run by measuring the same devices again but swapped the channels to investigate if the SQUIDs had influenced the results and measured very similar values. In run #2 four devices with 1.5 mm long legs were measured. As one can see, similar uniformity in T_C and R_n were observed and similar non-uniformity appeared in the saturation powers and the G's. The T_C and R_n variations for these devices are about 3% and 6%, respectively. The saturation power difference for 1 mm leg devices can be as large as a factor of 1.5 and for 1.5 mm leg devices the difference can increase to 1.9. The lowest measured dark NEP is 7×10^{-19} W/√Hz for a 1.5 mm long leg TES.

TABLE 1 SUMMARY OF THE MEASUREMENTS FOR 500 NM THICK SIN MEMBRANE ARRAY IN RUN #1

TES Parameter	P33	P16	P32	P09
Leg length [μm]	1000	1000	1000	1000
Tc [mK]	106	103	106	105
Rn [mΩ]	167	164	158	160
Sat. power [fW]	22.4	28.9	35.6	33.4
G [pW/K]	0.57	0.73	0.87	0.83
Exp. NEP [aW/√Hz]	4.15	4.15	4.15	4.15
Meas. NEP [aW/√Hz]	0.85	0.9	1.05	1.05

TABLE 2 SUMMARY OF THE MEASUREMENTS FOR 500 NM THICK SIN MEMBRANE ARRAY IN RUN #2

TES Parameter	P56	P45	P41	P70
Leg length [μm]	1500	1500	1500	1500
Tc [mK]	103	103	103	103
Rn [mΩ]	168	166	163	160
Sat. power [fW]	13.1	15.8	14.2	24.7
G [pW/K]	0.31	0.38	0.34	0.59
Exp. NEP [aW/√Hz]	0.3	0.33	0.32	0.42
Meas. NEP [aW/√Hz]	0.7	0.8	0.75	1

TABLE 3 SUMMARY OF THE MEASUREMENTS FOR 250 NM THICK SIN MEMBRANE ARRAY IN RUN #3

TES Parameter	P16	P69	P09
Leg length [μm]	1000	1500	1000
Tc [mK]	103	106	105
Rn [mΩ]	169	158	160
Sat. power [fW]	21.3	3.5	10
G [pW/K]	0.55	0.07	0.25
Exp. NEP [aW/√Hz]	0.4	0.14	0.27
Meas. NEP [aW/√Hz]	0.75	0.5	0.6

TABLE 4 SUMMARY OF THE MEASUREMENTS FOR 250 NM THICK SIN MEMBRANE ARRAY IN RUN #4

TES Parameter	P66	P64	P72
Leg length [μm]	1500	1500	1500
Tc [mK]	105	101	102
Rn [mΩ]	170	170	166
Sat. power [fW]	3.6	5.5	3.4
G [pW/K]	0.07	0.11	0.07
Exp. NEP [aW/√Hz]	0.15	0.18	0.14
Meas. NEP [aW/√Hz]	0.5	0.6	0.5

Table 3 and 4 summarize the measurement results on the chip with 250 nm thick SiN membrane. This time we were only able to measure three devices in each run. In run #3 the T_C and R_n were very uniform. However we observed a factor of two difference in saturation power between device P16 and P09 despite of having exactly the same geometry. Three out of four devices with 1.5 mm long legs were very uniform. The variations in terms of the T_C and R_n for these devices are about 5% and 7%, respectively. Although the device P64 has 1.6 times higher saturation power than other three (including P69 in run #4), in general the variation seems to be smaller. Dark NEPs as low as 5×10^{-19} W/√Hz were measured. This is particularly interesting because this is the first time such a low NEP is demonstrated in an array. The devices made on 250 nm SiN membrane have a lower NEP and a lower saturation power in comparison with those on 500 nm SiN membrane. This is expected because the thinner SiN gives a lower thermal conductance.

The speed of these devices was measured by applying a small pulse to the bias line and recording the response. The amplitude of the pulse was less than 5% of the bias. The time constants vary between 1-4.5 ms depending on the bias point. At the typical operating point that is R/R_n=0.3, the time constant is 1.4 ms. The time constants for the devices with relatively higher G, saturation power and noise (NEP=1 aW/√Hz) are shorter and vary between 0.4-0.7 ms in the transition.

IV. SUMMARY AND OUTLOOK

We have successfully fabricated various types of 8×9 S-band test arrays on 500 nm and 250 nm thick SiN membranes. The overall yield was almost 100 % for devices processed on 500 nm SiN an above 93% for devices processed on 250 nm SiN. The variation of the critical temperatures and normal resistances of devices across the arrays are less than 5% and 7% respectively. Large variations in saturation power and the thermal conductance (G) were measured. Despite having exact nominal device geometries this difference can be as large as factor of two with in an array. Optical microscopic inspection of the SiN legs revealed formation of spots on sections of the legs that can be partly the reason for the large variation in G. We also see deviations in the width of the SiN legs compared to the pattern on the photo mask (nominal value). The width of the legs for 8 pixels on the chip in Table 1 and 2 was measured between 3.3-3.6 μm, where the nominal value was 2 μm. This is mainly due to our current process that implies on-membrane lithography that suffers from reflection of the light from the Al layer under the membrane. The leg width variation alone cannot explain the large variation we see in our devices. We expect to solve this problem by acquiring Deep Reactive Ion Etching (DRIE) process that enables us to pattern the legs on bulk Si before etching away the substrate. The measured dark NEPs for devices fabricated on 250 nm SiN membrane are $5\text{-}6\times10^{-19}$ W/√Hz and for devices on 500 nm SiN membrane about $7\text{-}10\times10^{-19}$ W/√Hz. For long leg devices on a 500 nm membrane (Table 1 and 2) the measured NEP is about a factor of 2-2.5 higher than the expected NEP from the measured G using Eq. (1). For similar devices on a 250 nm membrane (Table 4), this factor increases to 3-3.5. This is somewhat surprising since less excess noise is expected from devices with lighter legs [5]. On the other hand we also see that the measured G's in Table 3 and 4 are about a factor of 4 smaller than for the devices in Table 1 and 2, while the membrane is only thinner by a factor of 2. Answering these questions requires further investigation. One possible explanation might be the accuracy of our G estimations. In presence of any external loading power, we would measure

lower saturation power and therefore underestimate the *G*. The matter is worse for more sensitive devices, where the saturation power is well below 10 fW.

We have made substantial progress towards a generic technology that is capable of delivering the required detectors for SAFARI. While most of the individual performance numbers are approaching or exceeding the requirements, there is still significant work required to optimize the designs. For the S-band pixels the fabrication process should be modified to use DRIE Si etching in order to achieve better uniformity in the array and to be able to scale up the current design to the full-size (43×43) array. In addition, to increase the sensitivity, the silicon nitride legs should be shorter, and therefore thinner and narrower.

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