Direct Integration of an SIS Mixer with a High-Impedance SiGe Low Noise Amplifier

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***Abstract*—We present the design and preliminary characterization of a cryogenic SiGe low noise amplifier optimized for direct integration with an SIS mixer. The LNA was designed to provide 25 dB gain over an IF frequency range of 4–8 GHz. The noise temperature of the LNA was simulated to be less than 6 K over the band at a power consumption of 720 μW. The LNA was directly connected to the SIS mixer block and measurement results yielded a minimum noise temperature of approximately 40 K at an LO frequency of 214 GHz.**

***Index Terms*—Silicon germanium, cryogenic, superconductor-insulator-superconductor mixer, low noise amplifier, focal plane array**

I. Introduction

The pumped output resistance of an SIS mixer is a function of both the LO frequency and the DC bias point. For broadband devices, this output resistance is typically well above the 50 Ω impedance level that is expected at the input of most cryogenic low noise amplifiers (LNAs). Thus, low noise amplifiers are usually matched to an SIS mixer either through an isolator [1], [2] or a matching network [3]–[6]. An alternative approach is to specifically design the amplifier to achieve nominal performance when its input is terminated by an SIS mixer. For large-scale focal plane arrays, a direct connection from an SIS mixer to the low noise amplifier is needed to increase scalability while maintaining a low-level of complexity. Silicon germanium (SiGe) cryogenic low noise amplifiers are an attractive option for the implementation of these large-scale systems, due to their increased yield and competitive low-GHz noise performance in comparison with HEMT based amplifiers [7], [8].

In this paper, we present the preliminary design, implementation, and characterization of a 4–8 GHz SiGe low-noise IF amplifier that is optimized for direct integration with an SIS mixer. The amplifier operates at a DC power consumption of just 720 μW and was designed to provide greater than 25 dB of power gain at a noise temperature ranging from 3–6 K over the frequency band.

II. Design and Fabrication

An SIS mixer has an IF output impedance that can be modeled by a parallel RC circuit, where the resistive component is given by the slope of the pumped I-V curve and the capacitance is related to a combination of the parallel plate capacitance of the SIS junction(s) and the capacitances associated with the embedding circuit. For our initial experiments, we selected an SIS mixer with the pumped IV curves shown in Fig. 1. The device is a three junction series array SIS mixer and is described in [9].

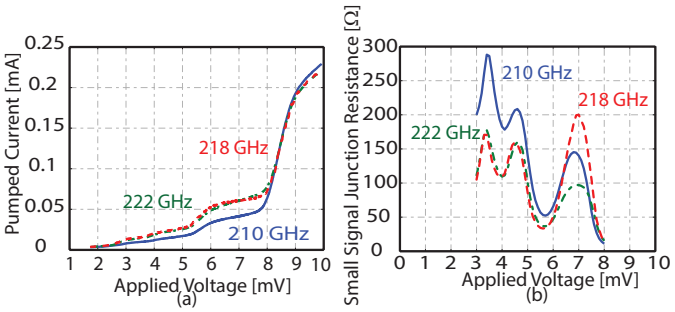


Fig. 1. SIS mixer properties. (a) Pumped IV curve for local oscillator frequencies of 210, 218, and 222 GHz. (b) Corresponding small-signal output resistance

To facilitate the design of an amplifier, the equivalent IF impedance of the SIS mixer was determined as follows. The conductance of the SIS junction was found using a linear regression. The resulting generator resistance is plotted in Fig. 1 as a function of bias voltage. Since the Y-factor is maximized near the center of the photon step, we have chosen a bias voltage of 7 mV as the operating point for our design. The corresponding output resistance of the mixer ranges from 100–200 Ω, depending on the local oscillator frequency. Rather than designing for a fixed LO frequency, we chose a generator impedance of 150 Ω, which is considerably higher than the 50 Ω impedance to which a typical LNA is matched. The intrinsic shunt capacitance of the SIS mixer is estimated to be 270 fF.

Designing a low-noise amplifier for a large generator impedance has pros and cons. For a given transistor technology, the optimum generator impedance is inversely proportional to the device periphery. As low-noise devices are typically biased at a fixed current density to realize the minimum noise, a smaller transistor periphery corresponds to a lower overall current, which translates to a decrease in power consumption. On the other hand, realizing a broadband matching network given a high generator impedance requires large reactances, which are not easy to realize using transmission line components.

As an initial demonstration, we have implemented a two-stage amplifier using discrete SiGe HBTs fabricated in the

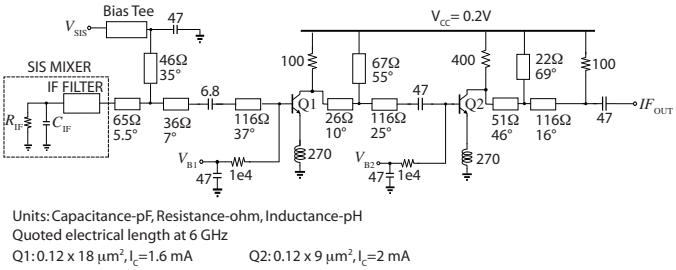


Fig. 2. Low noise amplifier schematic diagram.

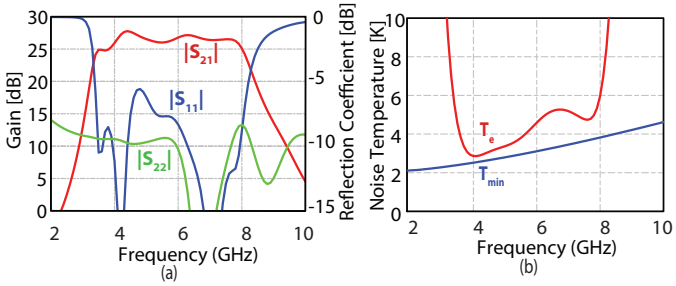
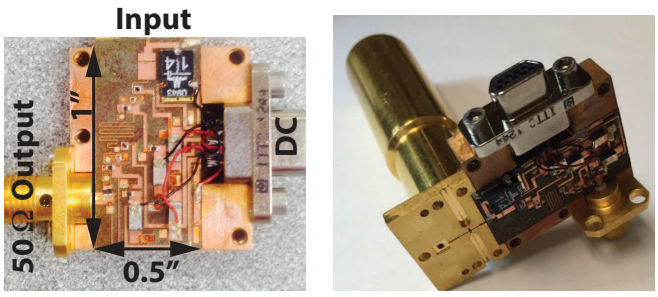


Fig. 3. Simulated performance of amplifier driven from 150 Ω generator impedance. The simulation also considers the 270 fF SIS capactiance as well as the series embedding network. (a) Scattering parameters (b) noise performance.

IBM BiCMOS8HP technology platform [10]. A schematic of the low noise amplifier appears in Fig. 2. The equivalent model of the SIS mixer is shown as a parallel RC block and the IF choke filter is modeled as a network block, the S-parameters of which were obtained using HFSS. The input matching network of the LNA serves to transform the output impedance of the SIS mixer to the impedance required to minimize the noise temperature of the amplifier over the 4–8 GHz frequency range. A dual-bias tee has been incorporated in the input matching network, with a shunt transmission line providing a path to supply the SIS bias voltage and a large resistor allowing for bias to be applied to the base of the HBT. The SIS bias is further filtered using a commercial surface mount bias-tee (Marki BT-0014SM-2). A degeneration inductance of approximately 270 pH is connected between the emitter of the input transistor and the chassis ground to enable simultaneous noise and impedance match. Resistors at the output of the first- and second-stage transistors ensure unconditional stability. Inter-stage and output matching networks are used to flatten the gain and provide output matching. Finally, the circuit is designed to run from a supply voltage of $V_{CC} = 0.2$ V at a current of $I_{CC} = 3.6$ mA, resulting in a total power consumption of 0.72 mW.

The scattering parameters and noise temperature of the amplifier were simulated using the models reported in [8] and the results appear in Fig. 3. These simulations are for a generator impedance of 150 Ω and include the effect of the intrinsic capacitance of the SIS mixer as well as the impedance transformation associated with the SIS IF filter network. All simulation results have been referenced to the plane of the intrinsic SIS mixer. From 4–8 GHz, the simulated power gain is higher than 25 dB, with less than 3 dB of gain variation



(a) (b)

Fig. 4. (a) Close-up of assembled low-noise amplifier. (b) Hybrid mixer/amplifier module. The mixer chip connects directly to the LNA via a 0.125mm, 1mm long wire.

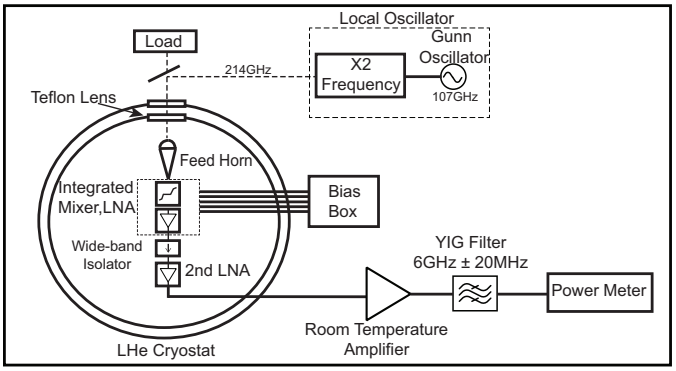


Fig. 5. Block diagram of the measurement setup.

across the band. The simulated input return loss is better than 7 dB over the entire band. For a generator impedance of 150 Ω, the simulated noise performance is below 6 K over the entire frequency range. Moreover, as the generator impedance is swept from 100–200 Ω, the noise performance is expected to change by less than 1 K over the majority of the frequency range.

III. Experimental Results

The amplifier was assembled using a mixture of bondable and surface mount components. A close-up of the circuit board is shown in Fig. 4(a). The board measures just 12.7 mm by 25.4 mm. A micro-D connector was incorporated into the housing to provide DC bias to the amplifier and the SIS mixer. The amplifier housing was designed to mate with an existing SIS mixer block [9], and a direct connection was made between the amplifier and the SIS mixer chip using a 0.125 mm wide, 1 mm long BeCu wire. The hybrid mixer/LNA assembly is shown in Fig. 4(b).

A block diagram and photograph of the measurement setup are shown in Figs. 5 and 6, respectively. The mixer/amplifier assembly was cooled to 4.2 K in a liquid helium cryostat. A 214 GHz local oscillator was quasi-optically coupled to the SIS mixer. The output of the LNA was further amplified by a second gain stage (LNF-LNC4-16A) before exiting the cryostat. A third amplifier (Minicircuits ZVA-183,2-18 GHz) at room temperature was used to further amplify the IF signal before band-limiting and power detection.

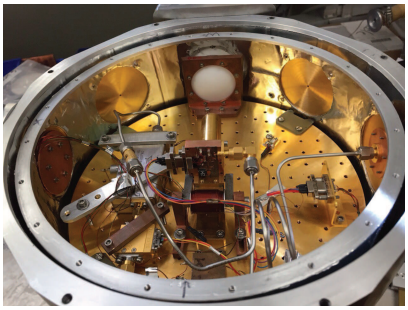


Fig. 6. Photograph of the measurement setup

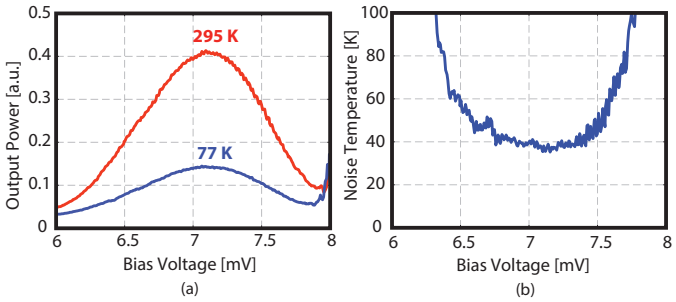


Fig. 7. (a) Output power measurement at 77 K and 295 K. (b) Double-sideband system noise temperature. These measurements are for an LO frequency of 214 GHz and an IF frequency of 6 GHz.

A double-sideband Y-factor measurement was carried out using ambient (295 K) and liquid nitrogen cooled black bodies (77K) placed in the input beam of the receiver. For these measurements, the IF was centered at 6 GHz with a bandpass of 40 MHz. For a local oscillator frequency of 214 GHz, the corresponding signal sideband frequencies were 208 and 220 GHz. The results of the Y-factor measurement, taken with the amplifier operating at its nominal bias point of 0.72 mW, are plotted in Fig. 7(a). The corresponding double-sideband system noise temperature appears in Fig. 7(b). The system noise temperature was found to be better than 40 K over a wide range of bias voltages. As these data include optical losses, the intrinsic performance of the mixer/amplifier assembly is expected to be better than that reported in Fig. 7(b).

IV. Conclusions

The results presented in this paper demonstrate the feasibility of achieving excellent system performance using sub-milliwatt SiGe LNAs directly integrated with SIS mixers. Although, these initial results are narrow-band, future adoption of this technology will require broadening the IF bandwidth. A logical next step is to demonstrate the operation of the SIS/LNA assembly over both wide RF input bandwidths as well as over at least a 4–8 GHz IF bandwidth. If successful, the combination of ultra-low-power consumption and tight integration is expected to impact the scalability of SIS focal plane array systems.

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