

20 gigasample per second analog-to-digital conversion for ultra-wideband radio astronomy

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Abstract— As receiver bandwidth increases, it becomes necessary to increase the speed of the analog-to-digital conversion (ADC) as well as the digital signal processing (DSP) in the system back end. Otherwise, one would require a very complex filter bank system employing a large number of analog modules to break the IF bandwidth into small blocks for digital sampling and signal processing. Fortunately, a new generation of ADC with multi-GHz bandwidth has emerged, and DSP technology has been following Moore's law. A 26 gigasample per second (GSa/s) 3-bit ADC is commercially available from Hittite, Inc (recently acquired by Analog Devices). Using this ADC, SAO, in collaboration with Techn Instruments, has demonstrated high fidelity 3-bit 20 GSa/s conversion with data captured directly and asynchronously by a SERDES transceiver on the Xilinx Virtex 7 XC7VX690T Field Programmable Gate Array (FPGA). This development suggests that IF bandwidths in multiples of ~10 GHz could soon be handled by a single compact module.

I. INTRODUCTION

In 2013 with "Competitive Grants Program For Science" (CGPS) funding from Smithsonian Institution (SI) the SAO DSP group embarked on a project to design a circuit module based on a Hittite 3-bit (with overflow) 26 GSa/s ADC. This builds on our work on a 5 GSa/s ADC presently being applied at the Submillimeter Array (SMA) [1].

The ADC part number is HMCAD5831LP9BE [2], and it has been designed onto a board with an FMC (Vita 57.1 standard) connector interface to a Xilinx development board, the VC709[3]. This carries a powerful XC7VX690T FPGA. 80 GTH Multi-Gigabit Serial Transceivers are available on the FPGA. 10 GTH pairs brought out to the FMC connector on the VC709 evaluation board.

The GTH Transceiver is a sophisticated subsystem capable of transmitting and receiving serial data at rates up to 13.1 Gb/s per channel (though the -2 speed grade FPGA on the VC709 is limited to 11Gb/s operation). The transmitter and receiver each have several functional blocks that are critical for reliable reception of data from the Hittite ADC. The Hittite ADC is a "3 plus" bit resolution part, outputting 3 bits plus an over-range bit, in other words encoding a total of 10 analog levels. The digital output is demultiplexed into two 4-bit paths, with each path transmitting data at half the sample rate, or 10Gb/s for a 20GSPS conversion rate. Thus eight GTH receiver channels are sufficient to receive the data.

An XOR input on the ADC allows the user to multiply the digital data out of the chip by a modulating signal, to ensure there are enough data transitions for successful clock recovery. An INHIBIT input to the ADC forces the ADC data to zero, causing the modulation sequence to appear at all ADC output pairs.

II. PCB DESIGN DETAILS

A critical requirement for achieving error-free data transmission from the ADC to the FPGA is the use of a modulation sequence with which the eight serial data streams are XORed internal to the ADC chip. The GTH receivers detect the clock embedded in the data stream by sensing the data edges; for this clock detection system to achieve and retain lock, the data edges must occur sufficiently often. One GTH transmitter is used to provide this modulation sequence in a very flexible manner.

The HMC723 D-flip-flop is provided to synchronize the incoming modulation stream to a half-sample-rate clock provided by the ADC. This relaxes the timing requirement of the modulation stream from the 20GHz clock domain of the ADC to the 10GHz Fsample/2 domain. A variable delay chip, HMC856, is provided between the DFF and the ADC chip to adjust the timing of the synchronized sequence to meet the setup and hold requirements of the ADC's internal registers.

A pair of HMC859 divide-by-eight chips create the 156.25 MHz reference clock necessary for data reception in the GTH receivers from the 10GHz clock output from the ADC. DC power is supplied from the +12v available on the FMC connector. Two DC/DC switching converters convert +12 to the -5.0 and -3.3v supply rails required by the ADC and other components.

D/A converters are provided to set the ADC's REFT and REFB levels, and thus the conversion range. The signal input of the ADC is single-ended, dc-coupled, and is buffered internally by an emitter-follower stage, so the signal applied to the ADC core is offset by the Vbe of this stage. The DACs set the top and bottom of the reference ladder to the desired input range offset by this value. The nominal settings are REFT = -900mv, REFB = -(900 + 256) mv, and thus the nominal input span is 256mv, or 1mv per LSB. The board sits piggyback on the VC709 and connects via a Samtec ASP- 134488-01 FMC-

HPC (FPGA Mezzanine Connector- High Pin Count) connector.

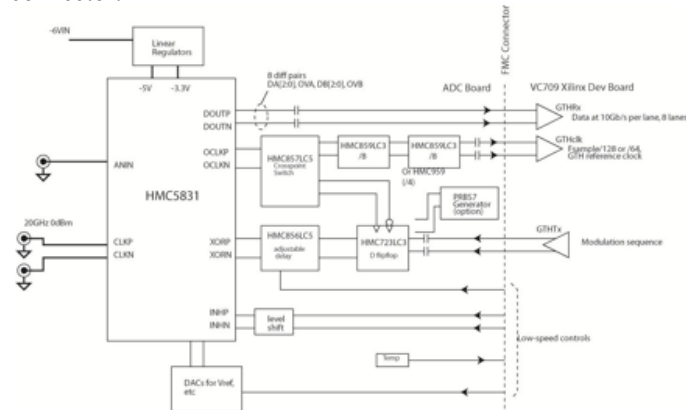


Fig. 1 Block diagram of the circuit board designed to carry the 20 GSa/s ADC

Serial data output to or input from the FPGA are at “Current Mode Logic” (CML) levels below ground and must therefore be AC-coupled to the FPGA. A long time constant is desirable here to provide a long averaging time for low dc disparity. 100nF “ultra-wideband” capacitors from American Technical Ceramics are used to provide a 5us (100nf * 50 ohm half-circuit termination resistance) time constant with low losses at RF frequencies:

III. MODULATING SEQUENCE

The modulating sequence with which the ADC data is XORED must meet two criteria:

- It must have low dc disparity. In other words it must have approximately the same number of 1s and 0s so that, when the ADC output is inhibited, the ac-coupled sequence will not contain an appreciable DC component that would degrade the data eye.
- It must result in a sufficient frequency of data transitions in the modulated data streams such that the GTH receiver clock recovery system can function properly.

Additionally, the modulation sequence may have the word- and channel-alignment codes built-in to permit the Rx logic to do word- and channel-alignment. Note that the PRBS sequence is only used for adjustment of the phase of the modulation data and is not used as the modulation sequence itself.

The second requirement demands that the chosen modulation sequence have an extremely low probability of aligning with the ADC output data; if the two sequences were to align for a sufficiently long period, the receivers would see no clock transitions and would fall out of lock. This could cause one or more lanes to lose alignment with others. The maximum transition-free interval over which the receiver clock recovery system will stay in lock is not specified in the Xilinx documentation.

We experimented with several sequences and chose a slightly modified 250MHz square wave. The 640-bit sequence contains eight cycles of this waveform, plus one instance of the comma (for word alignment) and one instance of the channel-bond sequence (for lane-to-lane alignment). A few cycles of the modulating sequence can be seen in figure 2.



Fig. 2 Sample few cycles of modulation sequence.

The single spike positive is one bit of the comma; the extended chattering area is the channel-bond sequence. An RF input high-passed at say 500MHz would have virtually zero probability of ever aligning with this sequence.

The firmware was developed in Xilinx's Vivado design environment (v2014.2) and comprises a MicroBlaze soft processor, many standard MicroBlaze peripherals, and a custom peripheral which includes the six GTH receivers, one GTH transmitter, modulation and demodulation sources, and the 10Gb/s Ethernet components necessary for high-speed data output.

IV. TEST RESULTS

A. Noise tests

With a noise generator to the ADC board via the VLF-7200 LPF and adjusted the noise level to about 1.6 LSBs rms. We acquired data, computed a 2048-point power spectrum, and averaged the results for 1000 such records. Figure 3 shows the resultant spectrum. Note the stop bands are at a level of about -14 dBc as expected for 3-bit sampling.

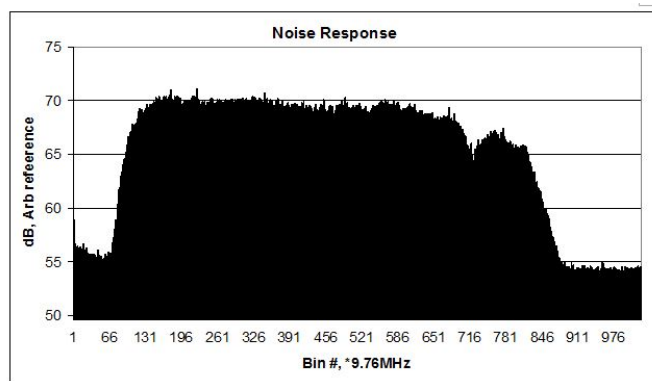


Fig. 3 Spectrum of low pass filtered wideband noise sampled at 20 GSa/s.

B. Sine wave tests

We tested the dynamic response to a sine wave with a 100MHz synthesizer, phase-locked to the ADC clock generator. Spectra are taken with no noise added to the sine wave, then then with 0.5 LSB of noise to the sine wave suppressed the spurs due to coarse quantization. The spectra shown in figure 4 are the result of accumulating about 150,000

sine wave samples. The Spurious Free Dynamic Range at -24 dBc in the non-dithered case is as expected for 3-bit sampling.

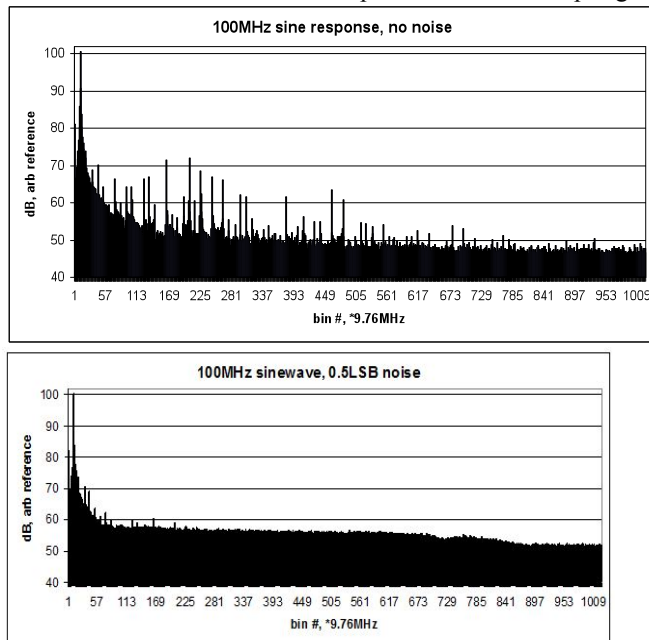


Fig. 4 Spectrum 100 MHz sine response, The top panel shows the spectrum with no noise added, the bottom with 0.5 LSB of noise dithering. Adding some noise suppresses the spurs due to quantization and improves Spurious Free Dynamic Range (SFDR).

C. Sparkle codes

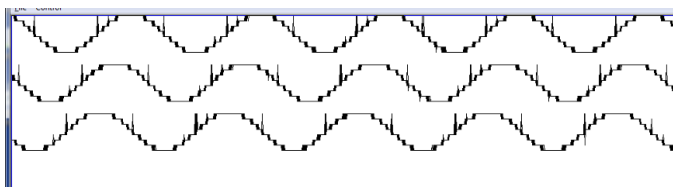


Fig. 5 Sine wave snapshot showing sparkle codes. frequency of occurrence is exaggerated in the above display due to infinite persistence of the plotting program.

"Sparkle codes" often seen in flash converters, essentially a conversion error. Hittite reports that others have seen these. Inspection of the waveforms indicate that they occur about

once in 3000 points for this waveform, typically at the 011 to 100 or 100 to 011 code transition (but not always). Figure 5 shows a snapshot of time domain sine wave data showing the sparkle codes manifest as glitches in the waveform.

V. CONCLUSIONS

We have evaluated the fastest ADC integrated circuit available in commercial and industrial markets (the 26 GSps Hittite HMC5913) evaluated its performance for the noise like signals typical in radio astronomy digital signal processing. The interface via the FMC connector and GTH receivers using the GTH transmitter as a modulation source is extremely robust, and the ADC performs in accordance with its expectations up to 22 GSa/s. Sparkle codes occur with a surprising frequency, but don't seem to degrade dynamic performance appreciably. We expect this ADC might find application as high frequency radio observatories, such as those approaching the terahertz bands, for example ALMA [4], and SMA.

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